FUJITSU SEMICONDUCTOR
DATA SHEET

Revision 1.0

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89930C Series

MB89P935C/PV930A

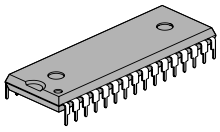
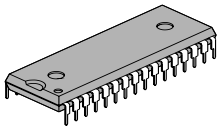
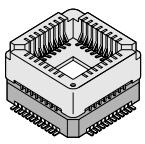
■ DESCRIPTION

The MB89930C series is a line of single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as timers, serial interfaces, A/D converter and external interrupts.

■ FEATURES

- MB89600 Series CPU core
- Minimum execution time: 0.4 µs/10MHz
- Interrupt processing time: 3.6 µs/10MHz
- I/O ports: max. 21 channels
- 21-bit timebase timer
- 8-bit PWM timer
- 8/16-bit capture timer/counter
- 10-bit A/D converter: 8 channels
- UART
- 8-bit serial I/O
- External interrput 1 (Edge): 3 channels
- External interrupt 2 (Level): 8 channels
- Wild Register: 2 bytes
- OTPROM Read protection (Refer to "■ Programming the OTPROM in MB89P935C")
- Low-power consumption modes (sleep mode and stop mode)
- DIP and SH-DIP package
- CMOS Technology

■ PACKAGE

32-pin plastic DIP	32-pin plastic SH-DIP	48-pin ceramic MQFP
		
(DIP-32P-M04)	(DIP-32P-M05)	(MQP-48C-P01)

■ PRODUCT LINEUP

Part number / Parameter	MB89P935C	MB89PV930A
Classification	One-time PROM product (read protection)	Piggyback/evaluation product (for evaluation and development)
ROM size	16K x 8-bit (internal PROM)	32K x 8-bit (external EPROM)
RAM size	512 x 8 bits	
CPU functions	Number of instructions: : 136 Instruction bit length: : 8 bits Instruction length: : 1 to 3 bytes Data bit length: : 1, 8, 16 bits Minimum execution time: : 0.4 µs to 6.4 µs(10 MHz) Minimum interrupt processing time: : 3.6 µs to 57.6 µs(10 MHz)	
Ports	General-purpose I/O ports (CMOS): 21 (also serve as peripherals) (4 ports can be set as N-ch open-drain type)	
21-bit timebase timer	21-bit Interrupt cycle: 0.82, 3.3, 26.2, or 419.4 ms at 10-MHz main clock	
Watchdog timer	Reset generation cycle: 209.7ms minimum at 10-MHz main clock	
8-bit PWM timer	8-bit interval timer operation (square output capable, operating clock cycle: 1 tinst, 16 tinst, 64 tinst, and 8/16-bit capture timer/counter output) 8-bit resolution PWM operation (conversion cycle: 256 tinst, 4096 tinst, 16384 tinst and 256 times 8/16-bit capture timer/counter output)	
8/16-bit capture timer/counter	8-bit capture timer/counter x 1 channel + 8-bit timer or 16-bit capture timer/counter x 1 channel Capable of event count operation and square wave output using exteranl clock input with 8-bit timer 0 or 16-bit counter	
UART	Transfer data length: 6/7/8 bits Transfer rate: 300 to 9600 bps at 10 MHz	
8-bit Serial I/O	8 bits LSB first/MSB first selectable One clock selectable from four operation clocks (one external shift clock, three internal shift clocks: 2 tinst, 8 tinst and 32 tinst)	
12-bit PPG timer	Output frequency: Pulse width and cycle selectable	
External interrupt 1 (wake-up function)	3 channels (interrupt vector, request flag, request output enable) Edge selectable (Rising edge, falling edge, or both edges) Also available for resetting stop/sleep mode (Edge detectable even in stop mode)	
External interrupt 2 (wake-up function)	1 channel with 8 inputs (Independent L-level interrupt and input enable) Also available for resetting stop/sleep mode (Level detectable even in stop mode)	
10-bit A/D converter	10-bit precision x 8 channels A/D conversion function (Conversion time: 38 tinst) Continuous activation by 8/16-bit timer/counter output or timebase timer counter	
Wild Register	8-bit x 2	
Standby mode	Sleep mode and Stop mode	
Power supply voltage	3.0V to 5.5V	2.7V to 5.5V

Note: 1 Tinst = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89P935C	MB89PV930A
DIP-32P-M04	O	X
DIP-32P-M05	O	X
MQP-48C-P01	X	O

O : Availabe X : Not available

■ DIFFERENCES AMONG PRODUCTS

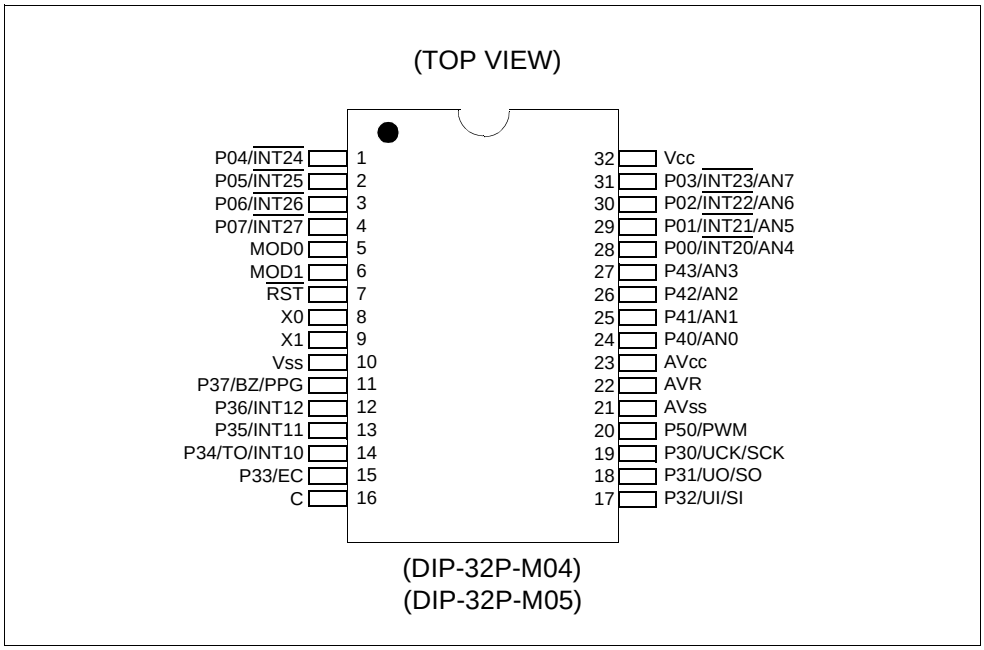
1. A/D Converter Power Supply Pin (AV_{CC}) and Reference Voltage Input Pin (AVR)

There are AV_{CC} and AVR pins in MB89P935C. They are absent in MB89PV930A. Hence, the electrical characteristics of MB89P935C is different from that of MB89PV930A. (Refer to "■ ELECTRICAL CHARACTERISTICS 5. A/D Converter Electrical Characteristics")

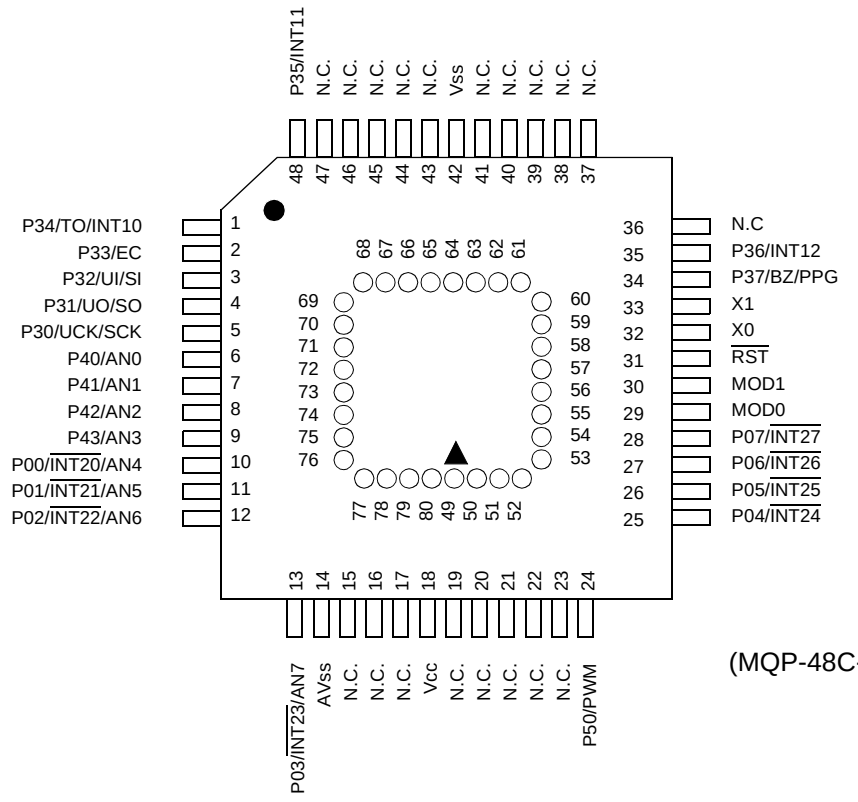
2. Curent Consumption

In the case of the MB89PV930A, add the current consumed by the EPROM which is connected to the top socket.

■ PIN ASSIGNMENT



(TOP VIEW)



(MQP-48C-P01)

Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol
49	Vpp	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	Vss	72	N.C.	80	Vcc

N.C.: As connected internally, do not use.

■ PIN DESCRIPTION

Pin Number		Pin Name	I/O Circuit Type	Function
DIP*1	MQFP*2			
8	32	X0	A	Pins for connecting the crystal resonator for the main clock. To use an external clock, input the signal to X0 and leave X1 open.
9	33	X1		
5	29	MOD0	B	Memory access mode setting input pins. Connect the pin directly to Vss.
6	30	MOD1		
7	31	$\overline{RST}$	C	Reset I/O pin. The pin is N-ch open-drain type with pull-up resistor and a hysteresis input as well. The pin outputs the “L” level when an internal reset request is present. Inputting an “L” level initializes internal circuits.
28 to 31	10 to 13	P00/$\overline{INT20}$/AN4 to P03/$\overline{INT23}$/AN7	G	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2 or as an A/D converter analog input. The input of external interrupt 2 is a hysteresis input.
1 to 4	25 to 28	P04/$\overline{INT24}$ to P07/$\overline{INT27}$	D	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2. The input of external interrupt 2 is a hysteresis input.
19	5	P30/UCK/SCK	D	General-purpose CMOS I/O port. This pin also serves as the clock I/O pin for the UART or 8-bit serial I/O. The resources is a hysteresis input.
18	4	P31/UO/SO	E	General-purpose CMOS I/O port. This pin also serves as the data output pin for the UART or 8-bit serial I/O.
17	3	P32/UI/SI	D	General-purpose CMOS I/O port. This pin also serves as the data input pin for the UART or 8-bit serial I/O. The resources is a hysteresis input.
15	2	P33/EC	D	General-purpose CMOS I/O port. This pin also serves as the external clock input pin for the 8/16-bit capture timer/counter. The resource is a hysteresis input.
14	1	P34/TO/INT10	D	General-purpose CMOS I/O port. This pin also serves as the output pin for the 8/16-bit capture timer/counter or as the input pin for external interrupt 1. The resource is a hysteresis input.
13,12	48, 35	P35/INT11, P36/INT12	D	General-purpose CMOS I/O ports. These pins also serve as the input pins for external interrupt 1. The resource is a hysteresis input.
11	34	P37/BZ/PPG	E	General-purpose CMOS I/O port. This pin also serves as the buzzer output pin or the 12-bit programmable pulse generator output.
20	24	P50/PWM	E	General-purpose CMOS I/O port. The pin also serves as the 8-bit PWM output pin.
24 to 27	6 to 9	P40/AN0 to P43/AN3	F	General-purpose CMOS I/O ports. These pins can also be used as N-channel open-drain ports. The pins also serve as A/D converter analog input pins.

*1: DIP-32P-M04 and DIP-32P-M05

*2: MQP-48C-P01

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Pin No.		Pin Name	I/O Circuit Type	Function
DIP*1	MQFP*2			
32	18	Vcc	—	Power supply pin
10	42	Vss	—	Power (GND) pin
23	—	AVcc	—	Power supply pin for A/D converter.
21	14	AVss	—	Power supply pin for A/D converter. Apply equal potential to this pin and the Vss pin.
22	—	AVR	—	Reference voltage input pin for the A/D converter.
16	—	C	—	Capacitance pin for regulating the power supply. Connect an external ceramic capacitor of about 0.1μF

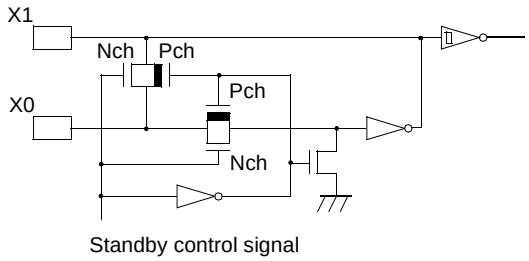
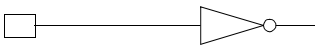
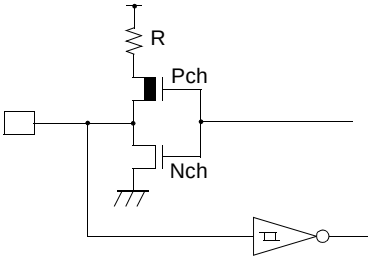
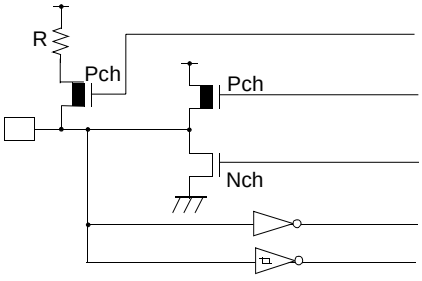
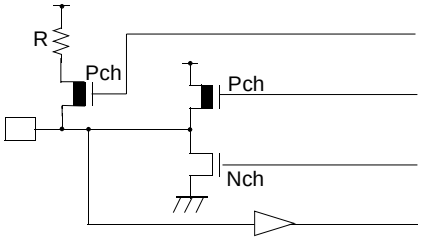
*1: DIP-32P-M04 and DIP-32P-M05

*2: MQP-48C-P01

•External EPROM Socket (MB89PV930A only)

Pin Number MQFP*1	Pin Name	I/O	Function
49	V_{pp}	O	“H” level output pin
50 51 52 53 54 55 58 59 60	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins.
61 62 63	O1 O2 O3	I	Data input pins.
64	V_{SS}	O	Power supply pin (GND).
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins.
70	$\overline{CE}$	O	Chip enable pin for the ROM. Outputs “H” in standby mode.
71	A10	O	Address output pin.
72	$\overline{OE}$	O	Output enable pin for the ROM. Always outputs “L”.
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins.
80	V_{CC}	O	Power supply pin for the EPROM.
56 57 72 74	N.C.	—	Internally connected pins. Always leave open.

■ I/O CIRCUIT TYPE

I/O Circuit Type	Circuit	Remarks
A		• Crystal oscillation type
B		• CMOS input
C		• The pull-up resistance (P-channel) Approx. 50 kΩ. • Hysteresis input
D		• CMOS output • CMOS input • Hysteresis input (Resource input) • Selectable pull-up resistor Approx. 50 kΩ.
E		• CMOS output • CMOS input • Selectable pull-up resistor Approx. 50 kΩ

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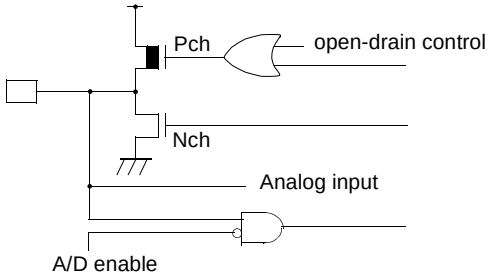
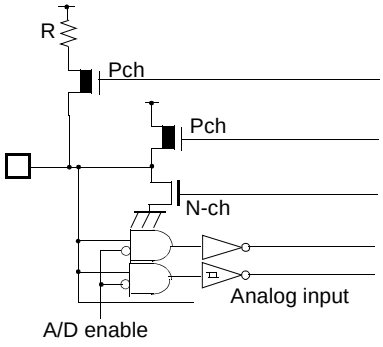
F		• CMOS output • CMOS input • Analog input • N-ch open-drain output available
G		• CMOS output • CMOS input • Hysteresis input (Resource input) • Analog input • Selectable pull-up resistor Approx. 50kΩ.

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor of at least 2 kilohms between the pin and the power supply.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Treatment of Power Supply Pins on Microcontrollers with A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

7. About the Wild Register Function

No wild register can be debugged on the MB89PV930A. For the operation check, test the MB89P935C installed on a target system.

8. Program Execution in RAM

When the MB89PV930A is used, no program can be executed in RAM.

■ PROGRAMMING THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Programming Socket Adaptor

To program to the PROM using an EPROM programmer, use the socket adaptor (manufacturer: Sun Hayato Co., Ltd.) listed below.

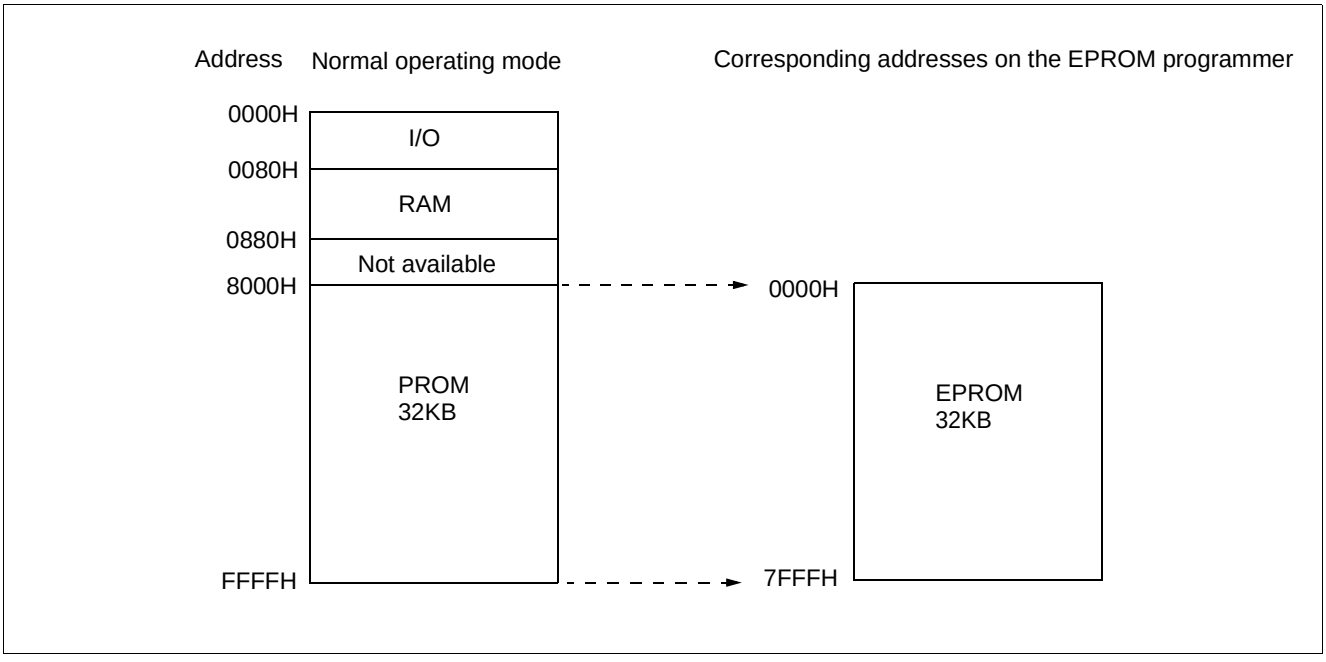
Package	Adaptor socket part number
LCC-32	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3986-0403

FAX 81-3-5396-9106

3. Memory Space

Memory space in each mode is diagrammed below.



4. Programming to the EPROM

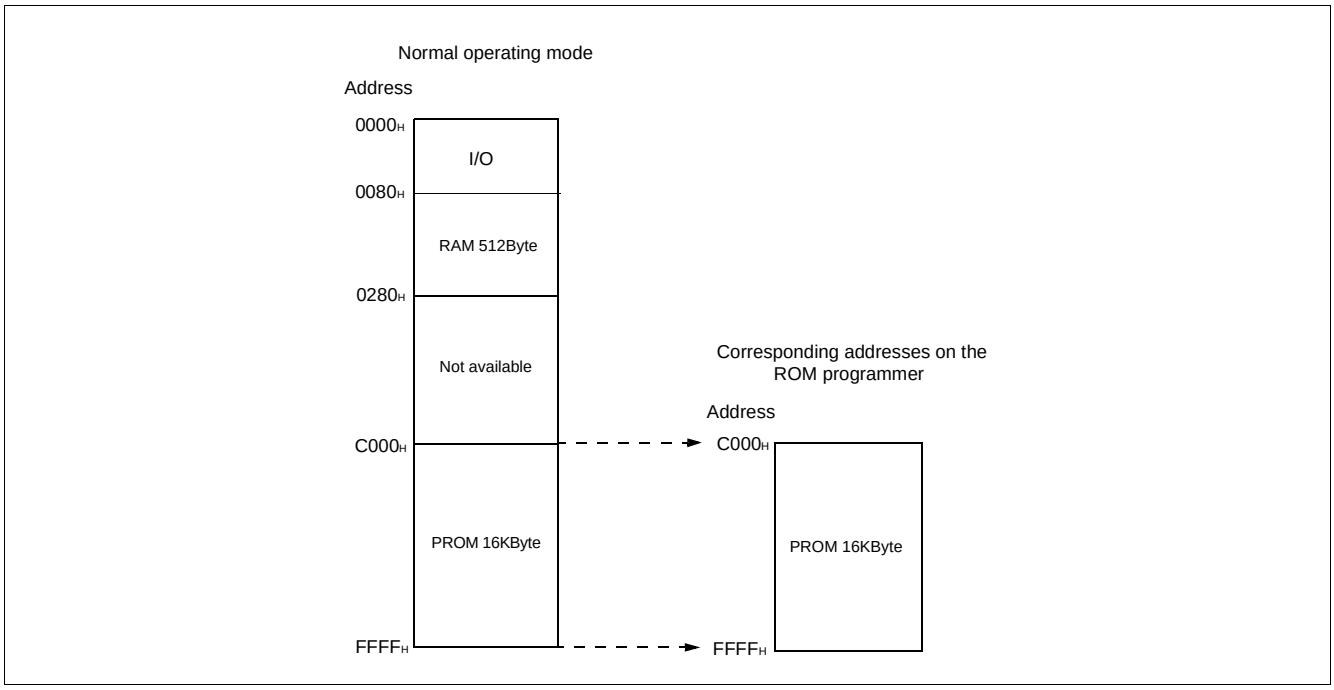
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ PROGRAMMING THE OTPROM IN MB89P935C

1. Memory Space



2. Programming the OTPROM

- To program the OTPROM using EPROM programmer AF200 (manufacturer: Yokogawa Digital Computer Corp.).

  Inquiry : Yokogawa Digital Computer Corp. : TEL (81)-42-333-6224

- To program the OTPROM using FUJITSU MCU programmer MB91919-001.

  Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770

  FAX (65)-2810220

Note : Programming the OTPROM in MB89P935C is serial programming mode only.

3. Programming Adaptor for OTPROM

- To program the OTPROM using EPROM programmer AF200, use the programming adaptor (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adaptor socket part number
DIP-32P-M04	ROM3-FPT30M02-8LA-FJ
DIP-32P-M05	Not available

Inquiry : Sun Hayato Co., Ltd : TEL (81)-3-3986-0403

FAX (81)-3-5396-9106

- To program the OTPROM using FUJITSU MCU programmer MB91919-001, use the programming adaptor listed below.

Package	Adaptor socket part number
DIP-32P-M04	MB91919-809 + MB91919-800
DIP-32P-M05	MB91919-814 + MB91919-800

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770

FAX (65)-2810220

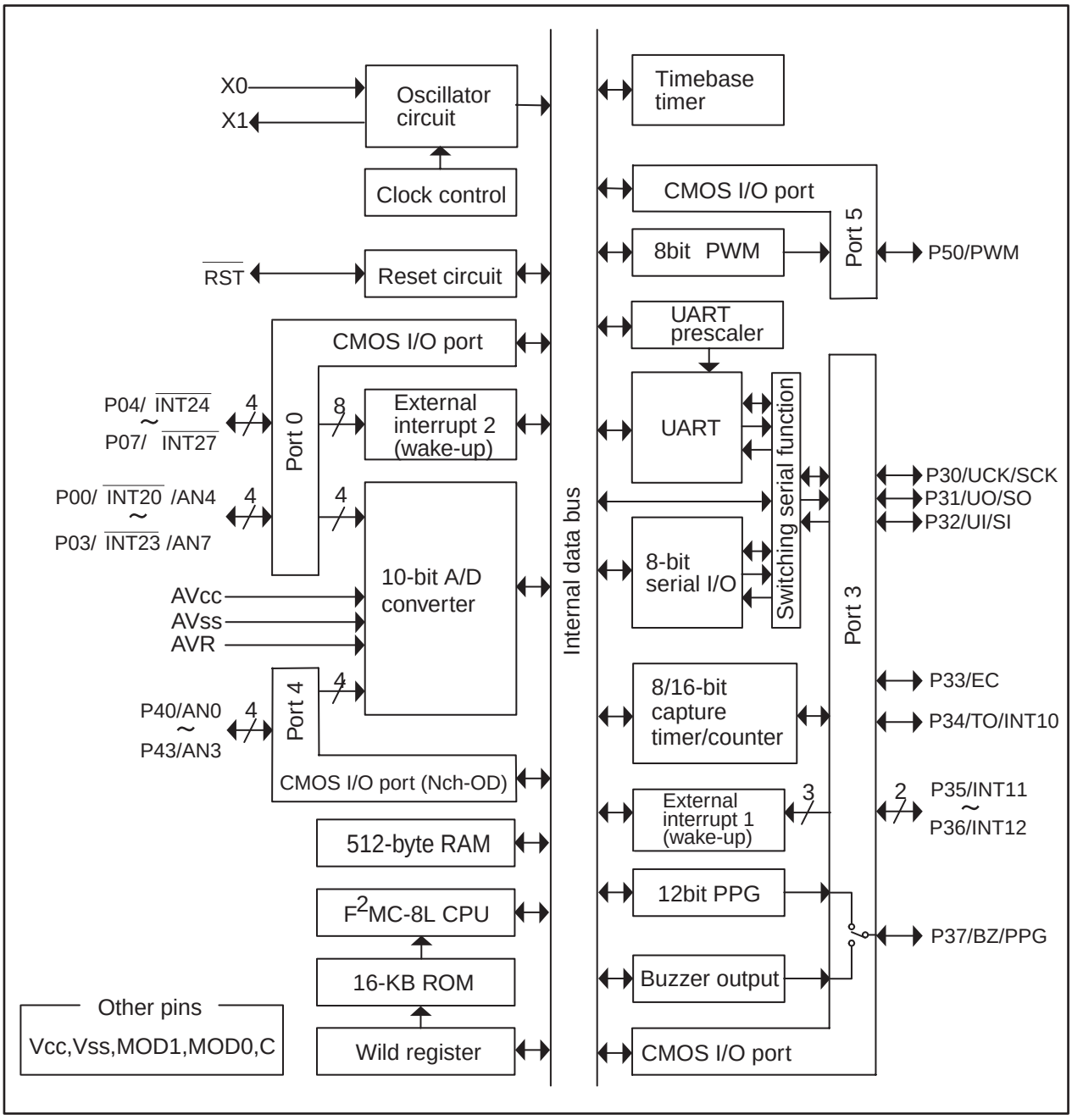
4. OTPROM Content Protection

OTPROM content can be read using serial programmer if the OTPROM content protection mechanism is not activated.

One predefined area of the OTPROM ($FFFC_H$) is assigned to be used for preventing the read access of OTPROM content. If the protection code "00_H" is written in this address ($FFFC_H$), the OTPROM content cannot be read by any serial programmer.

Note : The program written into the OTPROM cannot be verified once the OTPROM protection code is written ("00_H" in $FFFC_H$). It is advised to write the OTPROM protection code at last.

■ Block Diagram

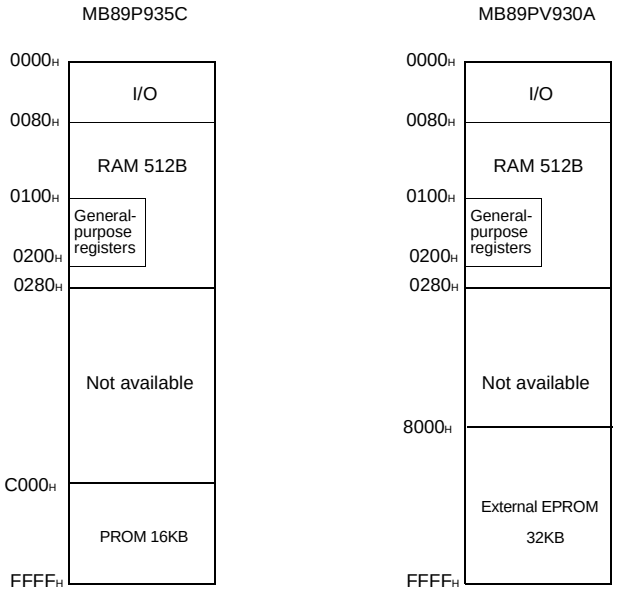


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89930C series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89930C series is structured as illustrated below.

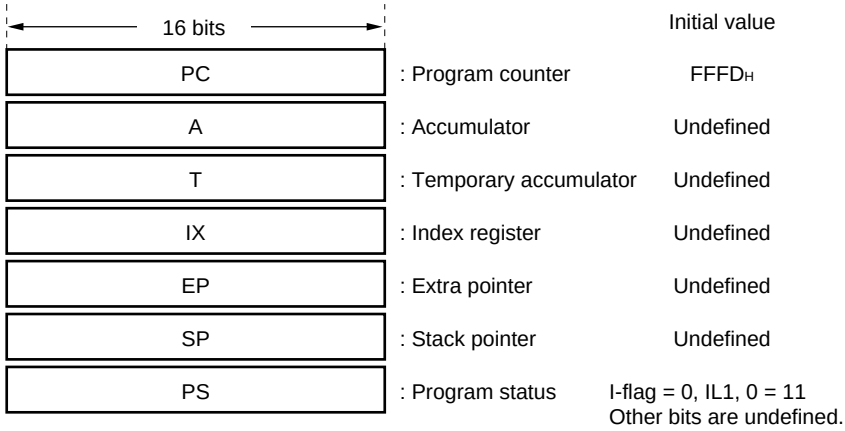
Memory Space



2. Registers

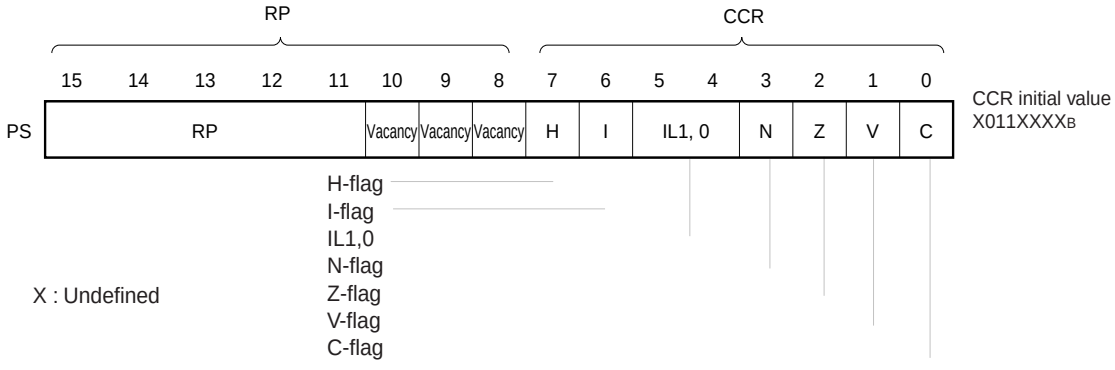
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



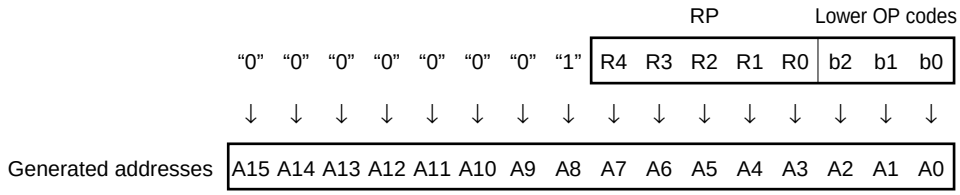
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

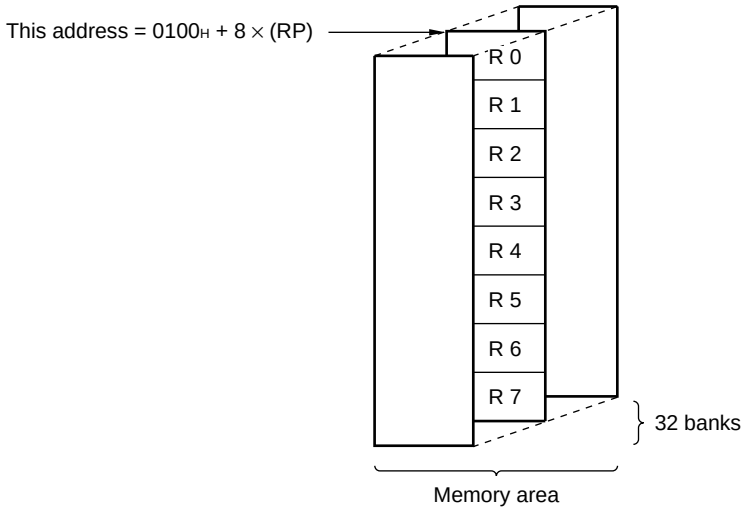
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit resister for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89930C series. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00H	PDR0	Port 0 data register	R/W	XXXXXXXXB
01H	DDR0	Port 0 data direction register	W	00000000B
02H to 06H	(Reserved)			
07H	SYCC	System clock control register	R/W	1--11100B
08H	STBC	Standby control register	R/W	00010---B
09H	WDTC	Watchdog timer control register	W	0---XXXXB
0AH	TBTC	Timebase timer control register	R/W	00---000B
0BH	(Reserved)			
0CH	PDR3	Port 3 data register	R/W	XXXXXXXXB
0DH	DDR3	Port 3 data direction register	W	00000000B
0EH	RSFR	Reset flag register	R	XXXX----B
0FH	PDR4	Port 4 data register	R/W	----XXXXB
10H	DDR4	Port 4 direction register	R/W	----0000B
11H	OUT4	Port 4 output format register	R/W	----0000B
12H	PDR5	Port 5 data register	R/W	-------XB
13H	DDR5	Port 5 data direction register	R/W	-------0B
14H	RCR21	12-bit PPG control register 1	R/W	00000000B
15H	RCR22	12-bit PPG control register 2	R/W	--000000B
16H	RCR23	12-bit PPG control register 3	R/W	0-000000B
17H	RCR24	12-bit PPG control register 4	R/W	--000000B
18H	BZCR	Buzzer register	R/W	-----000B
19H	TCCR	Capture control register	R/W	00000000B
1AH	TCR1	Timer 1 control register	R/W	00000000B
1BH	TCR0	Timer 0 control register	R/W	00000000B
1CH	TDR1	Timer 1 data register	R/W	XXXXXXXXB
1DH	TDR0	Timer 0 data register	R/W	XXXXXXXXB
1EH	TCPH	Capture data register H	R	XXXXXXXXB
1FH	TCPL	Capture data register L	R	XXXXXXXXB
20H	TCR2	Timer output control register	R/W	------00B
21H	(Reserved)			
22H	CNTR	PWM control register	R/W	0-000000B
23H	COMR	PWM compare register	W	XXXXXXXXB
24H	EIC1	External interrupt 1 control register 1	R/W	00000000B
25H	EIC2	External interrupt 1 control register 2	R/W	----0000B
26H	(Reserved)			
27H				
28H	SMC	Serial mode control register	R/W	00000-00B
29H	SRC	Serial rate control register	R/W	--011000B
2AH	SSD	Serial status and data register	R/W	00100-1XB

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
$2B_H$	SIDR	Serial input data register	R	$XXXXXXXX_B$
	SODR	Serial output data register	W	11111111_B
$2C_H$	UPC	Clock division selection register	R/W	$----0010_B$
$2D_H$ to $2F_H$	(Reserved)			
30_H	ADC1	A/D converter control register 1	R/W	-0000000_B
31_H	ADC2	A/D converter control register 2	R/W	-0000001_B
32_H	ADDH	A/D converter data register H	R/W	$------XX_B$
33_H	ADDL	A/D converter data register L	R/W	$XXXXXXXX_B$
34_H	ADEN	A/D enable register	R/W	00000000_B
35_H	(Reserved)			
36_H	EIE2	External interrupt 2 control register1	R/W	00000000_B
37_H	EIF2	External interrupt 2 control register 2	R/W	$-------0_B$
38_H	(Reserved)			
39_H	SMR	Serial mode register	R/W	00000000_B
$3A_H$	SDR	Serial data register	R/W	$XXXXXXXX_B$
$3B_H$	SSEL	Serial function switching register	R/W	$-------0_B$
$3C_H$ to $3F_H$	(Reserved)			
40_H	WRARH1	Upper-address setting register 1	R/W	$XXXXXXXX_B$
41_H	WRARL1	Lower-address setting register 1	R/W	$XXXXXXXX_B$
42_H	WRDR1	Data setting register 1	R/W	$XXXXXXXX_B$
43_H	WRARH2	Upper-address setting register 2	R/W	$XXXXXXXX_B$
44_H	WRARL2	Lower-address setting register 2	R/W	$XXXXXXXX_B$
45_H	WRDR2	Data setting register 2	R/W	$XXXXXXXX_B$
46_H	WREN	Wild-register enable register	R/W	$XXXXXX00_B$
47_H	WROR	Wild-register data test register	R/W	$------00_B$
48 to $6F_H$	(Reserved)			
70_H	PUL0	Port 0 pull-up setting register	R/W	00000000_B
71_H	PUL3	Port 3 pull-up setting register	R/W	00000000_B
72_H	PUL5	Port 5 pull up setting register	R/W	$-------0_B$
73_H to $7A_H$	(Reserved)			
$7B_H$	ILR1	Interrupt level setting register 1	W	11111111_B
$7C_H$	ILR2	Interrupt level setting register 2	W	11111111_B
$7D_H$	ILR3	Interrupt level setting register 3	W	11111111_B
$7E_H$	ILR4	Interrupt level setting register 4	W	11111111_B
$7F_H$	ITR	Interrupt test register	Not available	$------00_B$

- : Unused, X : Undefined

Note : Do not use reserved area.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	AV_{CC} must not exceed VCC
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	AVR must not exceed AVcc
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 6.0	V	
“L” level maximum output current	I_{OL1}	—	20	mA	Pins P40 to P43
	I_{OL2}	—	10	mA	Pin excluding P40 to P43
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current x operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“H” level maximum output current	I_{OH}	—	–10	mA	
“H” level average output current	I_{OHAV}	—	–2	mA	Average value (operating current x operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor device can be permanently damaged by application of stress (voltage, current, temperature etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AVss = Vss = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	3.0*	5.5	V	Operation assurance range
		1.5	5.5	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	4.5	AV_{CC}	V	
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	P00 to P07, P30 to P37, P40 to P43, P50, UI/SI
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	$\underline{\text{MOD0}}$/1, $\overline{\text{RST}}$, EC, $\overline{\text{INT20}}$ to INT27, UCK/SCK, INT10 to INT12
"L" level input voltage	V_{IL}	V_{SS} - 0.3	0.3 V_{CC}	V	P00 to P07, P30 to P37, P40 to P43, P50, UI/SI
	V_{ILS}	V_{SS} - 0.3	0.2 V_{CC}	V	$\underline{\text{MOD0}}$/1, $\overline{\text{RST}}$, EC, $\overline{\text{INT20}}$ to INT27, UCK/SCK, INT10 to INT12
Open-drain output pin application voltage	V_D	V_{SS} - 0.3	V_{CC} + 0.3	V	P40 to P43
Operating temperature	T_A	–40	+85	°C	

*: This value depend on the operating conditions and the analog assurance range. See Figure 1 and "5. A/D converter Electrical Characteristics."

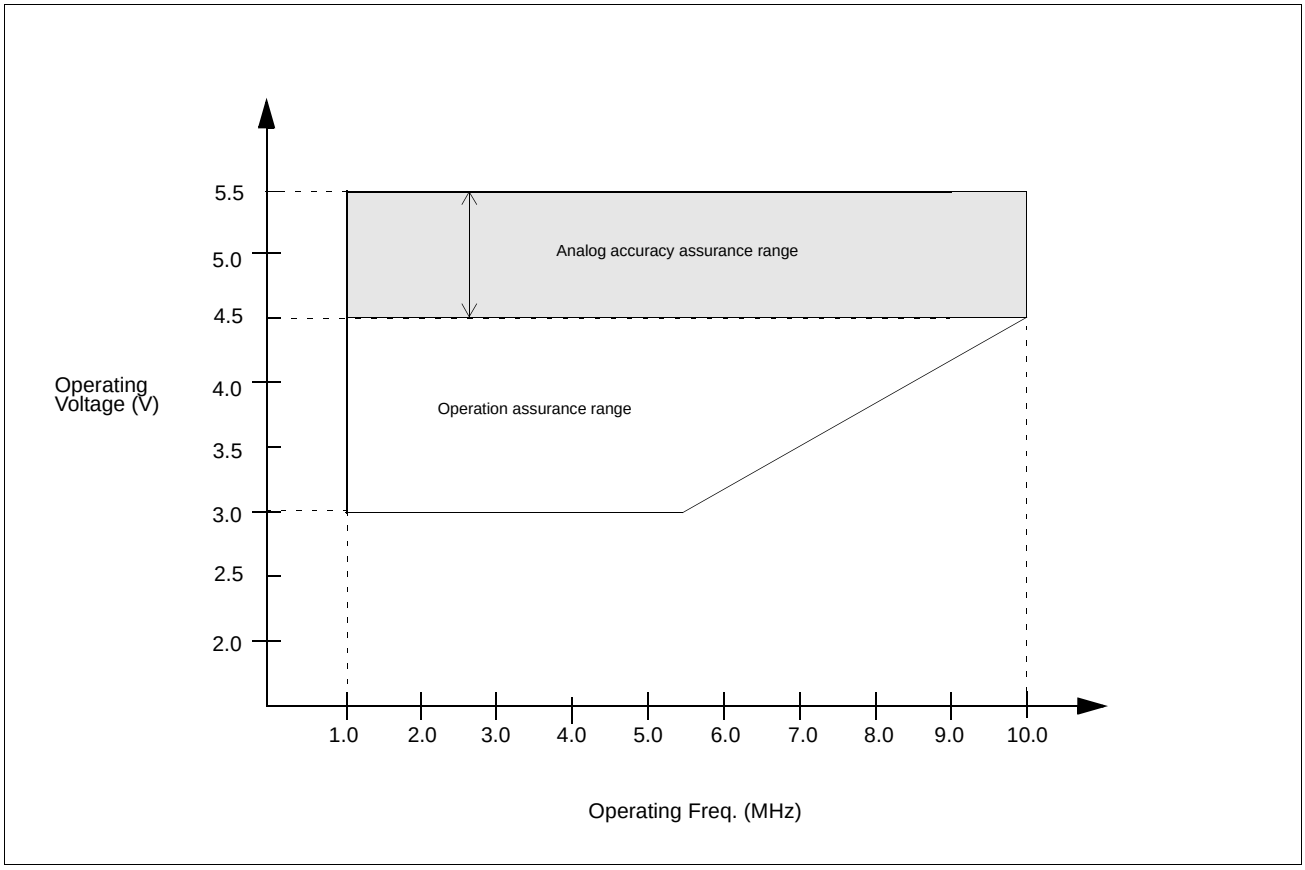


Figure 1 Operating Voltage vs. Operating Frequency

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, F_{CH} = 10 MHz(External clock), T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50, UI/SI	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0/1, UCK/SCK, EC, INT20 ~ INT27, INT10 ~ INT12	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 ~ P07 P30 ~ P37, P40 ~ P43, P50, UI/SI	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0/1, UCK/SCK, EC, INT20 ~ INT27, INT10 ~ INT12	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P40 ~ P43	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50	I_{OH} = –4.0mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 ~ P07, P30 ~ P37, P50, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P40 ~ P43	I_{OL} = 12.0 mA	—	—	0.4	V	
Input leakage current	I_{LI}	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50, MOD0/1	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50	V_I = 0.0V	25	50	100	kΩ	
Power supply current	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 10.0MHz Tinst= 0.4µs Main clock run mode	—	6	9	mA	
	I_{CCS}		F_{CH} = 10.0MHz Tinst= 0.4µs Main clock sleep mode	—	3	5	mA	
	I_{CCH}		Stop mode Ta=+25°C	—	—	10	µA	
	I_A	AV_{cc}	When A/D converting	—	2.3	6	mA	
	I_{AH}		When A/D stops Ta=+25°C	—	—	5	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, V_{CC}, V_{SS}	—	—	10	—	pF	

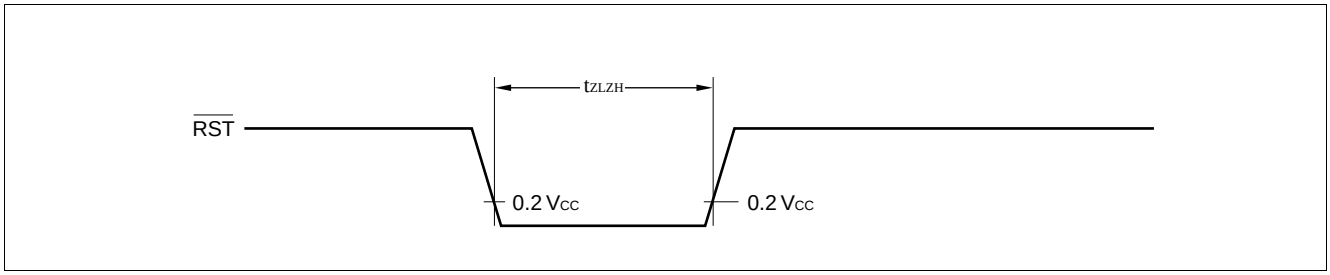
4. AC Characteristics

(1) Reset Timing

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}*	—	ns	

* : t_{HCYL} is the oscillation cycle ($1/F_C$) to input to the X0 pin.

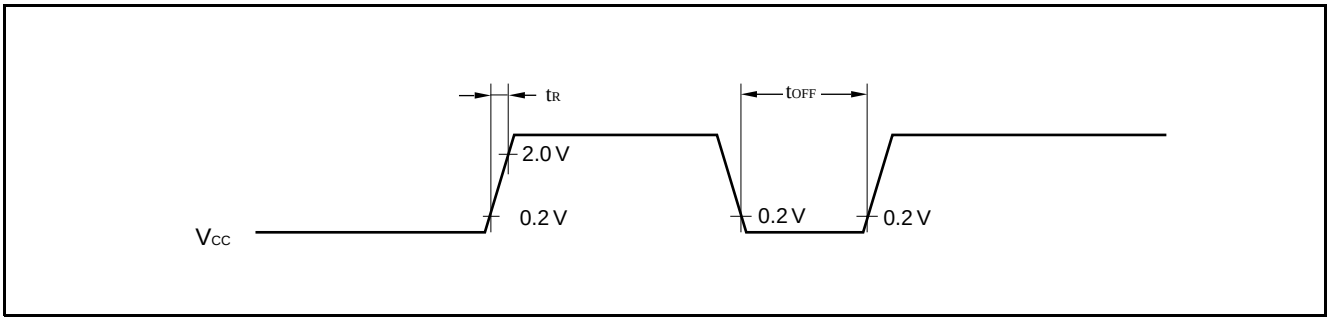


Note: The MCU operation is not guaranteed when the "L" pulse width is shorter than t_{ZLZH}.

(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations



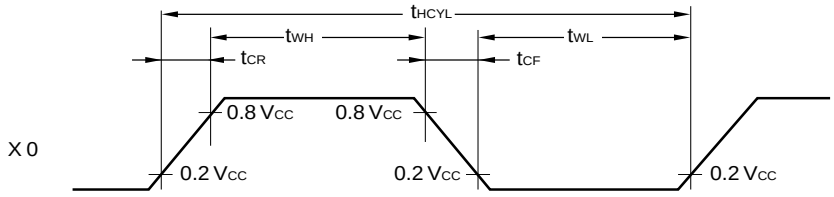
Note: The supply voltage must be set to the minimum value required for operation within the prescribed default oscillation setting time.

(3) Clock Timing

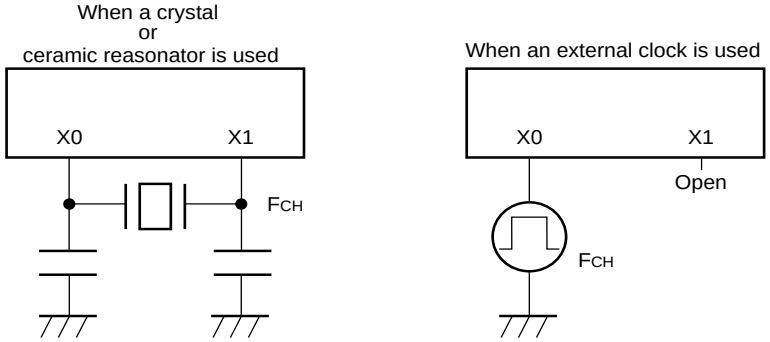
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Clock frequency	F_{CH}	—	1	10	MHz	
Clock cycle time	t_{HCYL}		100	1000	ns	
Input clock pulse width	t_{WH} t_{WL}		20	—	ns	
Input clock rising/falling time	t_{CR} t_{CF}		—	10	ns	

X0 and X1 Timing and Conditions



Main Clock Conditions



(4) Instruction Cycle

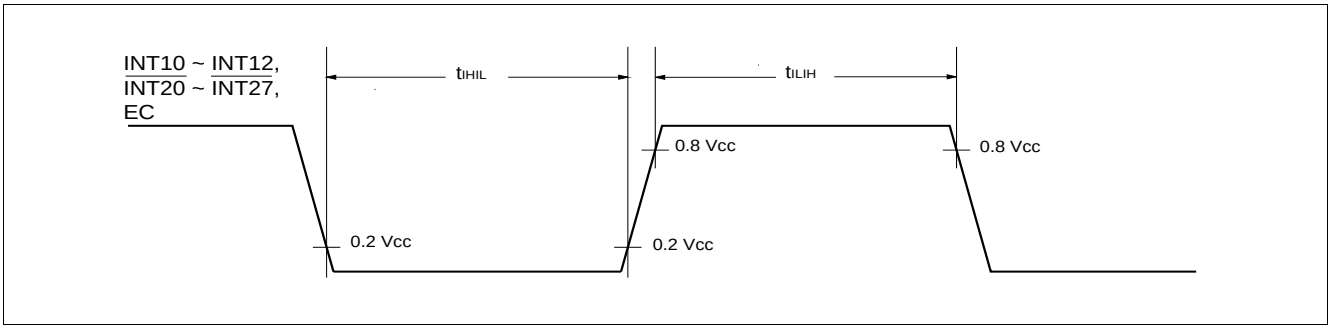
Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	4/F_{CH}, 8/F_{CH}, 16/F_{CH}, 64/F_{CH}	µs	t_{inst} = 0.4 µs when operating at F_{CH} = 10 MHz (4/F_{CH})

(5) Peripheral Input Timing

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width	t_{ILIH}	INT10 ~ INT12, INT20 ~ INT27, EC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width	t_{IHIL}		2 t_{inst}*	—	µs	

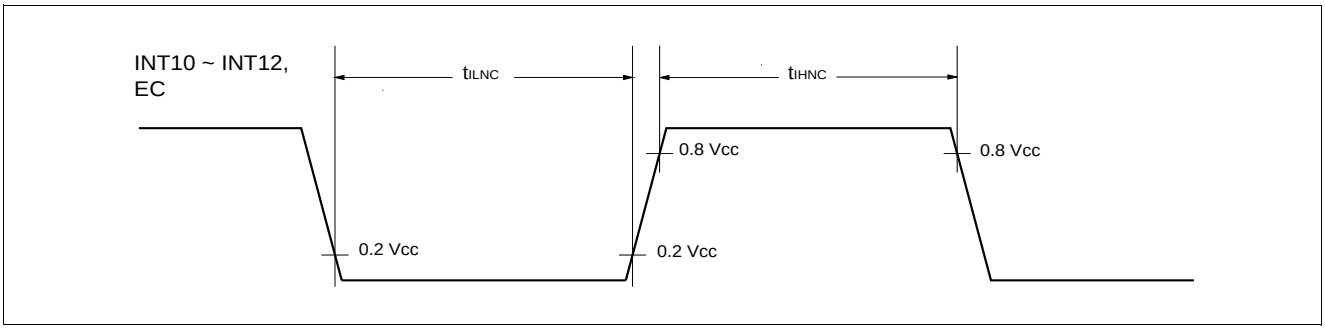
* : For information on t_{inst}, see “(4) Instruction Cycle.”



(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Peripheral input “H” noise limit	t_{IHNC}	INT10 to INT12, EC	7	15	23	ns	
Peripheral input “L” noise limit	t_{ILNC}		7	15	23	ns	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



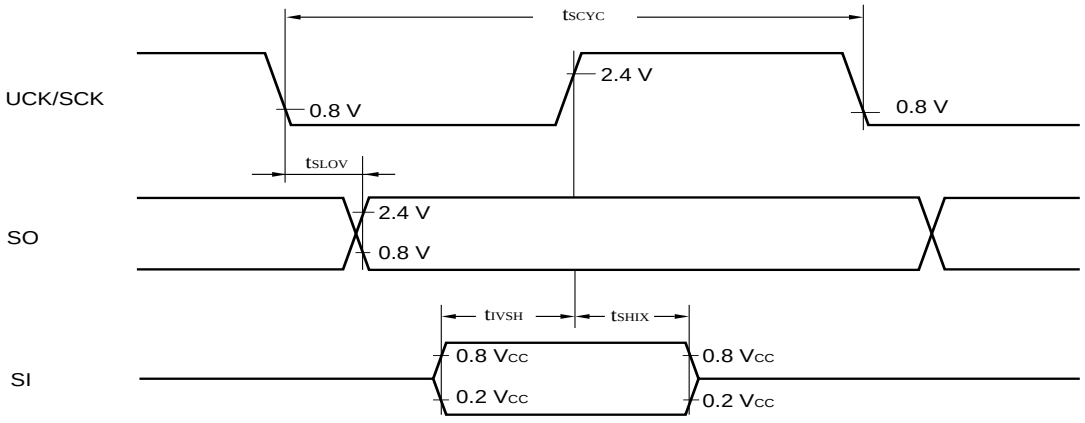
(6) UART, Serial I/O Timing

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

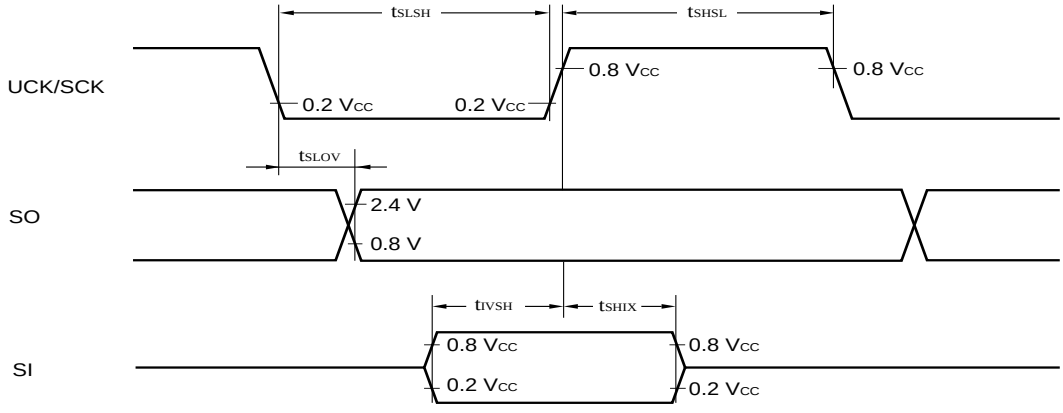
Parameter	Symbol	Pin	Condition	Value		Unit
				Min.	Max.	
Serial clock cycle time	t_{SCYC}	UCK/SCK	Internal shift clock mode	2 t_{inst}*	—	µs
UCK/SCK ↓ → SO time	t_{SLOV}	UCK/SCK, SO		–200	200	ns
Valid SI → UCK/SCK ↑	t_{IVSH}	UCK/SCK, SI		1/2 t_{inst}*	—	µs
UCK/SCK ↑ → valid SI hold time	t_{SHIX}	UCK/SCK, SI		1/2 t_{inst}*	—	µs
Serial clock “H” pulse width	t_{SHSL}	UCK/SCK	External shift clock mode	1 t_{inst}*	—	µs
Serial clock “L” pulse width	t_{SLSH}	UCK/SCK		1 t_{inst}*	—	µs
UCK/SCK ↓ → SO time	t_{SLOV}	UCK/SCK, SO		0	200	ns
Valid SI → UCK/SCK ↑	t_{IVSH}	UCK/SCK, SI		1/2 t_{inst}*	—	µs
UCK/SCK ↑ → valid SI hold time	t_{SHIX}	UCK/SCK, SI		1/2 t_{inst}*	—	µs

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode



5. A/D Converter Electrical Characteristics

(1) A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 5.0$ V ±10%, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

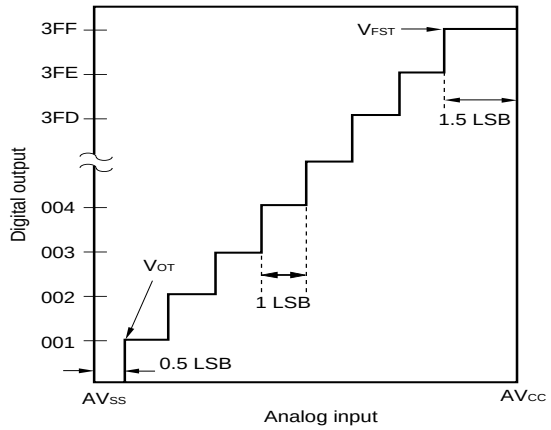
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	—	bit	
Total error			—	—	±3.0	LSB	MB89P935C
					±5.0		MB89PV930A
Linearity error			—	—	±2.5	LSB	MB89P935C
					±3.0		MB89PV930A
Differential linearity error			—	—	±1.9	LSB	MB89P935C
					±2.5		MB89PV930A
Zero transition voltage	V_{OT}		AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	LSB	MB89P935C
			AV_{SS} – 3.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 4.5 LSB		MB89PV930A
Full-scale transition voltage	V_{FST}		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	LSB	MB89P935C
			AVR – 6.5 LSB	AVR – 1.5 LSB	AVR + 2.0 LSB		MB89PV930A
A/D mode conversion time			—	—	38 tinst*	µs	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}		AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 3.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		—	140	260	µA	At A/D start
	I_{RH}		—	—	5	µA	At A/D stop

* For information on t_{inst}, see "(4) Instruction Cycle" in "4. AC Characteristics."

(2) A/D Converter Glossary

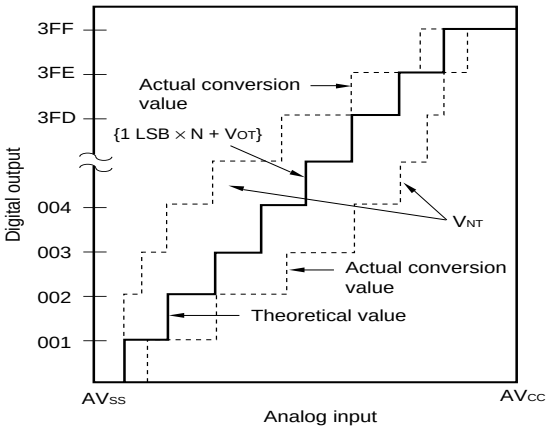
- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1111" ↔ "11 1111 1110") from actual conversion characteristics.
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values.

Theoretical I/O characteristics



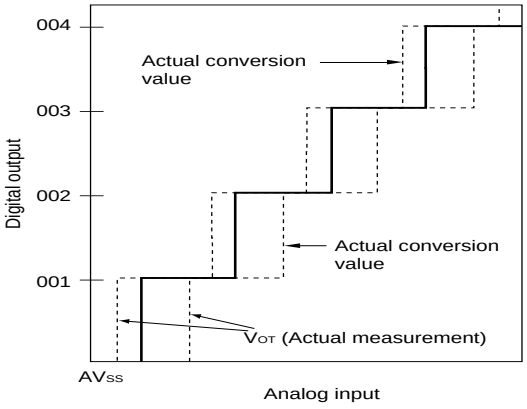
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

Total error

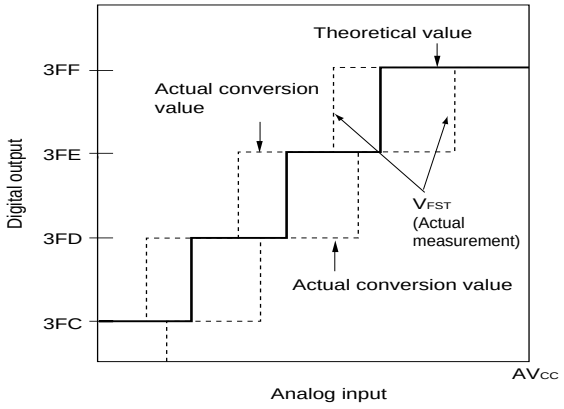


$$\text{Total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

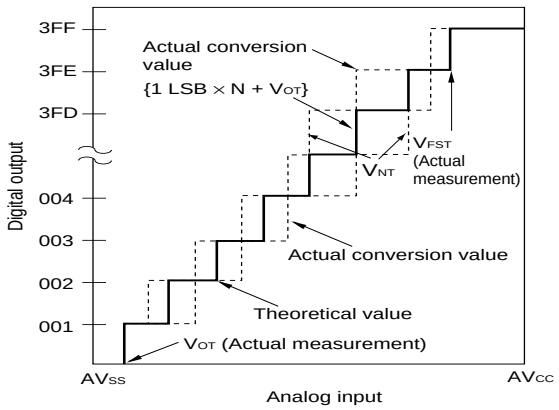
Zero transition error



Full-scale transition error

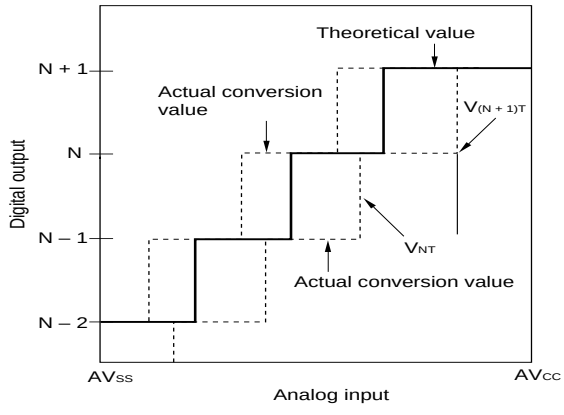


Linearity error



$$\text{Linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

Differential linearity error



$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

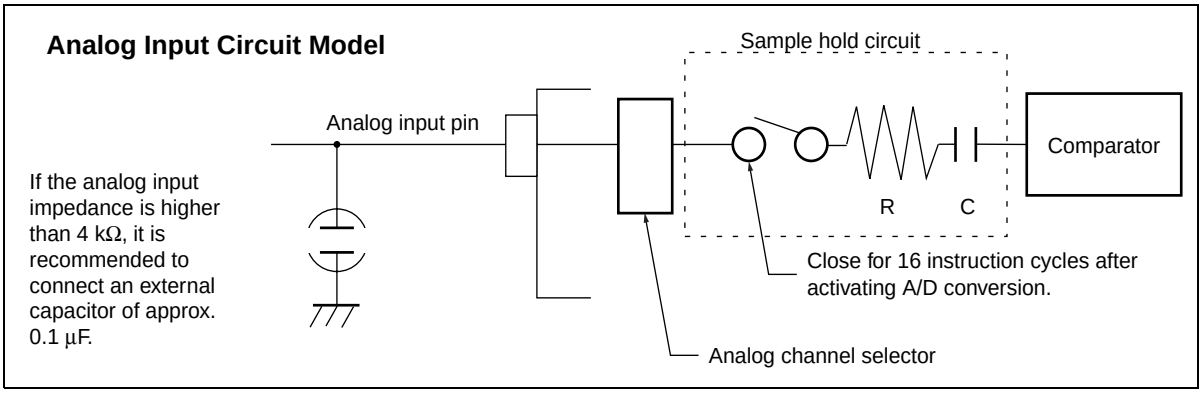
(3) Notes on Using A/D Converter

- Input impedance of the analog input pins
  The A/D converter used for the MB89930C series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for 16 instruction cycles after activation A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 4kΩ).

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.

Analog Input Circuit Model



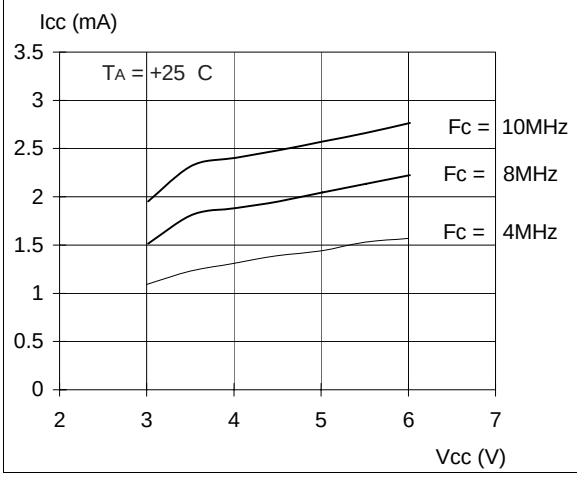
- Error
  The smaller the |AVR - AV_{SS}|, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

- Power Supply Current (External Clock)

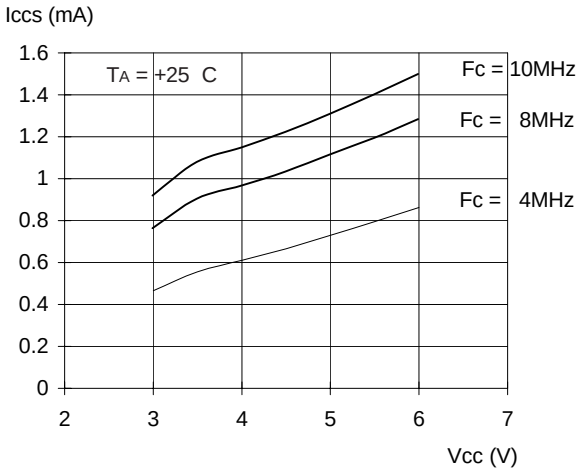
MB89P935A
At The Main Clock Operation
(Highest Clock Gear)

Icc vs. Vcc



MB89P935A
At The Main Sleep Operation
(Highest Clock Gear)

Iccs vs. Vcc



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

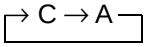
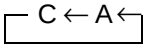
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 1

Table 1 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 1

Table 1 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

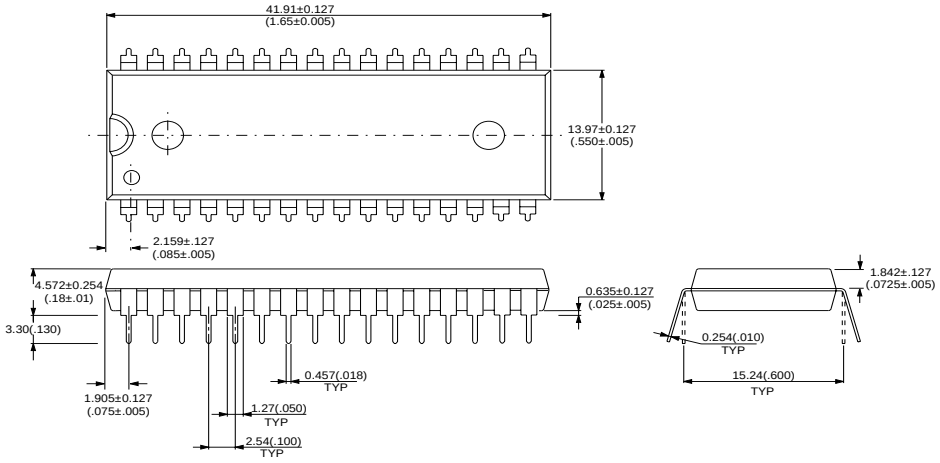
L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89P935CP	32-pin Plastic DIP (DIP-32P-M04)	
MB89P935CP-G-SH	32-pin Plastic SH-DIP (DIP-32P-M05)	
MB89PV930ACF	48-pin Ceramic MQFP (MQP-48C-P01)	

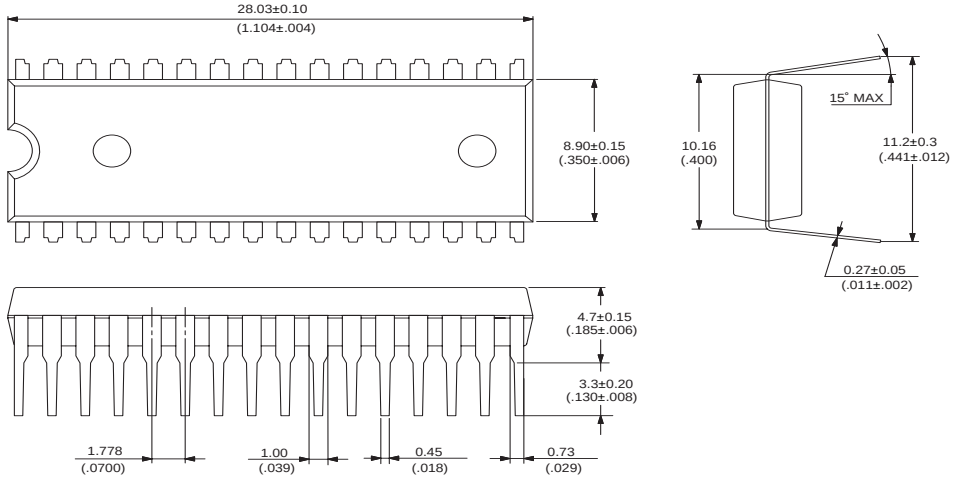
■ PACKAGE DIMENSIONS

32-pin Plastic DIP
DIP-32P-M04



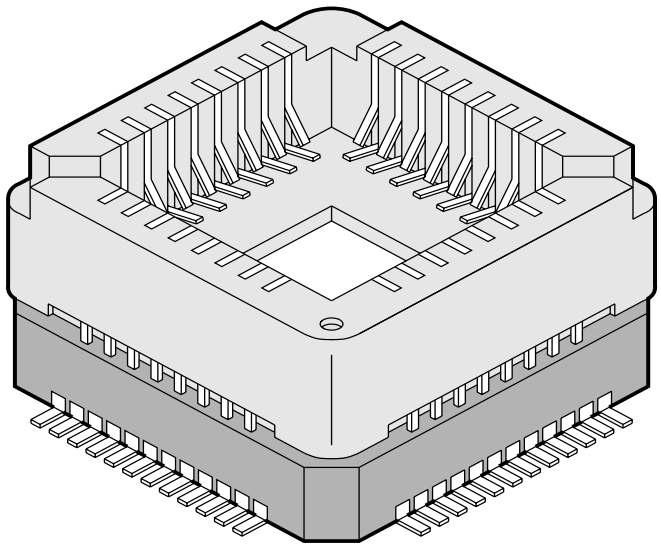
Dimensions in mm (inches)

32-pin Plastic SH-DIP
DIP-32P-M05



Dimensions in mm (inches)

48-pin Ceramic MQFP
MQP-48C-P01



(MQP-48C-P01)

Dimensions in mm (inches)

MEMO

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