SIEMENS

Multichannel Network Interface Controller for HDLC with Extensions MUNICH32X

PEB 20321 Version 2.2

Delta Sheet 06.98

This Delta Sheet describes the differences between MUNICH32X Version 2.2 and MUNICH32X V1.2 (Data Sheet 05.97).

Revision History: Previous Version:
Major Changes:

1 External Bus Modes

1.1 De-multiplexed Bus Modes

The Address Latch Enable (LALE) signal is used to mark the address phase in ***Multiplexed Bus Modes*** and triggers external latches to capture the current address with its falling edge. After a period of time the address is removed and data transfer cycle starts.

Although this signal was generated by MUNICH32X Version 1.x independent of the selected bus mode it is obsolete and thus **not supported by MUNICH32X V2.2 in De-multiplexed Bus Mode**.

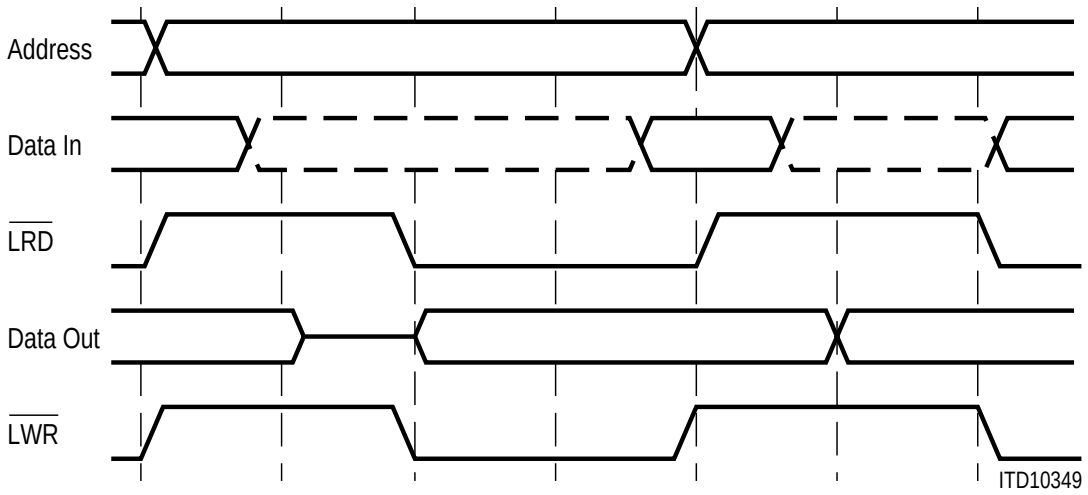

Figure 52

De-multiplexed Bus Cycle

Signal LALE is deleted from figure 52 describing the de-multiplexed bus cycle.

2 TMA Mode

In case of using subchanneling by fill masks the MUNICH32X supports two different modes of operation in Transparent Mode A (TMA). These modes are selected by bit 'CRC' in the channel configuration.

CRC = '0':

Data is transmitted transparently only in bit positions selected by the transmit fill mask (corresponding fill mask bit equal '1'). Masked bit positions are driven Tristate 'Z'.

In receive direction bits are received from bit positions selected by the receive fill mask (corresponding fill mask bit equal '1') only. Receive data is grouped to octets and stored in memory transparently (no gaps).

CRC = '1':

In transmit direction each data octet is masked with the transmit fill mask. Masked bit positions are overwritten with Tristate 'Z' when transmitted.

In receive direction the receive fill mask has to be set to 0xFF. The entire 8 bit time slot is received and stored byte aligned in memory. It is the software responsibility to mask received data octets as needed by the application.

3 Device ID

The Device ID has changed in the PCI Configuration Space and the boundary scan pattern as follows:

The Value of bit field "Revision ID" in the PCI Configuration Space has changed to 13_H.

Table 14

PCI Configuration Space Registers

Register Name	Short Name	Access (Read/ Write)	Absolute Address	Reset Value
...				
Class Code / **Revision ID V2.2**	CC / **RID**	R	08_H	028000/**13**$_H$
...				

Table 29
Boundary Scan Sequence in MUNICH32X V2.2

TDI →

Pin No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
1	LD15	I/O	3	**001**
2	LD14	I/O	3	**1**00
3	LD13	I/O	3	000
4	LD12	I/O	3	000
5	LD11	I/O	3	001
6	LD10	I/O	3	111
7	LD9	I/O	3	000
...	...	...	...	...

→ TDO

IDCODE: A 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to '1'.

TDI →	**0011**	0000 0000 0011 1100	0000 1000 001	1	→ TDO

Note: Since in test logic reset state the code '011' is automatically loaded into the instruction register, the ID code can easily be read out in shift DR state which is reached by TMS = 0, 1, 0, 0.

4 Pin Description

Pin 10 and Pin 61 are labled as 'N.C.1' and 'N.C.2'. Due to the Pull-Up recommendation in the Data Sheet 01/98 these pins should be treated and labled as '*Reserved*' and connected as recommended.

5 Frequency Ratio

The PCM mode 8.192 MHz is limited to a system (PCI) frequency >=25 MHz.

The serial core may fail on serial transmission and serial receive if operated below this frequency in 8.192 MHz mode.