

Description

The function of this low reset Type IC is to accurately reset systems after detecting the supply voltage at the time of switching power on and instantaneous power off in various CPU and other logic system. Further, this IC, with its super low consumption current is most suited as a voltage check circuit for a number of products which use batteries.

Features

- Super low current consumption ($I_{CCL} = 1.0\mu A$ Typ.)
- High current of output transistor ($I_{OL} = 20mA$ Typ.)
- Hysteresis circuit built in ($\Delta V_S = 100mV$ Typ.)
- It has on delay function to supplement the constant of outer C and R.

Applications

- Reset circuits for microcomputers, CPU and MPU.
- Reset circuit for logic circuitry.
- Battery voltage check circuit.
- Circuit for changing over to backup battery.
- Level detecting circuit.

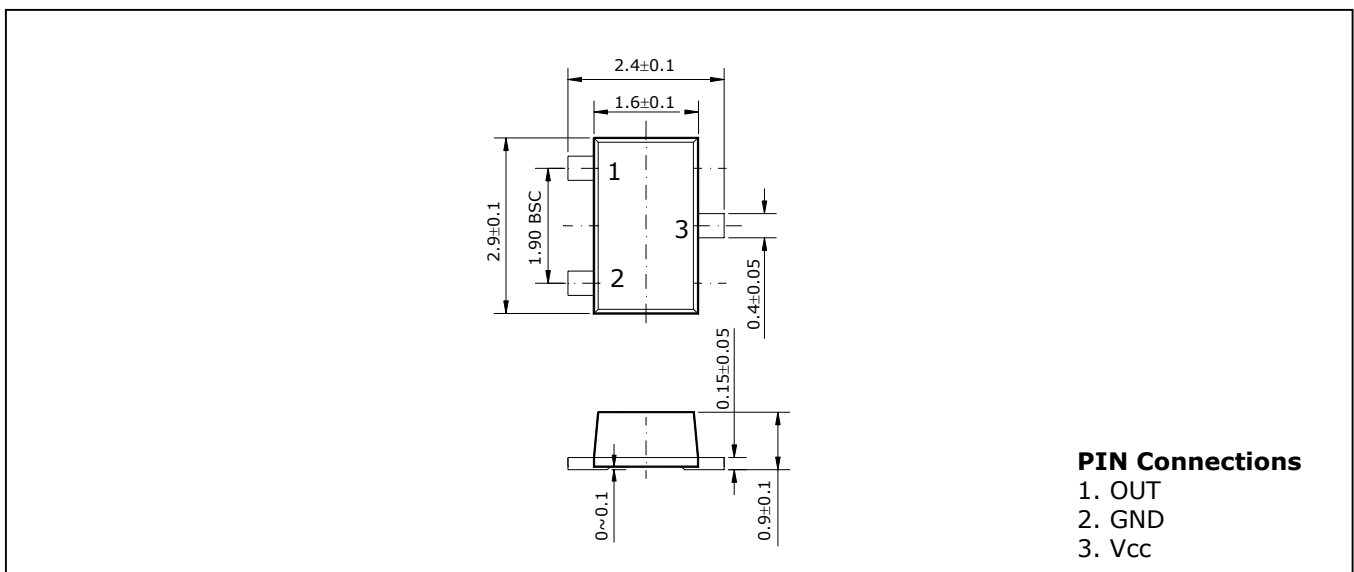
Ordering Information

| Type NO. | Marking | Package Code |
|----------|---------|--------------|
| S72NxxSF | N□□ | SOT-23F |

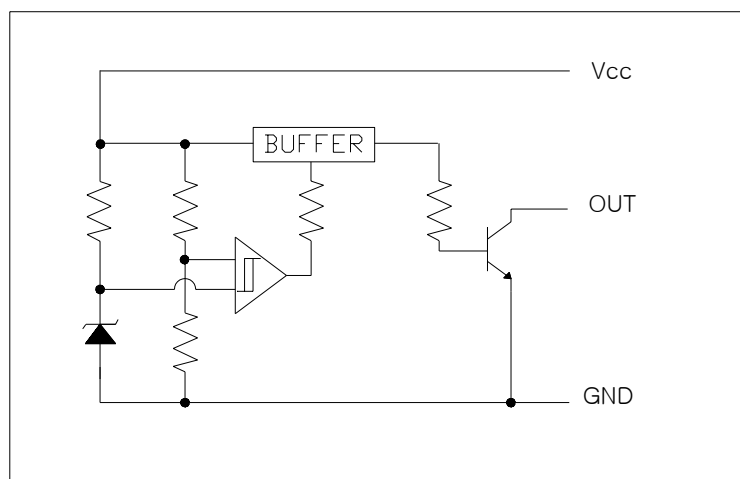
□□: Detecting Voltage Code

Outline Dimensions

Unit : mm



Equivalent Circuit Diagram



Maximum ratings

(Ta=25°C)

| Characteristic | Symbol | Ratings | Unit |
|--|--------|------------|------|
| Supply voltage | Vcc | -0.3 ~ +10 | V |
| Power Dissipation (Package Limitation) | PD * | 300 | mW |
| Operating Temperature | Topr | -20 ~ +75 | °C |
| Storage Temperature | Tstg | -40 ~ +125 | °C |

* With PCB(8×8 mm Copper Area) at Glass Epoxy Board (t=1.7 mm, Area; 20×20 mm)

Electrical Characteristics

(Vcc=5V, Ta=25°C)

| Characteristic | Symbol | Test Circuit | Test Condition | Min. | Typ. | Max. | Unit |
|--|--------|--------------|----------------------------------|------|--------|------|------|
| Detecting Voltage | VS | 1 | * See Table 1 | | | | |
| Hysteresis Voltage | Δ VS | 1 | RL=470Ω, VCC=L→H→L | 40 | 100 | 300 | mV |
| Temperature Coefficient Of detecting voltage | VS/Δ T | 1 | RL=470Ω, Ta= -20~75°C | - | ± 0.01 | - | %/°C |
| Low Level Output voltage | VOL | 1 | RL=470Ω, VCC= VS Min | - | 0.1 | 0.4 | V |
| Circuit current at ON | ICCL | 1 | RL=∞ Ω, VCC= VS Min | - | 100 | 180 | μA |
| Circuit current at OFF | ICCH | 1 | RL=∞ Ω, VCC=VS Max +0.1V | - | 1.0 | 2.5 | μA |
| Threshold Operating Voltage | Vopr | 1 | RL=4.7 kΩ, VOL ≤ 0.4V | - | 1.4 | 1.6 | V |
| Output Current at ON I | IOL 1 | 1 | RL=0Ω, VCC= VS Min | 10 | 20 | - | mA |
| Output Current at ON II | IOL 2 | 1 | RL=0Ω, VCC= VS Min, Ta= -20~75°C | 5 | - | - | mA |
| L→H Transmission delay time | tPLH | 2 | RL=4.7 kΩ, CL=100 pF | - | 100 | 500 | μs |
| H→L Transmission delay time | tPHL | 2 | RL=4.7 kΩ, CL=100 pF | - | 10 | 20 | μs |

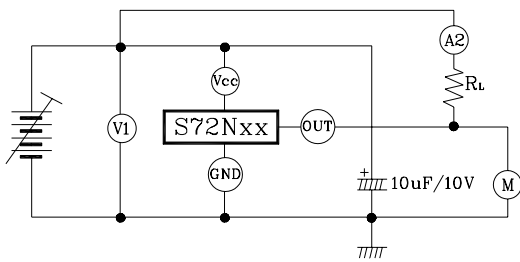
*** Table 1**

Electrical Characteristics

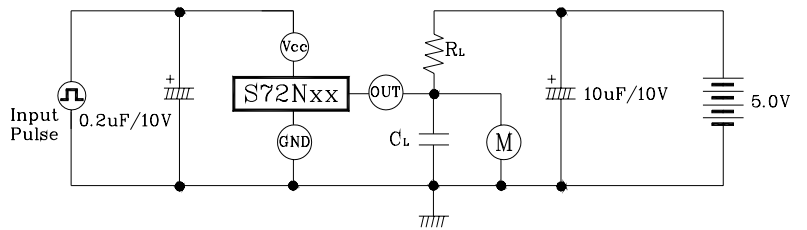
(V_{cc}=5V, T_a=25°C)

| Characteristic | Symbol | Test Circuit | Test Condition | Min. | Typ. | Max. | Unit | |
|-------------------|--------|--------------|----------------------------------|----------|------|------|------|---|
| Detecting voltage | VS | 1 | RL=470Ω VCC=H→L VOL ≤ 0.4V | S72N45SF | 4.30 | 4.5 | 4.70 | V |
| | | | | S72N42SF | 4.00 | 4.2 | 4.40 | |
| | | | | S72N39SF | 3.70 | 3.9 | 4.10 | |
| | | | | S72N36SF | 3.40 | 3.6 | 3.80 | |
| | | | | S72N33SF | 3.10 | 3.3 | 3.50 | |
| | | | | S72N31SF | 2.90 | 3.1 | 3.30 | |
| | | | | S72N29SF | 2.75 | 2.9 | 3.05 | |
| | | | | S72N27SF | 2.55 | 2.7 | 2.85 | |
| | | | | S72N25SF | 2.35 | 2.5 | 2.65 | |
| | | | | S72N23SF | 2.15 | 2.3 | 2.45 | |

Test Circuit 1

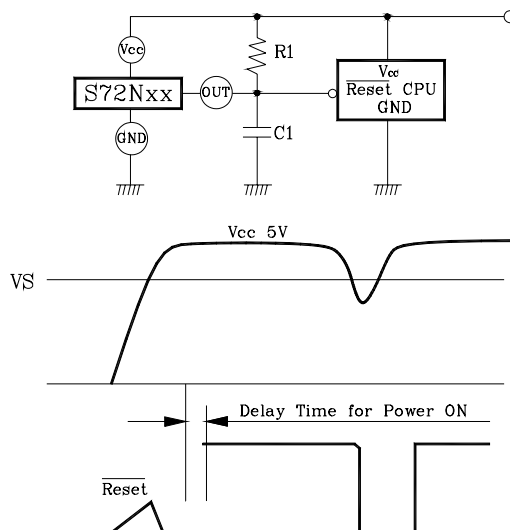
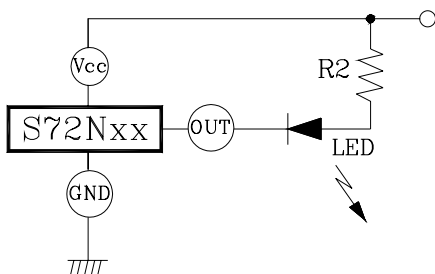


Test Circuit 2



Application Circuit

(1) Battery Low Indicator



(Note)

- (1) Connecting of LED and R2 obtains a voltage drop indicator.
- (2) Connecting of C1 and selection of time constant with C1 and R1 set the power on delay time.

Electrical Characteristic Curves

Fig. 1 $V_O - V_{CC}$

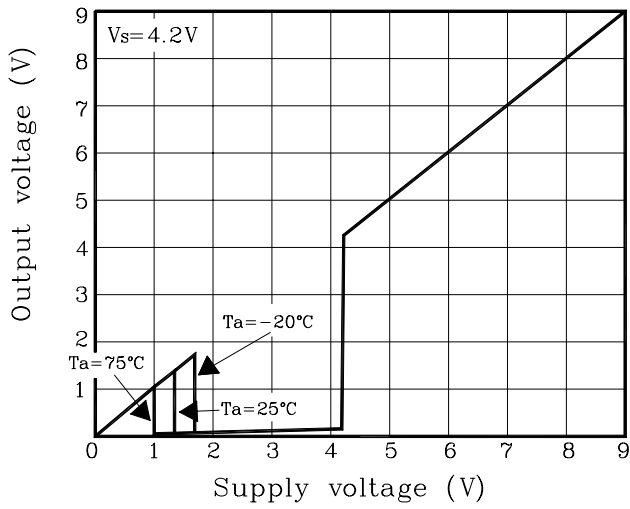


Fig. 2 $I_{CC} - V_{CC}$

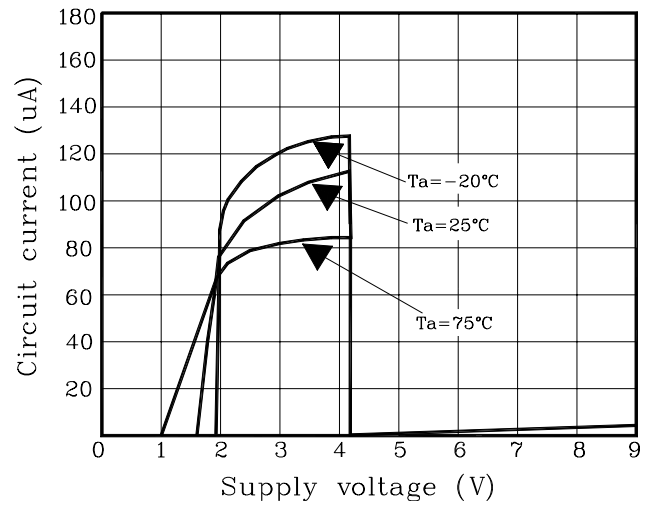


Fig. 3 $\Delta V_S - T_a$

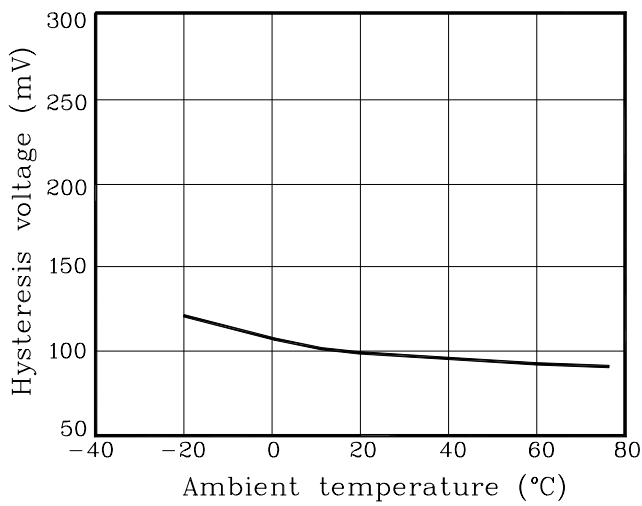


Fig. 4 $V_S - T_a$

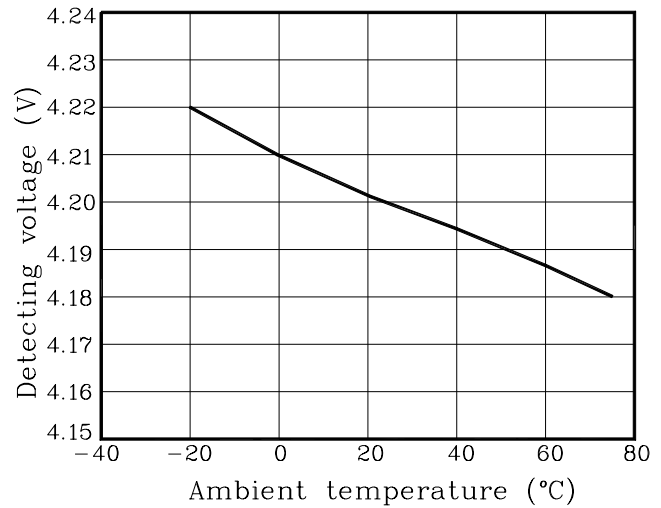


Fig. 5 $I_{CCL} - T_a$

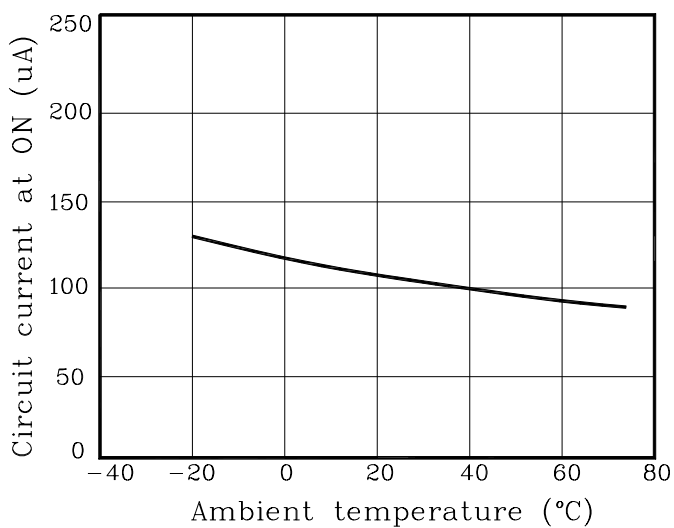


Fig. 6 $V_{OL} - T_a$

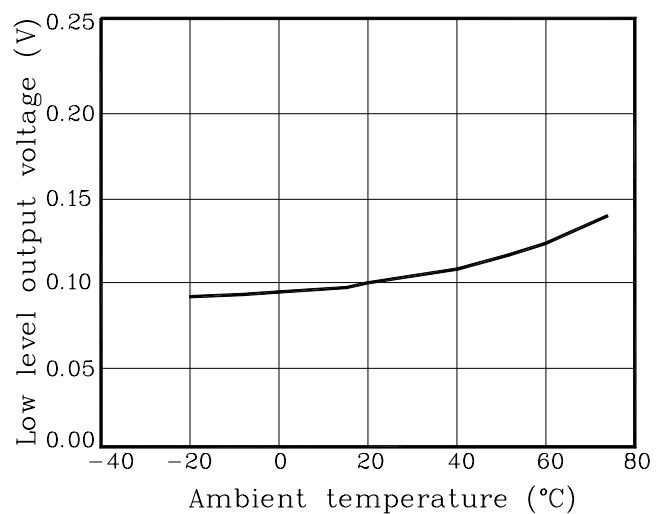


Fig. 7 $I_{OL} - T_a$

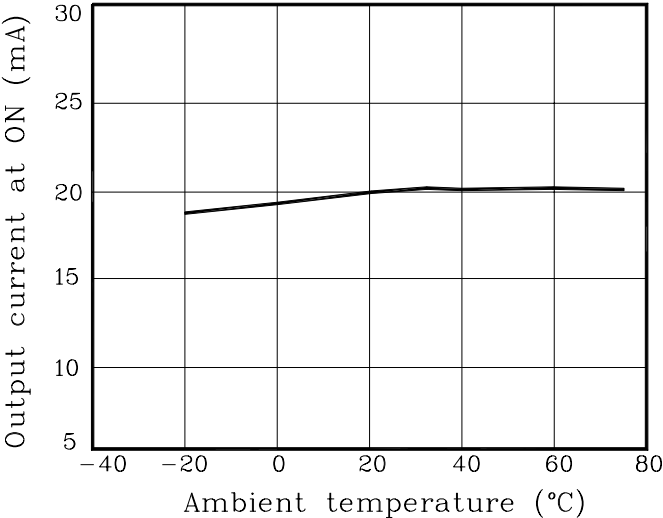


Fig. 8 $I_{CCH} - T_a$

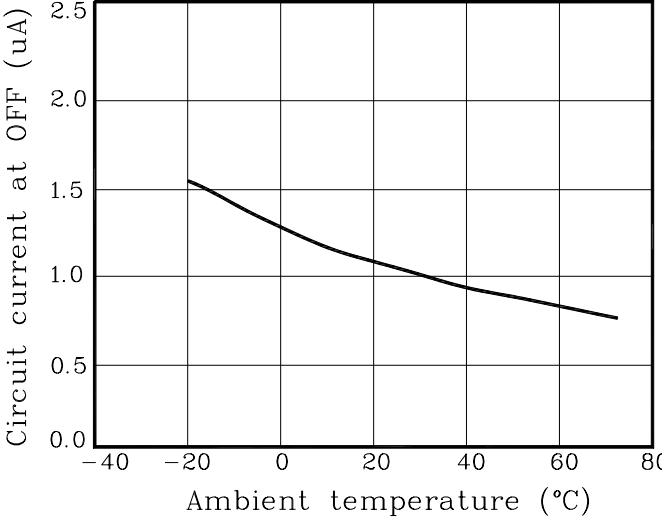
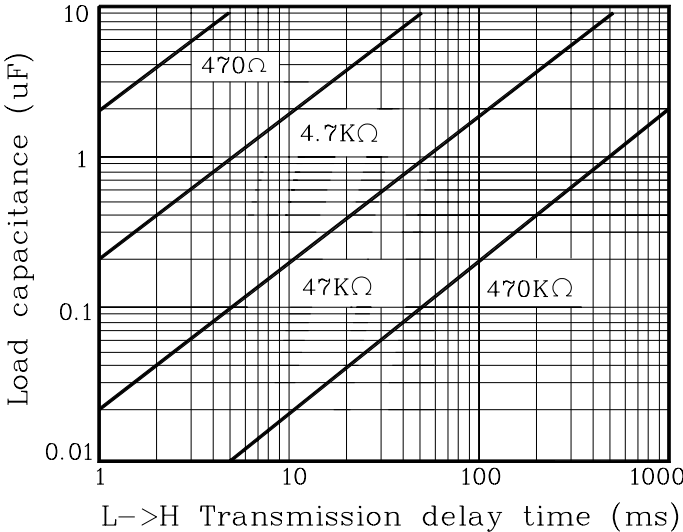


Fig. 9 $C_L - t_{PLH}$



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