Features

- **Single-chip Synthesizer + Effects, Typical Applications Include:**
  - **Wavetable Synthesis, Serial MIDI-In and -Out, MPU-401 (UART)**
  - **Effects: Reverb + Chorus on MIDI and/or Audio-in**
  - **Surround on Two or Four Speakers with Intensity/Delay Control**
  - **Four-band Parametric Equalizer**
  - **Audio-in Processing through Reverb, Chorus, Equalizer, Surround**
  - **Independent Microphone Echo Function for Karaoke**
- **High-quality Wavetable Synthesis**
  - **16-bit Samples, 44.1 kHz Sampling Rate, 24 dB Digital Filter per Voice**
  - **Up to 64-voice Polyphony**
- **High Performance**
  - **RISC Structure for Sound Synthesis/Processing**
  - **CISC Structure for MIDI/MPU-401 Communication and Housekeeping**
- **Available Wavetable Firmwares and Sample Sets**
  - **CleanWave8® Low-cost General MIDI(GM) 1 MB Firmware + Sample Set**
  - **CleanWave32® Top-quality 4 MB Firmware + Sample Set**
  - **Other Sample Sets Available Under Special Conditions**
- **Compatible**
  - **Firmware and Sounds Compatible with SAM9407/SAM9503**
  - **New Applications Can be Developed Using Dream® SAM9407 Standard Development Tools**
- **Low Voltage, Low Power**
  - **Single Low-frequency Crystal Operation and Built-in PLL Minimize RFI**
  - **I/O from 3V to 5.5V, Core 3.3V ± 10%**
  - **Power-down Mode**
- **Low Cost**
  - **Industry-standard 100-lead PQFP Package**
- **Typical Applications**
  - **PC Sound Cards with the Best Quality/Price Ratio**
  - **Computer Karaokes, Portable Karaokes**
  - **Keyboards, Portable Keyboard Instruments**

Description

The SAM9733 is a low-cost derivative of the SAM9407 and SAM9503. It retains the same high-quality synthesis with polyphony up to 64 voices. The SAM9733 maximum wavetable memory is 4 MB and the ISA bus communication is through a standard MPU-401. The SAM9733 is delivered in an industry-standard 100-lead plastic quad flat pack package (PQFP100).

The highly-integrated architecture of the SAM9733 combines a specialized high-performance RISC-based digital signal processor (Synthesis/DSP) and a general-purpose 16-bit CISC-based control processor on a single chip. An on-chip memory management unit (MMU) allows the synthesis/DSP and the control processor to share external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the ISA PC bus, the on-chip MIDI UART, and the Codec control interface, with minimum intervention from the control processor.

Integrated Synthesizer with Effects

SAM9733

Rev. 1714A–03/01

Typical Designs

Figure 1. PC Multimedia

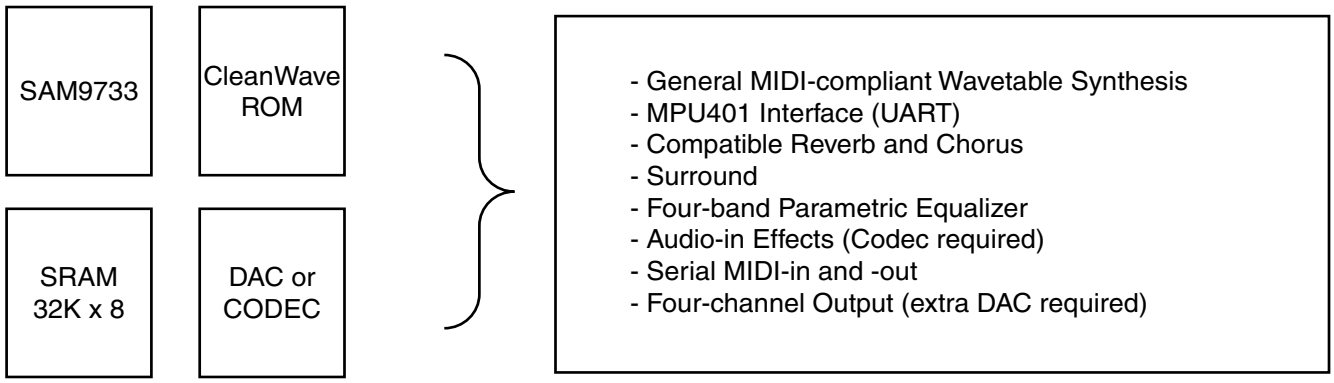


Figure 2. Low-cost Karaoke, Hand-held Karaoke

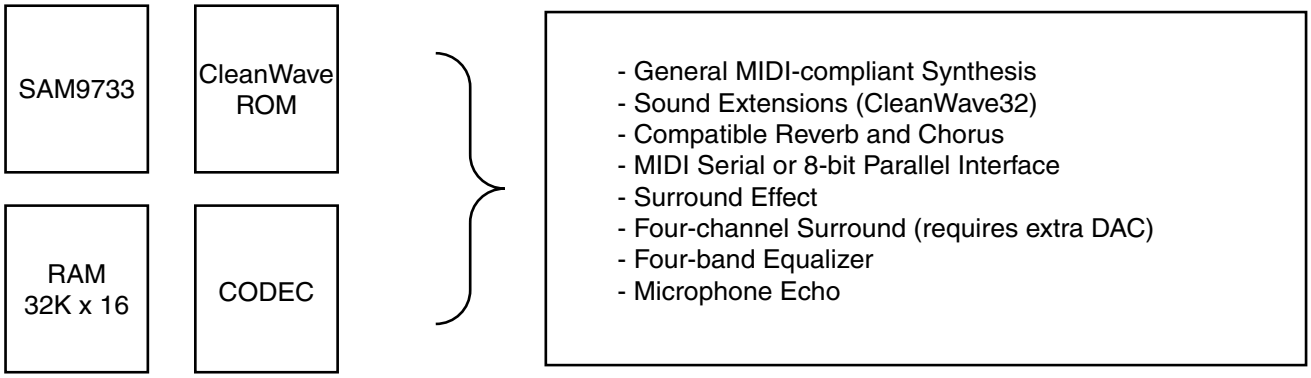
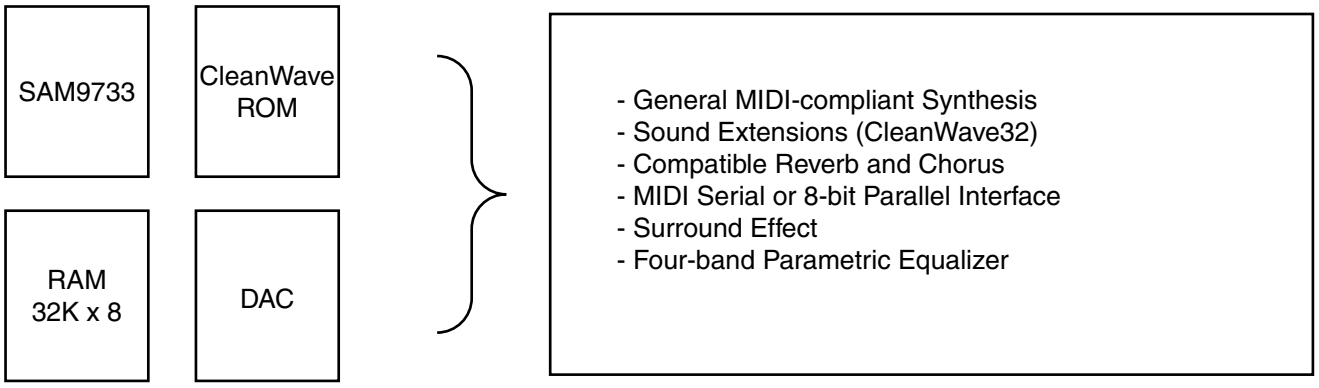
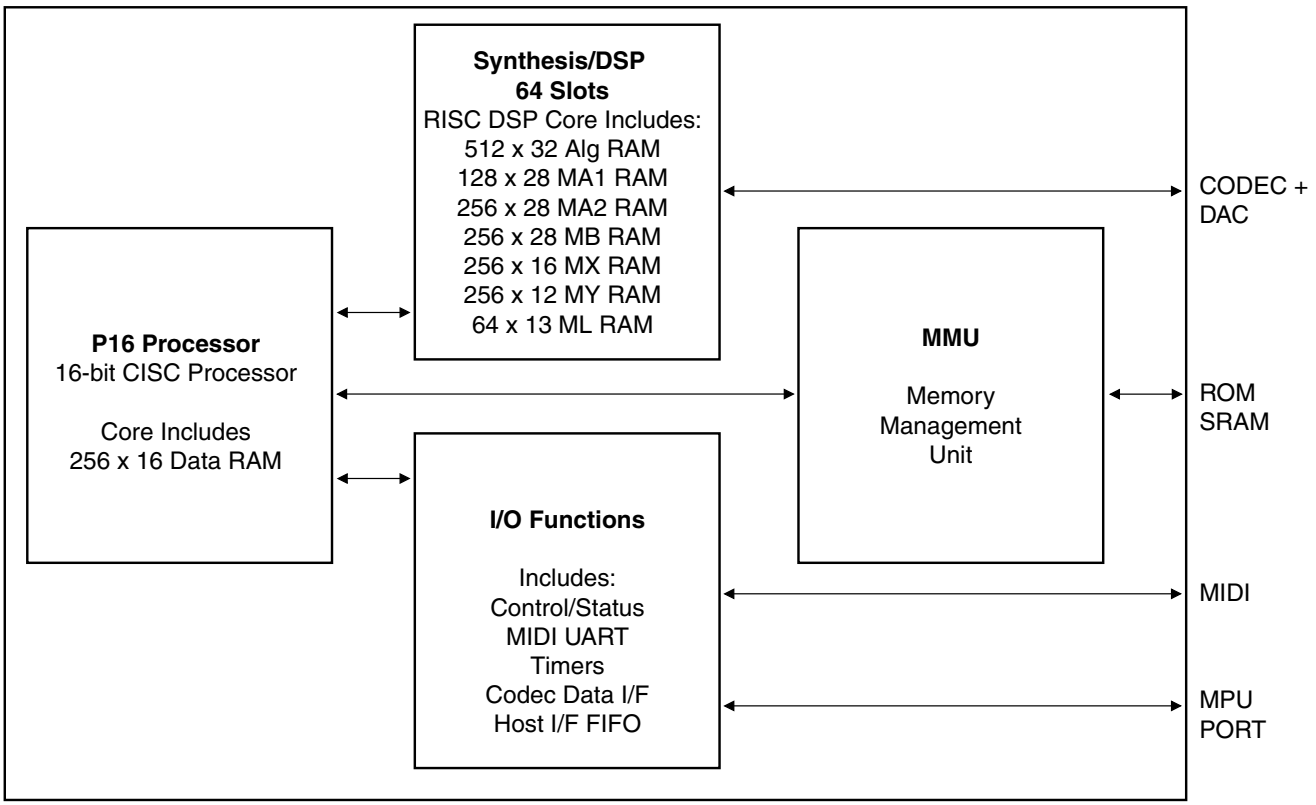


Figure 3. Low-cost Keyboard Instrument



General Description

Figure 4. IC Architecture



Synthesis/DSP Engine

The synthesis/DSP engine operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is divided into 16 micro-instructions known as algorithms. Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24 dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical application will use half the capacity of the synthesis/DSP engine for synthesis, thus providing state-of-the-art 32-voice wavetable polyphony. The remaining processing power will be used for typical functions such as reverberation, chorus, audio-in processing, surround effect, equalizer, etc.

Frequently-accessed synthesis/DSP parameter data are stored in five banks of on-chip RAM memory. Sample data or delay lines that are accessed relatively infrequently are stored in external ROM or SRAM memory. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS). Separate buses from each of the on-chip parameter RAM memory banks allow highly-parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to six simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 300 million operations per second (MOPS).

P16 Control Processor and I/O Functions

The P16 control processor is a general-purpose 16-bit CISC processor core that runs from external memory. It includes 256 words of local RAM data memory.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the PC ISA interface and then controls the synthesis/DSP by writing into the parameter RAM banks in the DSP core. Slowly-changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the ISA PC interface through specialized “intelligent” peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The ISA PC interface is implemented using one address line (A0), a chip-select signal, read and write strobes from the host, and an 8-bit data bus (D0 - D7).

The data bus can drive the PC bus directly (24 mA buffers). An external plug-and-play IC is required to map the 16-bit I/O addresses and AEN from the PC onto the address line and chip select from the SAM9733.

The ISA PC interface is normally used to implement a MPU-401 UART-mode-compatible interface with address 0 being the data register and address 1 being the status/control registers. Besides the standard two status bits of the MPU-401, two additional bits are provided to expand the MPU-401 protocol.

Karaoke and keyboard applications can take advantage of the 8-bit MPU-401 interface to communicate with the SAM9733 at high speed with the MIDI-IN and MIDI-OUT signals remaining available.

Memory Management Unit (MMU)

The MMU block allows external ROM and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single device (i.e., SRAM) to serve as delay lines for the synthesis/DSP and as data memory for the P16 control processor.

Pin Description

Table 1. Pin by Function

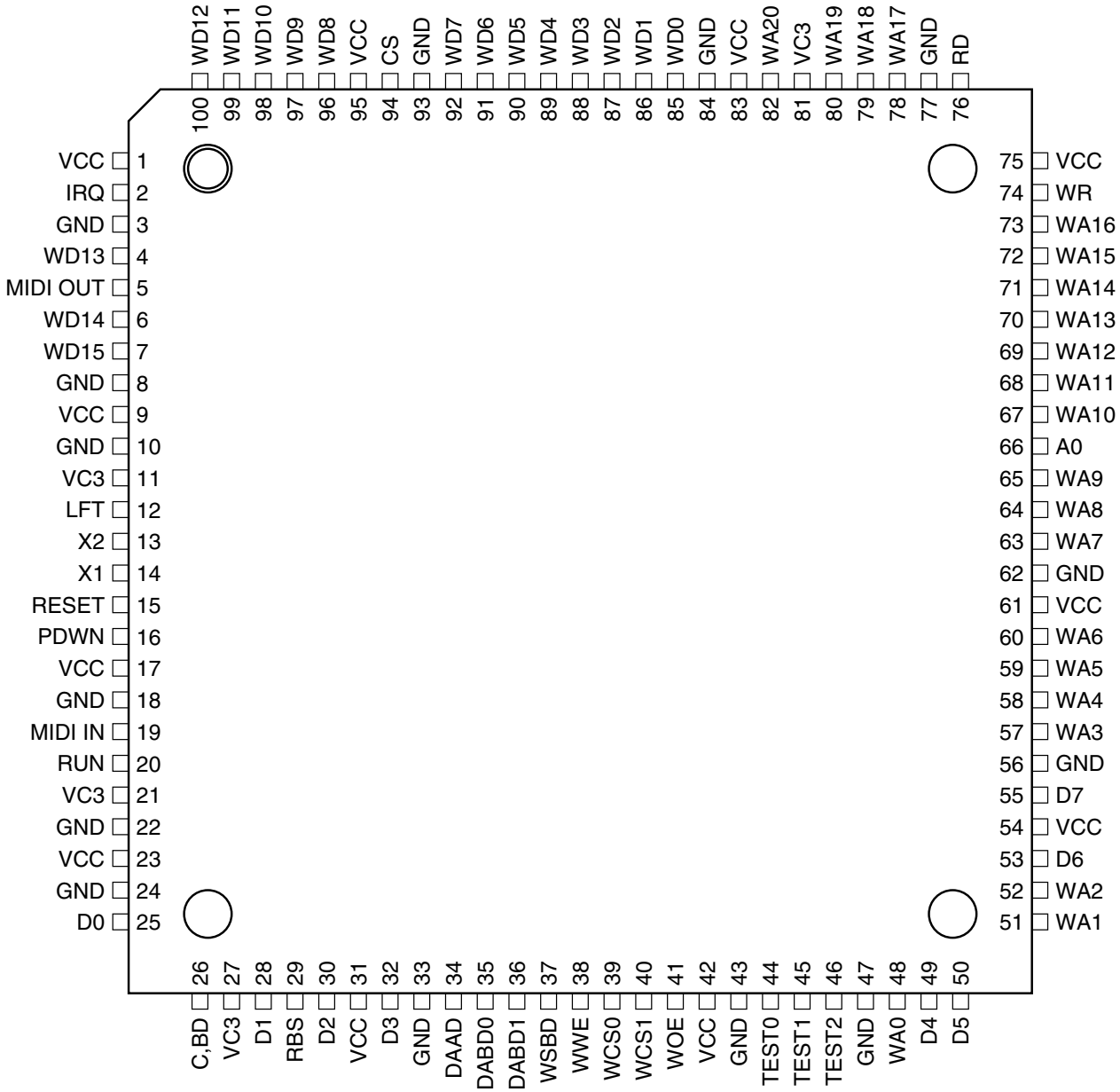
Pin Name	Pin Count	Type	Function
GND	14	PWR	Power Ground. All GND pins should be returned to digital ground.
VC3	4	PWR	Core Power +3.3V ± 10%. All V_{C3} pins should be returned to +3.3V.
VCC	11	PWR	Power +3V to +5.5V. All V_{CC} pins should be returned to +5V (or 3.3V in case of single 3.3V supply).
D0 - D7	8	I/O	8-bit data bus to host processor. Has enough driving power to drive ISA PC bus directly (24 mA buffer). Information on these pins is parallel MIDI (MPU-401 type applications). Direct ISA PC bus drive requires 5V V_{CC}.
$\overline{CS}$	1	IN	Chip select from host, active low.
$\overline{WR}$	1	IN	Write from host, active low.
$\overline{RD}$	1	IN	Read from host, active low.
A0	1	IN	Selects MPU-401 internal registers. 0: data registers (read/write) 1: status register (read) control register (write)
IRQ	1	TSOUT	Tri-state output pin. Can be connected directly to host IRQ line (24 mA).
$\overline{RESET}$	1	IN	Master reset input, active low. Schmitt trigger input.
X1, X2	2		Crystal connection. Crystal frequency should be Fs•256 (typ 11.2896 MHz). Crystal frequency is internally multiplied by four to provide the IC master clock. X1 can also be used as external clock input (3.3V input). X2 cannot be used to drive external ICs.
DABD0 - 1	2	OUT	Two stereo serial audio data outputs (four audio channels). Each output holds 64 bits (2 x 32) of serial data per frame. Audio data has up to 20-bit precision, DABD0 can hold additional control data (mute, A/D gain, D/A gain, etc.).
CLBD	1	OUT	Audio data bit clock, provides timing to DABD0 - 1.
WSBD	1	OUT	Audio data word select. The timing of WSBD can be selected to be I2S or Japanese compatible.
DAAD	1	IN	Stereo serial audio data input.
MIDI IN	1	IN	TTL level MIDI-IN input.
MIDI OUT	1	OUT	TTL level MIDI-OUT output.
WA0 - 20	21	OUT	External memory address (ROM/SRAM). Up to four megabytes of ROM.
WD0 - 15	16	I/O	PCM ROM/SRAM data.
RBS	1	OUT	SRAM byte select. Should be connected to the lower RAM address when an 8-bit wide SRAM is used. The type of RAM (16-bit/8-bit) can be selected by program.
$\overline{WCS0}$	1	OUT	PCM ROM chip select, active low.
$\overline{WCS1}$	1	OUT	SRAM chip select, active low.
$\overline{WWE}$	1	OUT	SRAM write enable, active low.
$\overline{WOE}$	1	OUT	PCM ROM/SRAM output enable, active low.
RUN	1	OUT	High when the synthesis is initialized. Can be used as $\overline{RESET}$ for an external device (Codec).

Table 1. Pin by Function (Continued)

Pin Name	Pin Count	Type	Function
LFT	1	ANA	PLL low-pass filter. Should be connected to an external RC network.
TEST0 - 2	3	IN	Test pins. Should be returned to GND.
$\overline{\text{PDWN}}$	1	IN	Power down, active low.

Pinout

Figure 5. SAM9733 in 100-lead PQFP Package



Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Typ	Max	Unit
	Ambient Temperature (Power applied)	-40		+85	°C
	Storage Temperature	-6.5		+150	°C
	Voltage on any pin (except X1)	-0.5		V_{CC} + 0.5	V
	Voltage on pin X1	-0.5		V_{C3} + 0.5	V
V_{CC}	Supply Voltage	-0.5		6.5	V
V_{C3}	Supply Voltage	-0.5		4.5	V
	Maximum I_{OL} per I/O pin (except D0, D7, IRQ)			10	mA
	Maximum I_{OL} per I/O pin D0, D7, IRQ			30	mA

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter/Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage [1]	3	3.3/5.0	5.5	V
V_{C3}	Supply Voltage	3	3.3	3.6	V
T_A	Operating Ambient Temperature	0		70	°C

Note: 1. D0 - D7 and IRQ can only be connected to PC ISA bus if V_{CC} = 5V ± 10%

DC Characteristics

Figure 6. DC Characteristics (T_A = 25°C, V_{CC} = 3 to 5.5V, V_{C3} = 3.3V ± 10%)

Symbol	Parameter/Condition	VCC	Min	Typ	Max	Unit
V_{IL}	Low-level Input Voltage	3.3 5.0	-0.5 -0.5		1.0 1.7	V V
V_{IH}	High-level Input Voltage	3.3 5.0	2.3 3.3		VCC + 0.5 VCC + 0.5	V V
V_{OL}	Low-level Output Voltage. D<7:0>, IRQ: I_{OL} = -24 mA others except LFT, X2: I_{OL} = -3.2 mA	3.3 5.0			0.45 0.45	V V
V_{OH}	High-level Output Voltage. D<7:0>, IRQ: I_{OH} = 10 mA others except LFT, X2: I_{OH} = 0.8 mA	3.3 5.0	2.8 4.5			V V
I_{CC}	Power Supply Current (Crystal Freq. = 12 MHz)	3.3 5.0		70 25	90 35	mA mA
	Power Down Supply Current			70	100	µA

Timings

All timing conditions: V_{CC} = 5V, V_{C3} = 3.3V, T_A = 25°C, signals D0 - D7 with 220Ω pull-up, 30 pF capacitance, signal IRQ with 470Ω pull-down, 30 pF capacitance, all other outputs except X2 and LFT load capacitance = 30 pF.

All timings refer to tck, the internal master clock period.

The internal master clock frequency is four times the frequency at pin X1. Therefore tck = $t_{XTAL}/4$.

The sampling rate is given by 1/(tck•1024). The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 kHz sampling rate).

Crystal Frequency Selection Consideration

There is a trade-off between the crystal frequency and the support of widely-available external ROM components. Table 4 gives information on selecting the best fit for a given application.

Table 4. Crystal Frequency Selection Consideration

Sample Rate (k\Hz)	XTAL (MHz)	tck (ns)	ROM t_A (ns)	Comment
48	12.288	20.35	92	Maximum Frequency
44.1	11.2896	22.14	101	Recommended for Current Designs
37.5	9.60	26.04	120	
31.25	8.00	31.25	146	

Using 11.2896 MHz crystal frequency allows the use of widely-available ROMs with 100 ns access time while providing state-of-the-art 44.1 kHz sampling rate.

PC Host Interface

Figure 7. Host Interface Read Cycle

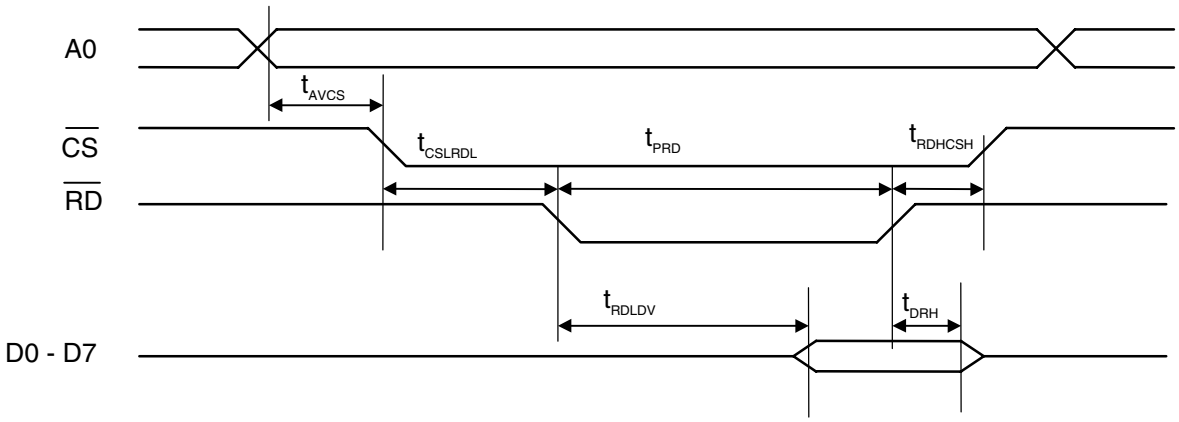


Figure 8. Host Interface Write Cycle

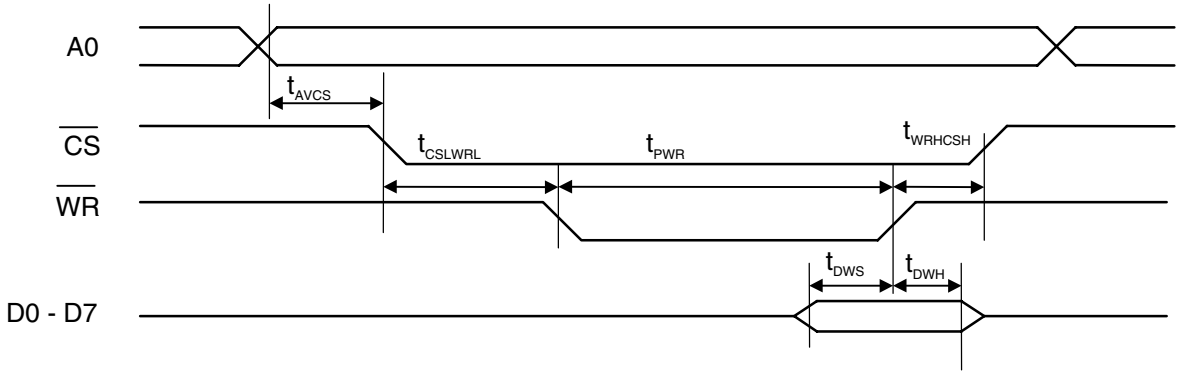


Table 5. Timing Parameters

	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address Valid to Chip Select Low	0			ns
t_{CSLRDL}	Chip Select Low to $\overline{RD}$ Low	5			ns
t_{RDHCSH}	$\overline{RD}$ High to $\overline{CS}$ High	5			ns
t_{PRD}	$\overline{RD}$ Pulse Width	50			ns
t_{RDLDV}	Data Out Valid from $\overline{RD}$			20	ns
t_{DRH}	Data Out Hold from $\overline{RD}$	5		10	ns
$t_{CSLRWRL}$	Chip Select Low to $\overline{WR}$ Low	5			ns
t_{WRHCSH}	$\overline{WR}$ High to $\overline{CS}$ High	5			ns
t_{PWR}	$\overline{WR}$ Pulse Width	50			ns
t_{DWS}	Write Data Setup Time	10			ns
t_{DWH}	Write Data Hold Time	0			ns

External ROM Timing

Figure 9. ROM Read Cycle

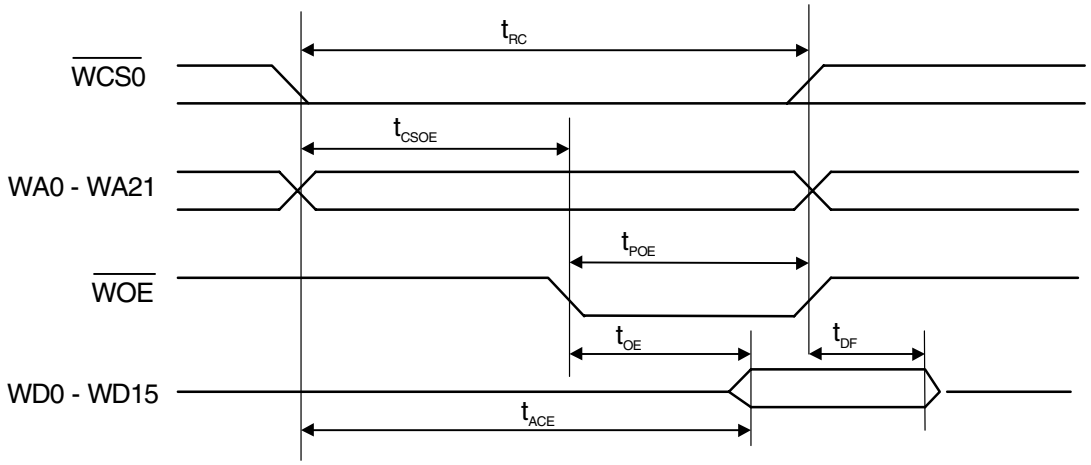


Table 6. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	5•tck		6•tck	ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ Low	2•tck - 5		3•tck + 5	ns
t_{POE}	Output Enable Pulse Width		3•tck		ns
t_{ACE}	Chip Select/Address Access Time	5•tck - 5			ns
t_{OE}	Output Enable Access Time	3•tck - 5			ns
t_{DF}	Chip Select or $\overline{WOE}$ High to Input Data High-Z	0		2•tck - 5	ns

External RAM Timing

Figure 10. 16-bit SRAM Read Cycle

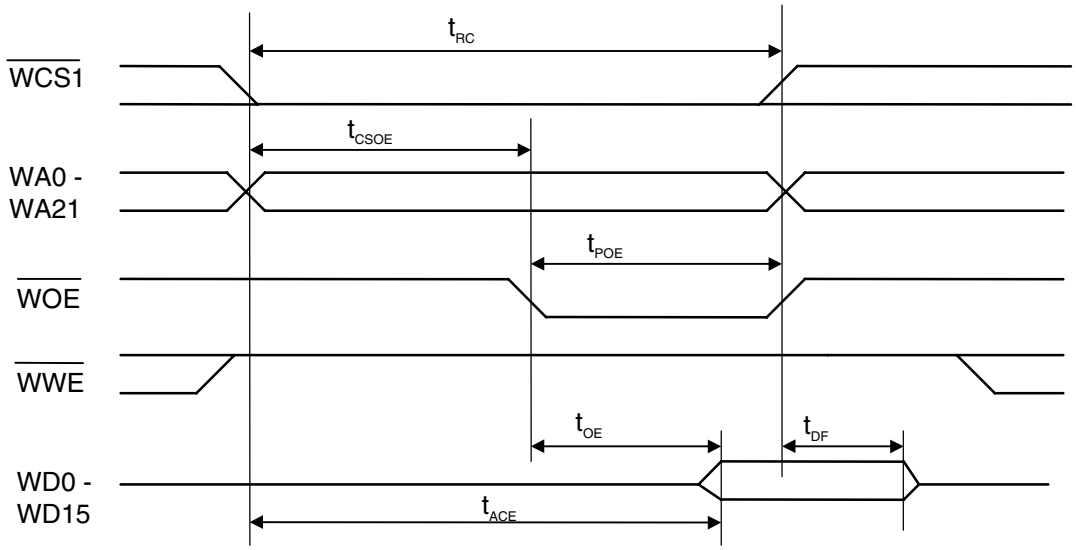


Figure 11. 16-bit SRAM Write Cycle

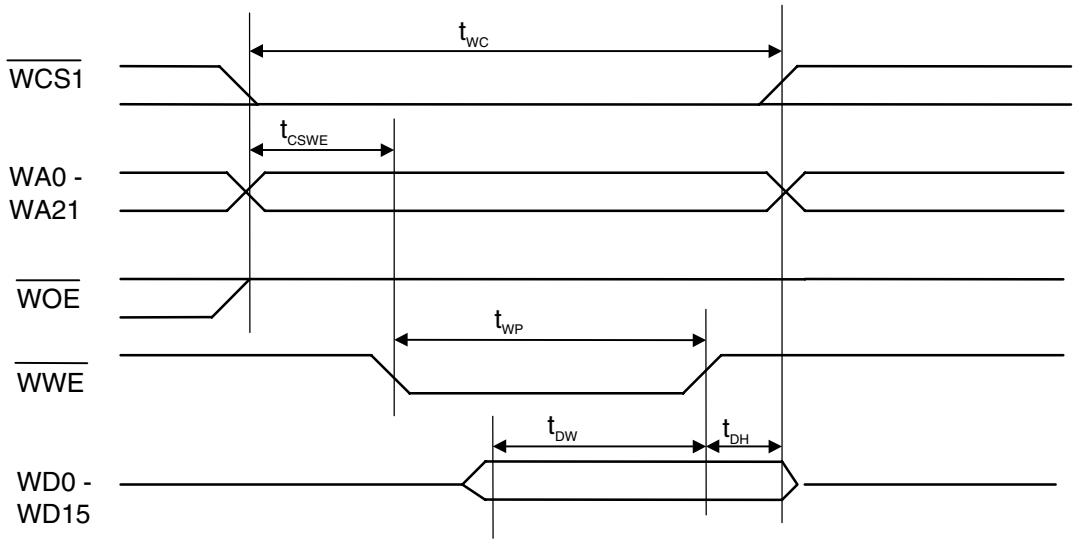


Table 7. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	5•tck	–	6•tck	ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ Low	2•tck - 5	–	3•tck + 5	ns
t_{POE}	Output Enable Pulse Width	–	3•tck	–	ns
t_{ACE}	Chip Select/Address Access Time	5•tck - 5	–	–	ns
t_{OE}	Output Enable Access Time	3•tck - 5	–	–	ns
t_{DF}	Chip Select or $\overline{WOE}$ High to Input Data High-Z	0	–	2•tck - 5	ns
t_{WC}	Write Cycle Time	5•tck	–	6•tck	ns
t_{CSWE}	Write Enable Low from $\overline{CS}$ or Address or $\overline{WOE}$	2•tck - 10	–	–	ns
t_{WP}	Write Pulse Width	–	4•tck	–	ns
t_{DW}	Data Out Setup Time	4•tck - 10	–	–	ns
t_{DH}	Data Out Hold Time	10	–	–	ns

Figure 12. 8-bit SRAM Read Cycle

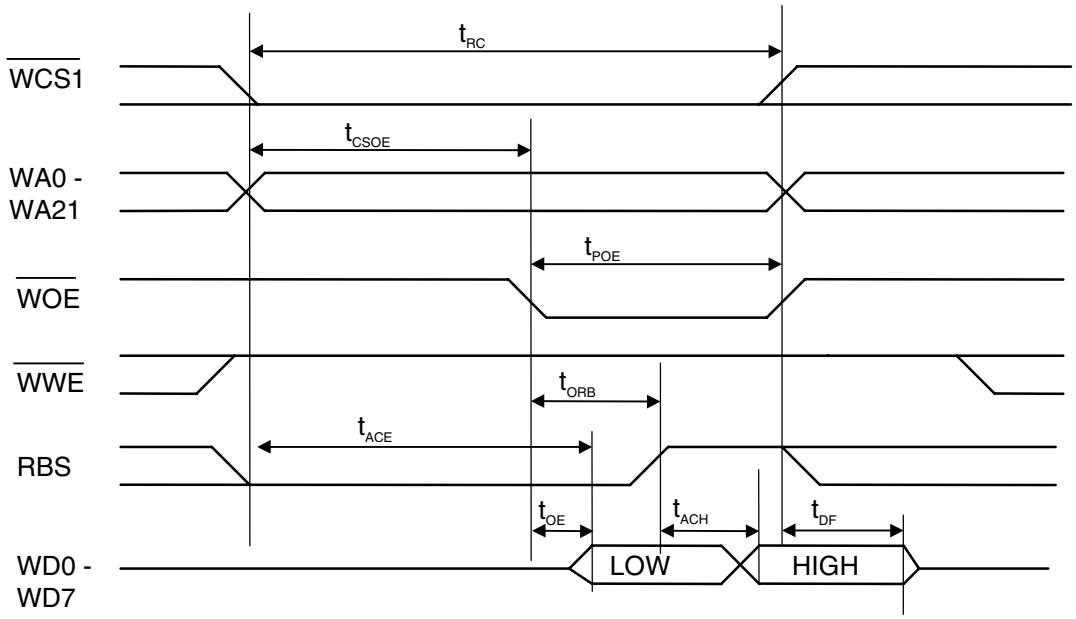


Figure 13. 8-bit SRAM Write Cycle

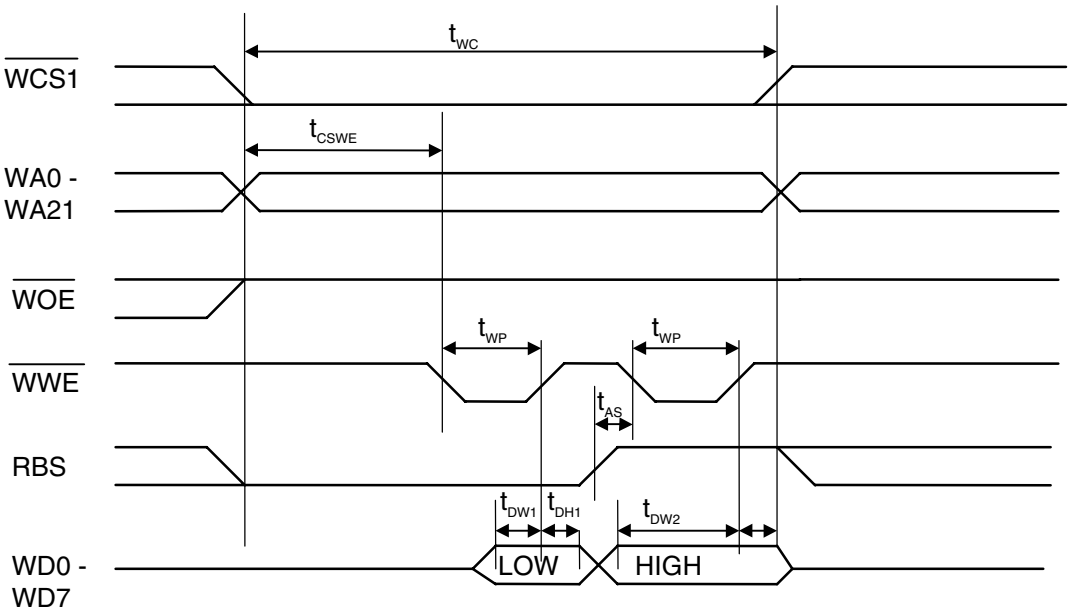


Table 8. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Word Read Cycle Time	5•tck		6•tck	ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ Low	2•tck - 5		3•tck + 5	ns
t_{POE}	Output Enable Pulse Width		3•tck		ns
t_{ACE}	Chip Select/Address Low Byte Access Time	3•tck - 5			ns
t_{OE}	Output Enable Low Byte Access Time	tck - 5			ns
t_{ORB}	Output Enable Low to Byte Select High	–	tck		ns
t_{ACH}	Byte Select High Byte Access Time	2•tck - 5			ns
t_{DF}	Chip Select or $\overline{WOE}$ High to Input Data High-Z	0		2•tck - 5	ns
t_{WC}	Word Write Cycle Time	5•tck		6•tck	ns
t_{CSWE}	First $\overline{WWE}$ Low from $\overline{CS}$ or Address or $\overline{WOE}$	2•tck - 10			ns
t_{WP}	Write (Low and High Byte) Pulse Width	1.5•tck - 5			ns
t_{DW1}	Data Out Low Byte Setup Time	1.5tck - 10			ns
t_{DH1}	Data Out Low Byte Hold Time	0.5•tck + 10			ns
t_{AS}	RBS High to Second Write Pulse	0.5•tck - 5			ns
t_{DW2}	Data Out High Byte Setup Time	2•tck - 10			ns
t_{DH2}	Data Out High Byte Hold Time	10			ns

Digital Audio

Figure 14. Digital Audio Timing

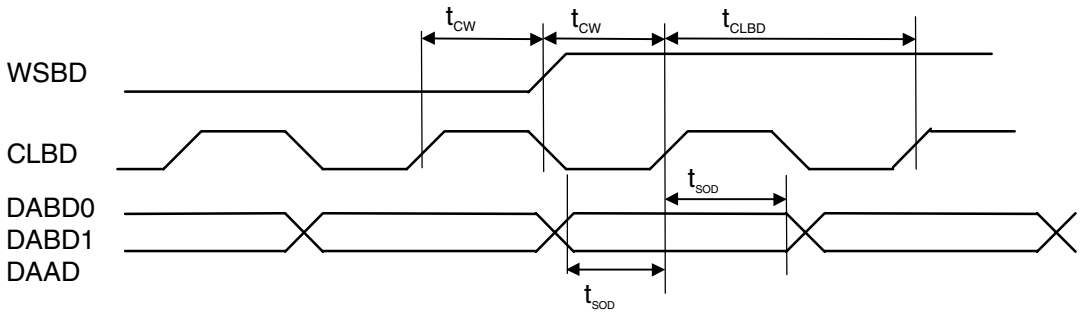
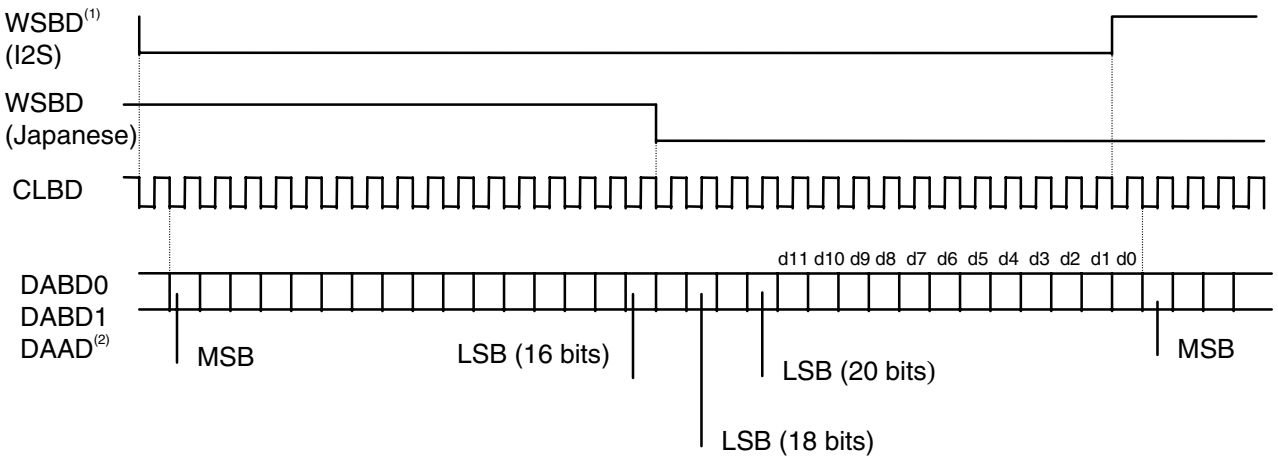


Table 9. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD Rising to WSBD	8•tck - 10			ns
t_{SOD}	DABD Valid Prior to/After CLBD Rising	8•tck - 10			ns
t_{CLBD}	CLBD Cycle Time		16•tck		ns

Digital Audio Frame

Figure 15. Digital Audio Frame Format



Notes: 1. Selection between I2S and Japanese format is a firmware option.

2. DAAD is 16 bits only.

3. When connected with Codecs such as CS4216 or CS4218, D0 - D11 can be used to hold independent auxiliary information on left and right words. Refer to corresponding Codec datasheets for details.

Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20 ms. The $\overline{\text{RESET}}$ signal is normally derived from the main board or PC master reset. However, a typical RC/diode power-up network can also be used for some applications.

After the low-to-high transition of $\overline{\text{RESET}}$, the following occurs:

- Synthesis/DSP enters an idle state.
- The RUN output is set to zero.
- P16 program execution starts from address 0100H in ROM space ($\overline{\text{WCS0}}$ low).

If $\overline{\text{PDWN}}$ is asserted low, then all I/Os and outputs will be floated, and the crystal oscillator and PLL will be stopped. The chip enters a deep power-down sleep mode. To exit power-down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

Recommended Board Layout

As for all HCMOS high-integration ICs, some rules of board layout should be followed for reliable device operation:

- GND, V_{CC}, V_{C3} distribution, decouplings

All GND, V_{CC}, V_{C3} pins should be connected. GND, V_{CC}, V_{C3} planes are strongly recommended below the SAM9733. The board GND and V_{CC} distribution should be in grid form. If 3.3V is not available, then V_{C3} can be connected to V_{CC} through 2*1N4148 diodes in series. This provides a minimum 1.4V voltage drop which allows V_{C3} to be within specifications.

Recommended decoupling is 0.1 µF at each corner of the IC with an additional 10 µF decoupling close to the crystal. V_{C3} requires a single 0.1 µF decoupling.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9733 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9733.

- Buses

Parallel layout from D0 - D7 and WA0 - WA21/WD0 - WD15 should be avoided. The D0 - D7 bus is an asynchronous high-transient current-type bus. Even on short distances, it can induce pulses on WA0 - WA21/WD0 - WD15 which can corrupt address and/or data on these buses.

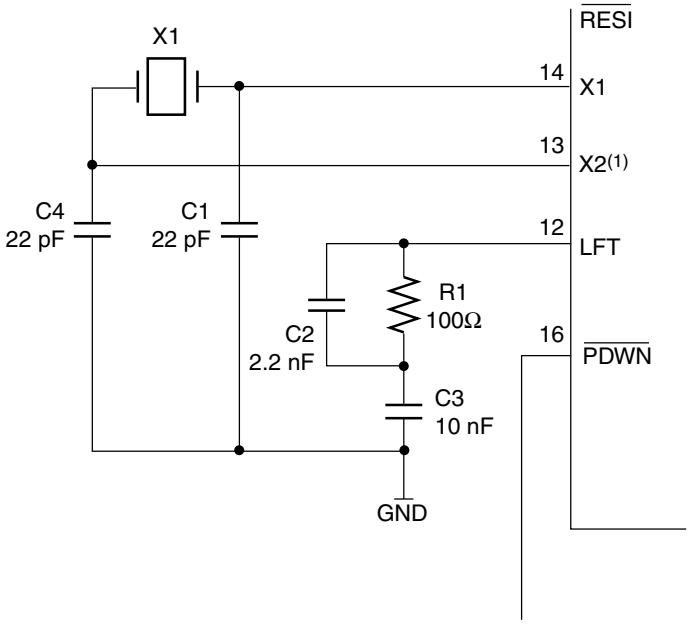
A ground plane should be implemented below the D0 - D7 bus, which connects both to the PC-ISA connector and to the SAM9733 GND.

A ground plane should be implemented below the WA0 - WA21/WD0 - WD15 bus, which connects both to the ROM/SRAM grounds and to the SAM9733.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section

Recommended Crystal Compensation and LFT Filter



Note: 1. The X2 output cannot be used to drive another circuit.

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