Features

- **AM/FM Tuner Front End with Integrated PLL**
- **AM Up-conversion System (AM-IF: 10.7 MHz)**
- **FM Down-conversion System (FM-IF: 10.7 MHz)**
- **IF Frequencies up to 25 MHz**
- **Fine-tuning Steps: AM = 1 kHz and FM = 50 kHz/25 kHz/12.5 kHz**
- **Fast Fractional PLL (Lock Time < 1 ms) Inclusive Spurious Compensation**
- **Fast RF-AGC, Programmable in 1-dB Steps**
- **Fast IF-AGC, Programmable in 2-dB Steps**
- **Fast Frequency Change by 2 Programmable N-divider**
- **Two DACs for Automatic Tuner Alignment**
- **High S/N Ratio**
- **3-wire Bus (Enable, Clock and Data; 3 V and 5 V Microcontrollers-compatible)**

Electrostatic sensitive device.
Observe precautions for handling.

AM/FM Front End IC

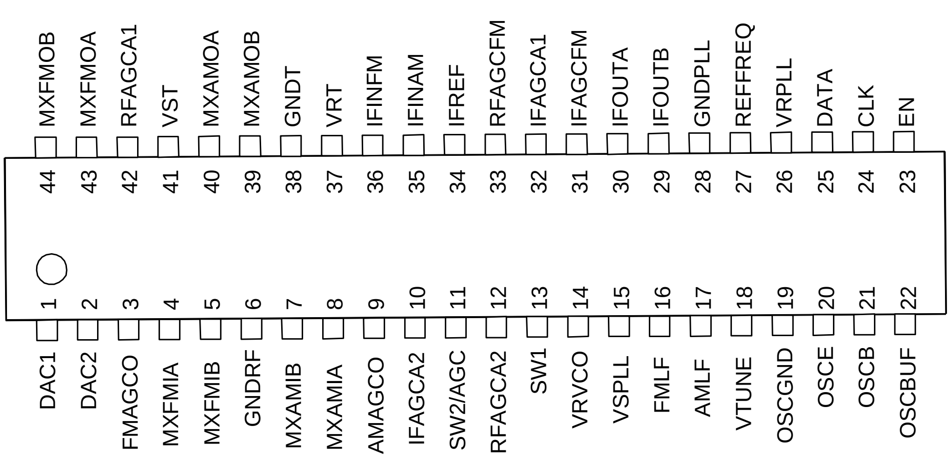
T4260

Description

The T4260 is an advanced AM/FM receiver with integrated fast PLL as a single-chip solution based on Atmel's high-performance BICMOS II technology. The low-impedance driver at the IF output is designed for the A/D of a digital IF. The fast tuning concept realized in this part is based on patents held by Atmel and allows lock times less than 1 ms for a jump over the FM band with a step width of 12.5 kHz. The AM up-conversion and the FM down-conversion allows an economic filter concept. An automatic tuner alignment is provided by built-in DACs for gain and offset compensation. The frequency range of the IC covers the FM broadcasting band as well as the AM band. The low current consumption helps the designers to achieve economic power consumption concepts and helps to keep the power dissipation in the tuner low.

Pin Description

Figure 1. Pinning SSO44

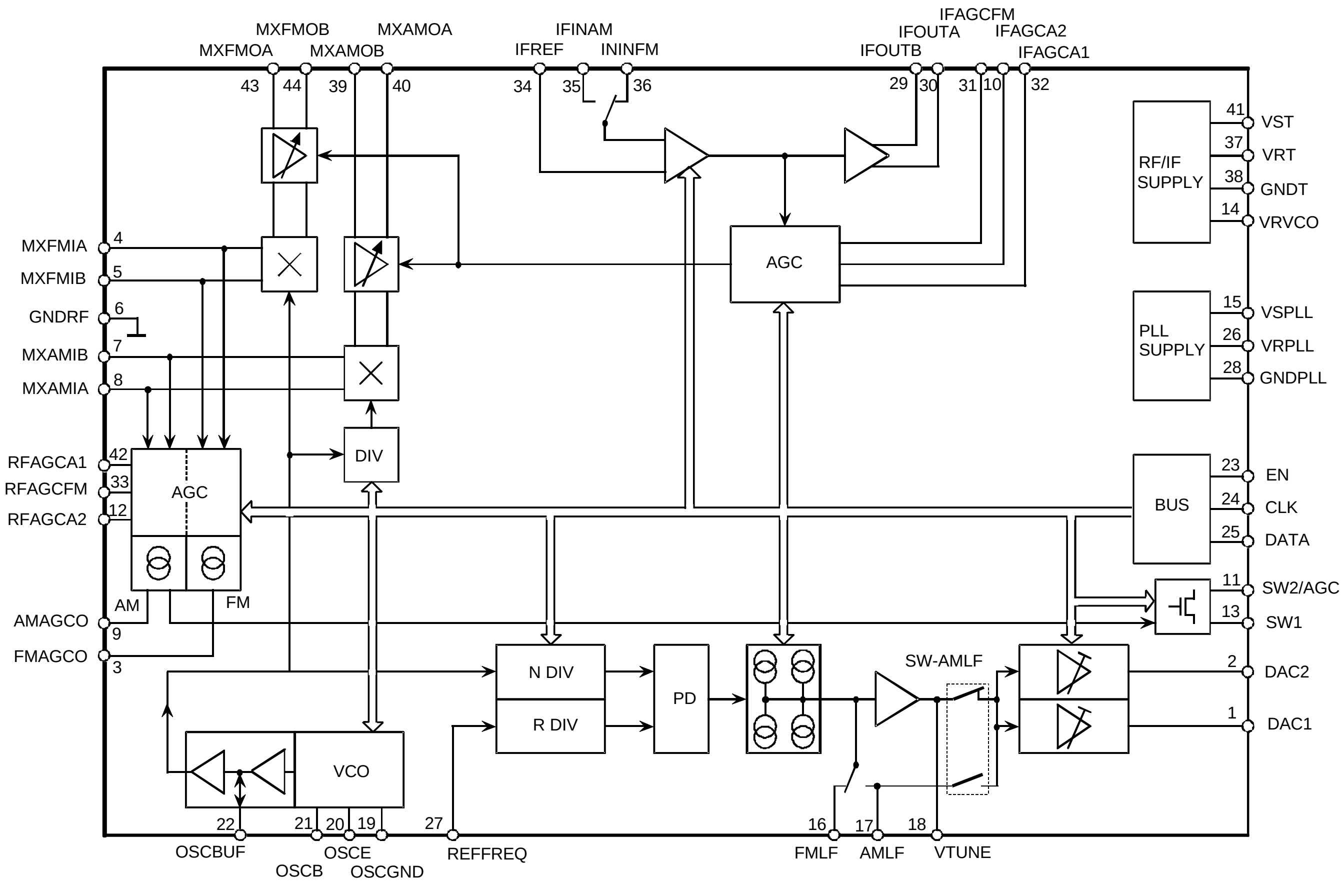


Rev. 4528D–AUDR–09/02

Pin Description

Pin	Symbol	Function
1	DAC1	DAC1 output
2	DAC2	DAC2 output
3	FMAGCO	FM AGC current
4	MXFMIA	FM mixer input A
5	MXFMIB	FM mixer input B
6	GNDRF	RF ground
7	MXAMIB	AM mixer input B
8	MXAMIA	AM mixer input A
9	AMAGCO	AM AGC current
10	IFAGCA2	AM IF-AGC filter 2
11	SW2/AGC	Switch 2 / AM AGC voltage
12	RFAGCA2	RF AM-AGC filter 2
13	SW1	Switching output 1
14	VRVCO	VCO reference voltage
15	VSPLL	PLL supply voltage
16	FMLF	FM loop filter
17	AMLF	AM loop filter
18	VTUNE	Tuning voltage
19	OSCGND	Oscillator ground
20	OSCE	Oscillator emitter
21	OSCB	Oscillator base
22	OSCBUF	Oscillator buffer output / input
23	EN	3-wire bus Enable
24	CLK	3-wire bus Clock
25	DATA	3-wire bus Data
26	VRPLL	PLL reference voltage
27	REFFREQ	PLL reference frequency
28	GNDPLL	PLL ground
29	IFOUTB	IF output B
30	IFOUTA	IF output A
31	IFAGCFM	FM IF-AGC filter
32	IFAGCA1	AM IF-AGC filter 1
33	RFAGCFM	RF FM-AGC filter
34	IFREF	IF amplifier reference input
35	IFINAM	IF amplifier AM input
36	IFINFM	IF amplifier FM input
37	VRT	Tuner reference voltage
38	GNDT	Tuner ground
39	MXAMOB	AM mixer output B
40	MXAMOA	AM mixer output A
41	VST	Tuner supply voltage
42	RFAGCA1	RF AM-AGC filter 1
43	MXFMOA	FM mixer output A
44	MXFMOB	FM mixer output B

Figure 2. Block Diagram



Functional Description

The T4260 implements an AM up-conversion reception path from the RF input signal to the IF output signal. A VCO and an LO prescaler for AM are integrated to generate the LO frequency to the AM mixer. The FM reception path generates the same LO frequency from the RF input signal by a down-conversion to the IF output. The IF A/D output is designed for digital signal processing. The IF can be chosen in the range of 10 MHz to 25 MHz. Automatic gain control (AGC) circuits are implemented to control the preamplifier stages in the AM and FM reception paths.

For improved performance, the PLL has an integrated special 2-bit shift fractional logic with spurious suppression that enables fast frequency changes in AM and FM mode by a low step frequency (f_{PDF}). In addition, two programmable DACs (Digital to Analog Converter) support the alignment via a microcontroller.

For a double-tuner concept, external voltage can be applied at the input of the DACs, the internal PLL can switched off and the OSC buffer (output) can also be used as input.

Several register bits (Bit 0 to Bit 145) are used to control the circuit's operation and to adapt certain circuit parameters to the specific application. The control bits are organized in four 8-bit, four 16-bit and three 24-bit registers that can be programmed by the 3-wire bus protocol. The bus protocol and the bit-to-register mapping is described in the section "3-wire Bus Description". The meaning of the control bits is mentioned in the following sections.

Absolute Maximum Ratings

All voltages are referred to GND

Parameters		Symbol	Value	Unit
Analog supply voltage	Pins 15 and 41	V_{ST}, V_{SPLL}	10	V
Maximum power consumption		P_{tot}	1.0	W
Ambient temperature range		T_{amb}	-40 to +85	°C
Storage temperature range		T_{stg}	-40 to +150	°C
Junction temperature		T_j	150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient, soldered to PCB	R_{thJA}	52	K/W

Operating Range

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage range [(1)]	Pins 15 and 41	V_{ST}, V_{SPLL}	8	8.5	10	V
Supply current	Pins 15 and 41	I_S	70		100	mA
Ambient temperature		T_{amb}	-40		85	°C
Oscillator frequency	Pin 21	R_{fi}	60		175	MHz

Note: 1. V_{ST} and V_{SPLL} must have the same voltage.

Electrical Characteristics

Test conditions (unless otherwise specified): V_{ST}/V_{SPLL} = +8.5 V, T_{amb} = +25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**PLL Divider**								
1.1	Programmable R-divider	14-bit register			3		16,383		A
1.2	Programmable (VCO) N-divider (1 kHz step frequency)	2- × 18-bit register switchable via Bit 5			3		262,143		A
1.3	Reference oscillator input voltage	f = 0.1 MHz to 3 MHz	27		100			mV_{rms}	B
1.4	Reference frequency	FM AM			120 120	150 2,850	10,000 10,000	kHz kHz	
1.5	Settling time in FM mode (switching from 87.5 MHz to 108 MHz or vice versa)	f_{PD} = 50 kHz I_{PD} = 2 mA				1		ms	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{ST}/V_{SPLL} = +8.5 V, T_{amb} = +25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2	**AMLF/FMLF**								
2.1	Output current 1	FMLF, AMLF = 1.8 V	16, 17		40	50	60	µA	A (1)
2.2	Output current 2	FMLF, AMLF = 1.8 V	16, 17		80	100	120	µA	A (1)
2.3	Output current 3	FMLF, AMLF = 1.8 V	16, 17		850	1000	1250	µA	A (1)
2.4	Output current 4	FMLF, AMLF = 1.8 V	16, 17		1650	2000	2450	µA	A (1)
2.5	Leakage current	FMLF, AMLF = 1.8 V	16, 17				10	nA	A (1)
3	**VTUNE**								
3.1	Saturation voltage LOW	$V_{SATH} = (V_A - V_{PDOFM})$	18	V_{SATL}	100	200	400	mV	C
3.2	Saturation voltage HIGH	$V_{SATH} = (V_A - V_{PDOFM})$	18	V_{SATH}			500	mV	C
4	**DAC1, DAC2**								
4.1	Output current		1, 2	$I_{DAC1,2}$			1	mA	D
4.2	Output voltage		1, 2	$V_{DAC1,2}$	0.3		V_S-0.6	V	A
4.3	Maximum offset range	offset = 0, gain = 58	1, 2		0.9	0.98	1.1	V	A (1)
4.4	Minimum offset range	offset = 127, gain = 58	1, 2		0.9	-0.98	-1.1	V	A (1)
4.5	Maximum gain range	gain = 255, offset = 64	1, 2		2.06	2.09	2.13		A (1)
4.6	Minimum gain range	gain = 0, offset = 64	1, 2		0.63	0.67	0.73		A (1)
5	**Oscillator**								
5.1	Frequency range		21		60		170	MHz	B
5.2	Fractional frequency range	Fractional mode	21		60		140	MHz	A
5.3	Buffer output		22		150			mV_{rms}	C
6	**Oscillator Input**								
6.1	Input voltage		21	V_{OSC}	150			mV_{rms}	A
7	**FM Mixer**								
7.1	Frequency range				75		163	MHz	B
7.2	Input IP3					133		dBµV	C
7.3	Input impedance					3.5		kΩ	D
7.4	Input capacitance						4	pF	D
7.5	Noise figure			F		14		dB	C
7.6	Conversion transconductance				2.6	3.1	3.6	mS	D (1)
8	**AM Mixer (Symmetrical Input)**								
8.1	Frequency range				0.075		26	MHz	B
8.2	Input IP3					133		dBµV	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{ST}/V_{SPLL} = +8.5 V, T_{amb} = +25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.3	Input impedance					2.5		kΩ	D
8.4	Noise figure			F		10		dB	C
8.5	Conversion transconductance				2.6	3.1	3.6	mS	D [1]
9	**Isolation**								
9.1	Isolation AM-FM					40		dB	C
9.2	IF suppression					40		dB	C
10	**RF-AGC**								
10.1	Frequency range	FM AM			75 0.075		163 26	MHz MHz	A
10.2	Output current	FM AM				5 5		mA mA	B
10.3	Output current time constant	FM rising FM falling AM symmetrical				2 50 40		ms ms ms	C
10.4	RF-AGC AM threshold (programmable with Bit 12 - Bit 15)	88 dBµV	42		87	88	90	dBµV	A [1]
		89 dBµV	42		88	89	91	dBµV	A [1]
		90 dBµV	42		89	90	92	dBµV	A [1]
		91 dBµV	42		90	91	93	dBµV	A [1]
		92 dBµV	42		91	92	94	dBµV	A [1]
		93 dBµV	42		92	93	95	dBµV	A [1]
		94 dBµV	42		93	94	96	dBµV	A [1]
		95 dBµV	42		94	95	97	dBµV	A [1]
		96 dBµV	42		95	96	98	dBµV	A [1]
		97 dBµV	42		96	97	99	dBµV	A [1]
		98 dBµV	42		97	98	100	dBµV	A [1]
		99 dBµV	42		98	99	101	dBµV	A [1]
		100 dBµV	42		99	100	102	dBµV	A [1]
		101 dBµV	42		100	101	103	dBµV	A [1]
		102 dBµV	42		101	102	104	dBµV	A [1]
		103 dBµV	42		102	103	107	dBµV	A [1]

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Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{ST}/V_{SPLL} = +8.5 V, T_{amb} = +25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.5	RF-AGC FM threshold (programmable with Bit 12 - Bit 15)	91 dBµV	33		90	91	93	dBµV	A (1)
		92 dBµV	33		91	92	95	dBµV	A (1)
		93 dBµV	33		92	93	96	dBµV	A (1)
		94 dBµV	33		93	94	96	dBµV	A (1)
		95 dBµV	33		94	95	98	dBµV	A (1)
		96 dBµV	33		95	96	99	dBµV	A (1)
		97 dBµV	33		96	97	102	dBµV	A (1)
		98 dBµV	33		97	98	101	dBµV	A (1)
		99 dBµV	33		98	99	102	dBµV	A (1)
		100 dBµV	33		99	100	104	dBµV	A (1)
		101 dBµV	33		100	101	104	dBµV	A (1)
		102 dBµV	33		101	102	105	dBµV	A (1)
		103 dBµV	33		102	103	106	dBµV	A (1)
		104 dBµV	33		103	104	107	dBµV	A (1)
		105 dBµV	33		104	105	108	dBµV	A (1)
		106 dBµV	33		105	106	109	dBµV	A (1)
11	**IF Amplifier**								
11.1	Frequency range				10		25	MHz	A
11.2	Output voltage					117		dBµV	B
11.3	Distortion (2-tone IM3)	f1 = 10.7 MHz f2 = 10.75 MHz RL = 2 × 300 Ω				55		dB	A
11.4	Gain (programmable in 2-dB steps)	Minimum gain Maximum gain				12 42		dB dB	A
11.5	Input impedance	FM AM	36, 35			330 2500		Ω Ω	D
12	**IF-AGC**								
12.1	IF-AGC AM/FM threshold (programmable with Bit 0 - Bit 2)	109 dBµV	29/30		108	109	112	dBµV	A (1)
		111 dBµV	29/30		110	111	114	dBµV	A (1)
		113 dBµV	29/30		111	113	115	dBµV	A (1)
		115 dBµV	29/30		113	115	117	dBµV	A (1)
		117 dBµV	29/30		116	117	121	dBµV	A (1)
		118 dBµV	29/30		117	118	122	dBµV	A (1)
		119 dBµV	29/30		118	119	123	dBµV	A (1)
		121 dBµV	29/30		120	121	126	dBµV	A (1)
12.2	AGC dynamic range					TBD		dB	B
12.3	AGC time constant (external capacity ≤ 100 nF)	FM rising FM falling AM symmetrical				16 4 200		µs ms ms	D
13	**IF Gain**								

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Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{ST}/V_{SPLL} = +8.5 V, T_{amb} = +25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13.1	IF gain (programmable with Bit 6 - Bit 9)	12 dB			9	12	14	dB	A (1)
		14 dB			12	14	16	dB	A (1)
		16 dB			14	16	18	dB	A (1)
		18 dB			17	18	20	dB	C (1)
		20 dB			17	20	22	dB	A (1)
		22 dB			19	22	24	dB	C (1)
		24 dB			21	24	26	dB	C (1)
		26 dB			23	26	28	dB	C (1)
		28 dB			25	28	30	dB	A (1)
		30 dB			27	30	32	dB	C (1)
		32 dB			29	32	34	dB	C (1)
		34 dB			31	34	36	dB	C (1)
		36 dB			33	36	38	dB	C (1)
		38 dB			35	38	40	dB	C (1)
		40 dB			37	40	42	dB	C (1)
		42 dB			39	42	44	dB	A (1)
14	**SWO1 (Open Drain)**								
14.1	Output voltageLOW	I = 1 mA, V_{SWO1} = 8.5 V	13	V_{SWOL}	100	160	200	mV	A
14.2	Output leakage current HIGH		13	I_{OHL}			10	µA	A
14.3	Maximum output voltage		13			8.5		V	C
15	**SW2/AGC (Open Drain in Switch Mode)**								
15.1	Output voltage LOW	I = 1 mA, V11 = 6 V	11	V_{SWOL}	100	160	200	mV	A
15.2	Output leakage current HIGH		11	I_{OHL}			10	µA	A
15.3	Maximum output voltage		11			6		V	C
16	**3-wire Bus, ENABLE, DATA, CLOCK**								
16.1	Input voltage	High Low	23-25	V_{BUS} V_{BUS}	2.7 -0.3		5.3 0.8	V V	A A
16.2	Clock frequency		24				1.0	MHz	B
16.3	Period of CLK		24	t_H t_L	250 250			ns ns	C C
16.4	Rise time EN, DA, CLK		23-25	t_R			400	ns	C
16.5	Fall time EN, DA, CLK		23-25	t_F			100	ns	C
16.6	Set-up time		23-25	t_S	100			ns	C
16.7	Hold time EN		23	t_{HEN}	250			ns	C
16.8	Hold time DA		25	t_{HDA}	0			ns	C

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Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

3-wire Bus Description

The register settings of the T4260 are programmed by a 3-wire bus protocol. The bus protocol consists of separate commands. A defined number of bits is transmitted sequentially during each command.

One command is used to program all bits of one register. The different registers available (see chapter "3-wire Bus Data Transfer") are addressed by the length of the command (number of transmitted bits) and by two address bits that are unique to each register of a given length. 8-bit registers are programmed by 8-bit commands, 16-bit registers are programmed by 16-bit commands and 24-bit registers are programmed by 24-bit commands.

Each bus command starts with a falling edge on the enable line (EN) and ends with a rising edge on EN. EN has to be kept LOW during the bus command.

The sequence of transmitted bits during one command starts with the MSB of the first byte and ends with the LSB of the last byte of the register addressed. To transmit one bit (0/1), DATA has to be set to the appropriate value (LOW/HIGH) and a HIGH-to-LOW transition has to be performed on the clock line (CLK) while DATA is valid. The DATA is evaluated at the falling edges of CLK. The number of HIGH-to-LOW transitions on CLK during the LOW period of EN is used to determine the length of the command.

Figure 3. 3-wire Pulse Diagram

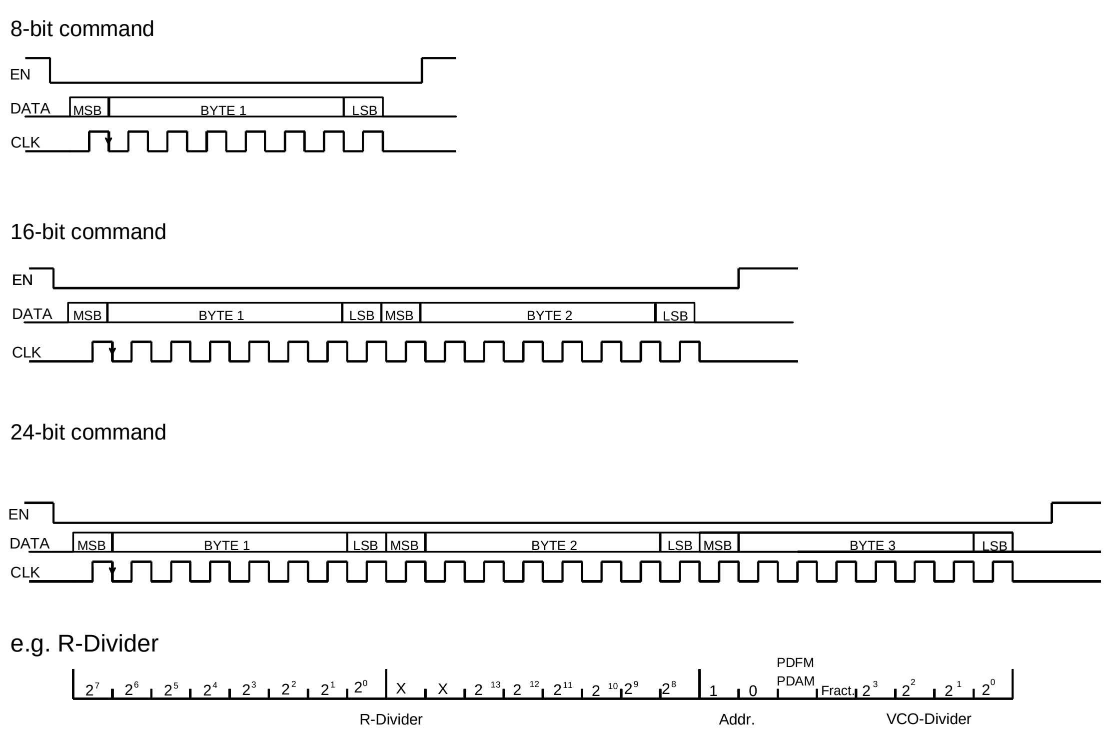
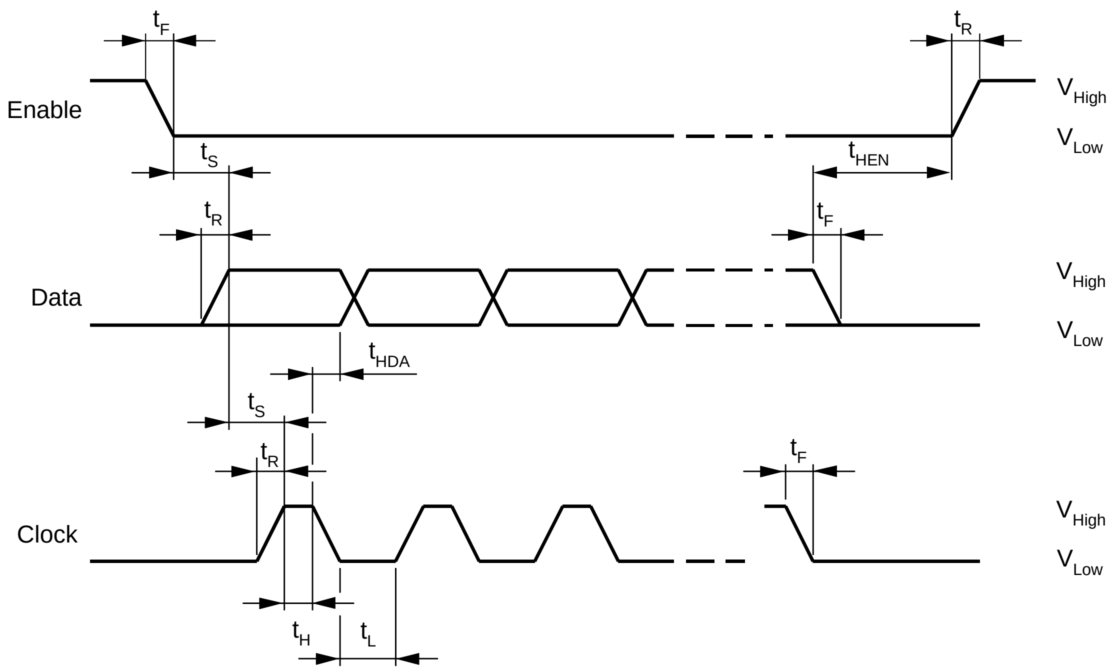


Figure 4. 3-wire Bus Timing Diagram



3-wire Bus Data Transfer

Table 1. Control Registers

A24_10																							
MSB			BYTE 1				LSB	MSB			BYTE 2				LSB	MSB			BYTE 3				LSB
R-Divider								R-Divider								ADDR.		PDA M/P DFM	Fractional	Divider VCO			
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	x	x	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	1	0	1/0	0/1	2^3	2^2	2^1	2^0
131	130	129	128	127	126	125	124	139	138	137	136	135	134	133	132	x	x	145	144	143	142	141	140

A24_01																							
MSB			BYTE 1				LSB	MSB			BYTE 2				LSB	MSB			BYTE 3				LSB
N2-Divider								N2-Divider								ADDR.		x	x	x	x	N2-Divider	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	0	1	0	0	0	0	2^{17}	2^{16}
109	108	107	106	105	104	103	102	117	116	115	114	113	112	111	110	x	x	123	122	121	120	119	118

A24_00																							
MSB			BYTE 1				LSB	MSB			BYTE 2				LSB	MSB			BYTE 3				LSB
N1-Divider								N1-Divider								ADDR.		x	x	x	x	N1-Divider	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	0	0	0	0	0	0	2^{17}	2^{16}
87	86	85	84	83	82	81	80	95	94	93	92	91	90	89	88	x	x	101	100	99	98	97	96

A16_11															
MSB			BYTE 1				LSB	MSB			BYTE 2				LSB
DAC2-Gain								ADDR.							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	1	1	x	x	x	x	x	x
73	72	71	70	69	68	67	66	x	x	79	78	77	76	75	74

A16_10															
MSB			BYTE 1				LSB	MSB			BYTE 2				LSB
DAC2-Offset								ADDR.		SW-AMLF	Osc.-Buffer	Low c.CP	High c.CP	SW-impulse	SW-wire
x	2^6	2^5	2^4	2^3	2^2	2^1	2^0	1	0	1 = standard	ON/OFF	HI/LO	HI/LO	ON/OFF	ON/OFF
59	58	57	56	55	54	53	52	x	x	65	64	63	62	61	60

A16_01															
MSB			BYTE 1				LSB	MSB			BYTE 2				LSB
DAC1-Gain								ADDR.					1=SW2 0=AGC	SW2 1=low	SW1 1=low
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	1	x	x	x	1/0	1/0	1/0
45	44	43	42	41	40	39	38	x	x	51	50	49	48	47	46

A16_00															
MSB			BYTE 1				LSB	MSB			BYTE 2				LSB
DAC1-Offset								ADDR.		Lock det. filter		Lock det. sensitiv.		Sh_LD_Direct	Sh_Direct
x	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	0	1/0	1/0	1/0	1/0	1/0	1/0
31	30	29	28	27	26	25	24	x	x	37	36	35	34	33	32

A8_11							
MSB			BYTE 1				LSB
ADDR.		Delay time high cur. CP2		Delay time high cur. CP1		HCDEL/Direct	HCDEL/_Direct
1	1	ON/OFF	HI/LO	ON/OFF	HI/LO	1/0	1/0
x	x	23	22	21	20	19	18

A8_10							
MSB			BYTE 1				LSB
ADDR.		AM/FM	IF-AGC	RF-AGC			
1	0	1/0	1/0	2^3	2^2	2^1	2^0
x	x	17	16	15	14	13	12

A8_01							
MSB			BYTE 1				LSB
ADDR.		IF-IN	VCO	IF-Gain			
0	1	AM/FM	HI/LO	2^3	2^2	2^1	2^0
x	x	11	10	9	8	7	6

A8_00							
MSB			BYTE 1				LSB
ADDR.		N2/N1	PLL ON/OFF	PDTE/PD	IF-AGC		
0	0	1/0	1/0	1/0	2^2	2^1	2^0
x	x	5	4	3	2	1	0

Bus Control

IF-AGC

The IF-AGC controls the level of the IF signal that is passed to the external ceramic filter and the IF input (AM Pin 35 or FM Pin 36 and Pin 34). In AM mode the time constant can be selected by the external capacitors at Pin 32 (IFAGCA1) and Pin 10 (IFAGCA2) and in FM mode by an external capacitor at Pin 31 (IFAGCFM). In AM mode, the double pole (by the capacitors at Pin 32 and Pin 10) allows a better harmonic distortion by a lower time constant.

The IF-AGC threshold can be controlled by setting Bits 0 to 2 as given in Table 2.

Table 2. IF-AGC Threshold

IF-AGC	B2	B1	B0
109 dBµV	0	0	0
111 dBµV	0	0	1
113 dBµV	0	1	0
115 dBµV	0	1	1
117 dBµV	1	0	0
118 dBµV	1	0	1
119 dBµV	1	1	0
121 dBµV	1	1	1

The IF-AGC ON/OFF can be controlled by Bit 16 as given in Table 3.

Table 3. IF-AGC

IF-AGC ON/OFF	B16
IF-AGC ON	0
IF-AGC OFF	1

PD Test

Only in FM mode, the locked and unlocked condition of the PLL can be signaled at the AMLF-Pin (Pin 17) by activation of PD test (Bit 3 = 1). The locked PLL (in FM mode) is signaled by a high level (5 V) and the unlocked PLL by a low level (0 V) at Pin 17. For the use of PD test, it is necessary to interrupt the external AM loop filter to VTUNE (Pin 18) and to FMLF (Pin 16). Moreover, the loop filter operating mode has to be set to PDFM active (Bit 145 = 0).

Table 4. PD-Test Mode

PD TE/PD	B3
Pin 17 = AMLF output (standard)	0
Pin 17 = Lock detect output	1

N1/N2

The N2/N1 Bit controls the active N-divider. Only one of the two N-Divider can be active. The N1-Divider is activated by setting Bit 5 = 0, the N2-Divider by setting Bit 5 = 1.

Table 5. N-Divider

N2/N1	B5
N1-divider active	0
N2-divider active	1

IF Amplifier

The IF gain amplifier can be used in AM and FM mode to compensate the loss of the external ceramic bandfilters.

The IF gain can be controlled in 2-dB steps by setting Bit 6 to Bit 9 as given in Table 6.

Table 6. IF Gain

IF Gain	B9	B8	B7	B6
12 dB	0	0	0	0
14 dB	0	0	0	1
16 dB	0	0	1	0
18 dB	0	0	1	1
20 dB	0	1	0	0
...	...	...	...	...
40 dB	1	1	1	0
42 dB	1	1	1	1

The selection of the IF amplifier input can be controlled by Bit 11 as given in Table 7.

Table 7. IF-IN Operating Mode

IF-IN AM/FM	B11
IF-IN FM	0
IF-IN AM	1

REMARK:
The AM input (Pin 35) has an input impedance of 2.5 kΩ for matching with a crystal filter. The FM input (Pin 36) has an input impedance of 330 Ω for matching with a ceramic filter.

VCO

The VCO HI/LO function is controlled by means of Bit 10.

Table 8. VCO Operating Mode

VCO HI/LO	B10
VCO high current	0
VCO low current	1

RF-AGC

The AM and FM RF-AGC controls the current into the AM and FM pin diodes (FM Pin 3 and AM Pin 9) to limit the level at the AM or FM mixer input. If the level at the AM or FM mixer input exceeds the selected threshold, then the current into the AM or FM pin diodes increases. If this step is not sufficient in AM mode, the source drain voltage of the MOSFET (Pin 11) can be decreased. In AM mode, the time constants can be selected by the external capacitors at Pin 42 (RFAGCA1) and at Pin 12 (RFAGCAM2) and in FM mode by an external capacitor at Pin 33 (RFAGCFM). In AM mode, the double pole (by the capacitors at Pin 42 and Pin 12) allows a better harmonic distortion by a lower time constant.

The RF-AGC can be controlled in 1-dB steps by setting the Bits 12 to 15. The values for FM and AM are controlled by Bit 17.

Table 9. RF-AGC

RF-AGC AM	RF-AGC FM	B15	B14	B13	B12
88 dB	91 dB	0	0	0	0
89 dB	92 dB	0	0	0	1
90 dB	93 dB	0	0	1	0
91 dB	94 dB	0	0	1	1
92 dB	95 dB	0	1	0	0
...	...	...	...	...	...
102 dB	105 dB	1	1	1	0
103 dB	106 dB	1	1	1	1

Reception Mode

There are two different operation modes, AM and FM, which are selected by means of Bit 17 and Bit 145 according to Table 1 and Table 2. In AM mode (Bit 17 = 1), the AM mixer, the AM RF-AGC, the AM divider (prescaler) and the IF AM amplifier (input at Pin 35) are activated. In FM mode (Bit 17 = 0), the FM mixer, the FM RF-AGC and the IF FM amplifier (input at Pin 36) are activated.

In AM or FM reception mode, Bit 145 has to be set to the corresponding mode. The buffer amplifier input can be connected to Pin 16 (with the external FM loop filter) by Bit 145 = 0 and to Pin 17 (with the external AM loopfilter) by Bit 145 = 1.

The AM/FM function for the tuner part is controlled by Bit 17 as given in Table 10.

Table 10. Tuner Operating Modes

AM/FM	B17
FM	0
AM	1

PLL

The PLL can switch off by Bit 4 = 0. In this case, the N-Divider signal is internally connected to ground.

Table 11. PLL Mode

PLL ON/OFF	B4
PLL OFF	0
PLL ON	1

There are two registers, HCDEL 1 (Bits 20 and 21) and HCDEL 2 (Bits 22 and 23), to control the delay time of the high-current charge pump and to deactivate them. Bit 18 (HCDEL_Direct) and Bit 19 (HCDEL_LD/ Direct) determine whether register HCDEL 1 or 2 is used.

If Bit 19 is 0, then Bit 18 is used to select between HCDEL 1 and HCDEL 2.

If Bit 19 is 1, and no lock detect is signaled, register HCDEL 1 is used, if Bit 19 is 1 and a lock detect is signaled, then HCDEL 2 is used. Switching to HCDEL 1 can be limited to one time per N1/N2 change by setting Bit 18 to Bit 19.

Table 12. High-current Charge Pump Delay Time Register

HCDEL 1/2 Select Mode	HCDEL_ LD/ Direct B19	HCDEL_ Direct B18
Direct HCDEL 1	0	0
Direct HCDEL 2	0	1
HCDEL = lock_detect	1	0
HCDEL = lock detect, only 1 change per N1/N2 change	1	1

If Bits 20 and 21 (HCDEL 1) or Bits 22 and 23 (HDCEL 2) are both set to 0, then the high-current charge pump is deactivated. Otherwise, the delay time can be selected as described in Table 13.

Table 13. Delay Time of HCDEL Register

High-current Charge Pump	B21/B23	B20/B22
OFF	0	0
Delay time 5 ns	0	1
Delay time 10 ns	1	0
Delay time 15 ns	1	1

The VCO frequency N-divided signal and the reference frequency R-divided signal (step frequency) will be compared. If the delay time between both signals is lower than the choosen time (LD_sens) the PLL lock detect is signalized.

The lock detect sensitivity is controlled by Bits 34 and 35 as follows.

Table 14. Lock Detect Sensitivity Time

LD_sens	B35	B34
9 ns	0	0
6 ns	0	1
5 ns	1	0
4 ns	1	1

REMARK: The values are the phase differences on the phase detector.

The Shift-Direct function can also be controlled by Bit 32 and Bit 33 as follows. If Bit 33 = 0 and Bit 32 = 0, the R/N-divider is shifted by two bits to the right. Bit 33 controls the manual or the lock detect-controlled 2-bit shift of the R/N-divider.

A divider 2-bit shift (Bit 33 = 0 and Bit 32 = 0) allows faster frequeny changes by using a four times higher step frequeny (e.g., f_{PDF} = 50 kHz instead of f_{PDF} = 12.5 kHz). If the PLL is locked (after the frequency change), the normal step frequency (e.g., f_{PDF} = 12.5 kHz) will be active again.

If no 2-bit shift is used (Bit 33 = 0 and Bit 32 = 1), the frequeny changes will be done with the normal step frequency (12.5 kHz).

Table 15. Manual and Lock Detect Shift Mode

Sh_LD Control	Sh_LD/Direct	Sh_Direct
	B33	B32
Dividers 2-bit shift	0	0
No shift	0	1
Sh = Lock_detect	1	0
Sh = Lock_detect, only 1 change per N1/N2 change	1	1

The lock detect filter is controlled by Bits 36 and 37 as given in Table 16.

Table 16. LD Filter

LD Filter	B37	B36
Direct	0	0
1 clock delay	0	1
2 clock delay	1	0
3 clock delay	1	1

REMARK:
Before the lock detect signal becomes valid, the phase comparison must be valid 0, 1, 2, 3 periods of f_{PFD}.

SW1 (Pin 13)

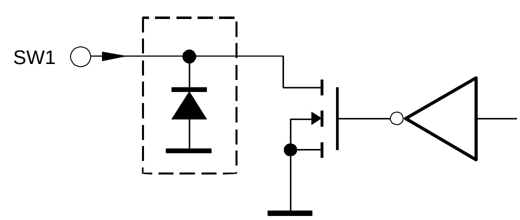
The switching output SW1 (Pin 13) is controlled by Bit 46 as given in Table 17.

Table 17. Switching Output

SW1	B46
High	0
Low	1

REMARK: SW1 is an open-drain output.

Figure 5. Internal Components at SW1



SW2/AGC (Pin 11)

The Pin SW2/AGC works as a switching output (open drain, Pin 11) or as an AM AGC-control pin to control the cascade stage of an external AM-preamplifier.

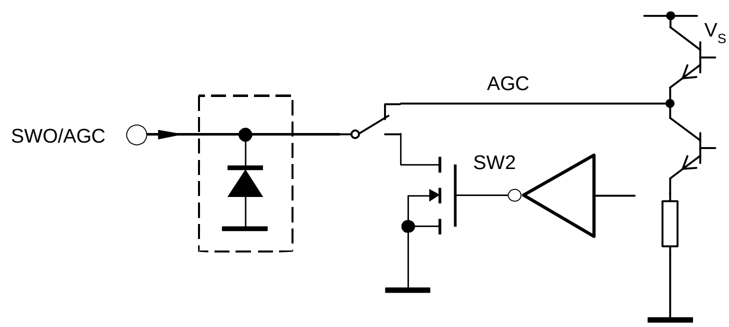
The SW2/AGC is controlled by Bits 47 and 48 as given in Table 18.

Table 18. Switching Output 2 / AGC Mode

SW2/AGC	B48	B47
AGC function	0	X
High	1	0
Low	1	1

REMARK: In AGC mode, the output voltage is 6 V down to 1 V.

Figure 6. Internal Components at SW2/AGC



Test Mode

A special test mode is implemented for final production test only. This mode is activated by setting Bit 123 = 1. This mode is not intended to be used by customer application. For normal operation Bit 123 has to be set to 0.

Table 19. Test Mode

Test Mode	B123
ON	1
OFF	0

AM Mixer

The AM mixer is used for up-conversion of the AM reception frequency to the IF frequency. Therefore, an AM prescaler is implemented to generate the necessary LO frequency from the VCO frequency.

The VCO divider can be controlled by the Bits 140 to 143 as given in Table 20.
(The VCO divider is only active in AM mode)

Table 20. Divider Factor of the AM Prescaler

Divider AM Prescaler	B143	B142	B141	B140
Divide by 2	0	0	0	0
Divide by 3	0	0	0	1
Divide by 4	0	0	1	0
Divide by 5	0	0	1	1
Divide by 6	0	1	0	0
Divide by 7	0	1	0	1
Divide by 8	0	1	1	0
Divide by 9	0	1	1	1
Divide by 10	1	x	x	x

FM Mixer

In the FM mixer stage, the FM reception frequency is down-converted to the IF frequency. The VCO frequency is used as LO frequency for the mixer.

PLL Loop Filter

The PLL loop filter selection for AM and FM mode can be controlled by Bit 145 as given in Table 21.

Table 21. Loop Filter Operating Mode

PDAM/PDFM	B145
PDFM active	0
PDAM active	1

Fractional Mode

The activated fractional mode (Bit 144 = 0) in connection with the direct shift (Bit 32 = 0) allows fast frequency changes (with the help of the 2-bit shift) with a four times higher step frequency. After the frequency change, the normal step frequency is active again.

If the fractional mode is deactivated (Bit 144 = 1) and direct shift mode is active, (Bit 32 = 0) the VCO frequency is set to the next lower frequency which is many times the amount frequency of 4 times step frequency. This means that the 2 shifted bits of the active N-Divider are not used in this mode. The shift bits are interpreted as logic 0.

The fractional mode with direct shift mode deactivated (Bit 32 = 1) allows normal frequency changes with a step frequency of 12.5 kHz.

Table 22. Fractional Mode

Fractional	B144
ON	0
OFF	1

Spurious Suppression

In fractional and direct shift mode the spurious suppression is able by SW wire and SW impulse.

Table 23. Spurious Suppression by SW Wire

SW Wire	B60
OFF	0
ON	1

Table 24. Spurious Suppression by Correction Current Charge Pump

SW Impulse	B61
OFF	0
ON	1

Charge Pump (AMLF/FMLF)

AMLF/FMLF is the current charge pump output of the PLL. The current can be controlled by setting the Bits 62 and 63. The loop filter has to be designed correspondingly to the chosen pump current and the internal reference frequency.

During the frequency change, the high-current charge pump (Bit 62) is active to enable fast frequency changes. After the frequency change, the current will be reduced to guarantee a high S/N ratio. The low-current charge pump (Bit 63) is then active. The high current charge pump can also be switched off by setting the bits of the active HCDEL register to 0 (Bit 20 and Bit 21 [HCDEL 1] or Bit 22 and Bit 23 [HCDEL 2]).

The current of the high-current charge pump is controlled by Bit 62 as given in Table 25.

Table 25. High-current Charge Pump

High-current Charge Pump	B62
1 mA	0
2 mA	1

The current of the low-current charge pump is controlled by Bit 63 as given in Table 26.

Table 26. Low-current Charge Pump

Low Current Charge Pump	B63
50 µA	0
100 µA	1

External Voltage at AMLF (Oscillator)

The oscillator (Pin 22) can be switched on/off by Bit 65. It is possible to use the oscillator buffer as an input or as an output. At the AMLF (Pin 17), an external tuning voltage can be applied (Bit 65 = 0). If this is not done, the IC operates in standard mode (Bit 65 = 1).

The oscillator, oscillator buffer and the AMLF are controlled by the Bits 65 and 64 as given in Table 27.

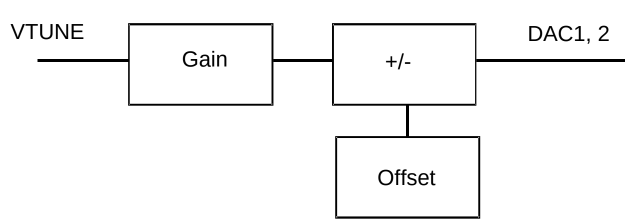
Table 27. Oscillator Operating Modes

Oscillator	Oscillator Buffer	AMLF (Pin 17)	B65	B64
OFF	INPUT	INPUT f. DAC's	0	X
ON	OFF	AMLF (standard)	1	0
ON	OUTPUT	AMLF (standard)	1	1

DAC1, 2 (Pins 1, 2)

For automatic tuner alignment, the DAC1 and DAC2 of the IC can be controlled by setting gain and offset values. The principle of the operation is shown in Figure 7. The gain is in the range of $0.67 \times V_{Tune}$ to $2.09 \times V_{Tune}$. The offset range is +0.98 V to -0.98 V. For alignment, DAC1 and DAC2 are connected to the varicaps of the preselection filter and the IF filter. For alignment, offset and gain are set for having the best tuner tracking.

Figure 7. Block Diagram of DAC1, 2



The gain of DAC1 and DAC2 has a range of approximately 0.67 × V(VTUNE) to 2.09 × V(TUNE). This range is divided into 255 steps. One step is approximately (2.09-0.67)/255 = 0.00557 × V(TUNE). The gain of DAC1 can be controlled by the Bits 38 to 45 (2^0 to 2^7) and the gain of DAC2 can be controlled by the Bits 66 to Bit 73 (2^0 to 2^7) as given in Table 28.

Table 28. Gain of DAC1, 2

Gain DAC1 Approximately	B45	B44	B43	B42	B41	B40	B39	B38	Decimal Gain
Gain DAC2 Approximately	**B73**	**B72**	**B71**	**B70**	**B69**	**B68**	**B67**	**B66**	**Decimal Gain**
0.6728 × V(TUNE)	0	0	0	0	0	0	0	0	0
0.6783 × V(TUNE)	0	0	0	0	0	0	0	1	1
0.6838 × V(TUNE)	0	0	0	0	0	0	1	0	2
0.6894 × V(TUNE)	0	0	0	0	0	0	1	1	3
...	...	...	...	...	...	...	...	...	...
0.9959 × V(TUNE)	0	0	1	1	1	0	1	0	58
...	...	...	...	...	...	...	...	...	...
2.0821 × V(TUNE)	1	1	1	1	1	1	0	1	253
2.0877 × V(TUNE)	1	1	1	1	1	1	1	0	254
2.0932 × V(TUNE)	1	1	1	1	1	1	1	1	255

Offset = 64 (intermediate position)

The offset of DAC1 and DAC2 has a range of approximately +0.98 V to -0.99 V. This range is divided into 127 steps. One step is approximately 1.97 V/127 = 15.52 mV. The offset of DAC1 can be controlled by the Bits 24 to Bit 30 (2^0 to 2^6) and the offset gain of DAC2 can be controlled by the Bits 52 to Bit 58 (2^0 to 2^6) as given in Table 29.

Table 29. Offset of DAC1, 2

Offset DAC1 Approximately	B30	B29	B28	B26	B26	B25	B24	Decimal Offset
Offset DAC2 Approximately	**B58**	**B57**	**B56**	**B55**	**B54**	**B53**	**B52**	**Decimal Offset**
0.9815 V	0	0	0	0	0	0	0	0
0.9659 V	0	0	0	0	0	0	1	1
0.9512 V	0	0	0	0	0	1	0	2
0.9353 V	0	0	0	0	0	1	1	3
...		...	...	...	...	...	...	...
-0.0120 V	1	0	0	0	0	0	0	64
...		...	...	...	...	...	...	...
-0.9576 V	1	1	1	1	1	0	1	125
-0.9733 V	1	1	1	1	1	1	0	126
-0.9890 V	1	1	1	1	1	1	1	127

Gain = 58 (intermediate position)

Permitted DAC Conditons

The internal operation amplifier of the DACs should not operate with a too high internal difference voltage at their inputs. This means that a voltage difference higher than 0.5 V at the internal OP input should be avoided in operation mode. The respective output OP in the DAC is necessary for the addition and amplification of the tuning voltage (at pin 18) with the desired voltage gain and offset value.

If the tuning voltage reaches a high value e.g. 9 V, with a gain setting of 2 times V_{Tune} and an offset of +1 V, then the output OP of the DAC should reach the (calculated) voltage of 19 V. The supply voltage of e.g. 10 V, however, limits the output voltage (of the DAC) to 10 V maximum.

Due to the (limiting) supply voltage and the internal gain resistance ratio of 6 , the missing 9 V (calculated voltage - V_s) cause a voltage of 1.5 V at the OP input. This condition may not remain for a longer period of time.

As long as the calculated DAC output voltage value does not exceed the supply voltage value by more than 3 V, no damages should occur during the product's lifetime as the input voltage of the internal OP input voltage does not exceed 0.5 V.

V_{Tune} x DAC gain factor + DAC offset < Vs + 3 V

(9 V x 2 + 1 V) < 10 V + 3 V (condition not allowed)

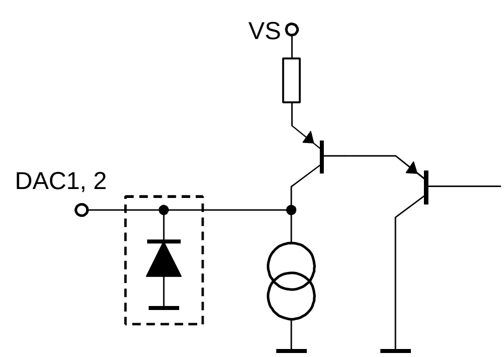
This means when having a gain factor of 2 and an offset value of 1 V, the tuning voltage should not exceed 6 V.

Maximum tuning voltage < (V_S + 3 V - DAC offset) / DAC gain factor

e.g.: maximum tuing voltage = (10 V + 3 V - 1 V) / 2 = 6 V

It is also possible to reduce the gain or the offset value instead of (or along with) the tuning voltage.

Figure 8. Internal Components of DAC1, 2

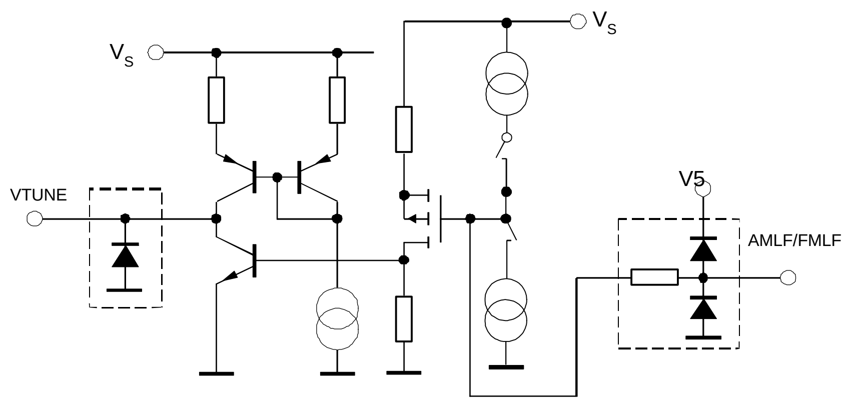


Input/Output Interface Circuits

VTUNE, AMLF and FMLF (Pins 16-18)

VTUNE is the loop amplifier output of the PLL. The bipolar output stage is a rail-to-rail amplifier.

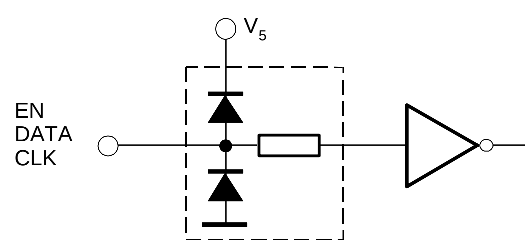
Figure 9. Internal Components at V_{Tune}, AMLF and FMLF



EN, DATA, CLK (Pins 23-25)

All functions can be controlled via a 3-wire bus consisting of Enable, Data and Clock. The bus is designed for microcontrollers which can operate with 3-V supply voltage. Details of the data transfer protocol can be found in the chapter “3-Wire Bus Description”.

Figure 10. Internal Components at Enable, Data and Clock



Application Information

PLL Concept of U4257BM

The PLL architecture of the T4260 allows a fast tuning response time of approximately 1 ms, for a jump over the FM band of 87.5 MHz to 108 MHz, with a phase detector frequency (f_{PDF}) of 12.5 kHz in FM mode. This fast response time with the small f_{PDF} frequency is achieved by a patented three-PLL concept.

The functional blocks are listed below.

DPLL1 (PLL1)

DPLL1 is a digital PLL and consists out of the following stages:

14-bit R-Divider
18-bit N-Divider
PFD (Phase Frequency Detector)
Charge pump (50 µA to 2000 µA)
Active loop amplifier
Lock detector

Fractional PLL (PLL2)

This is a fractional PLL with a 2-bit wide accumulator and consists out of the following stages:

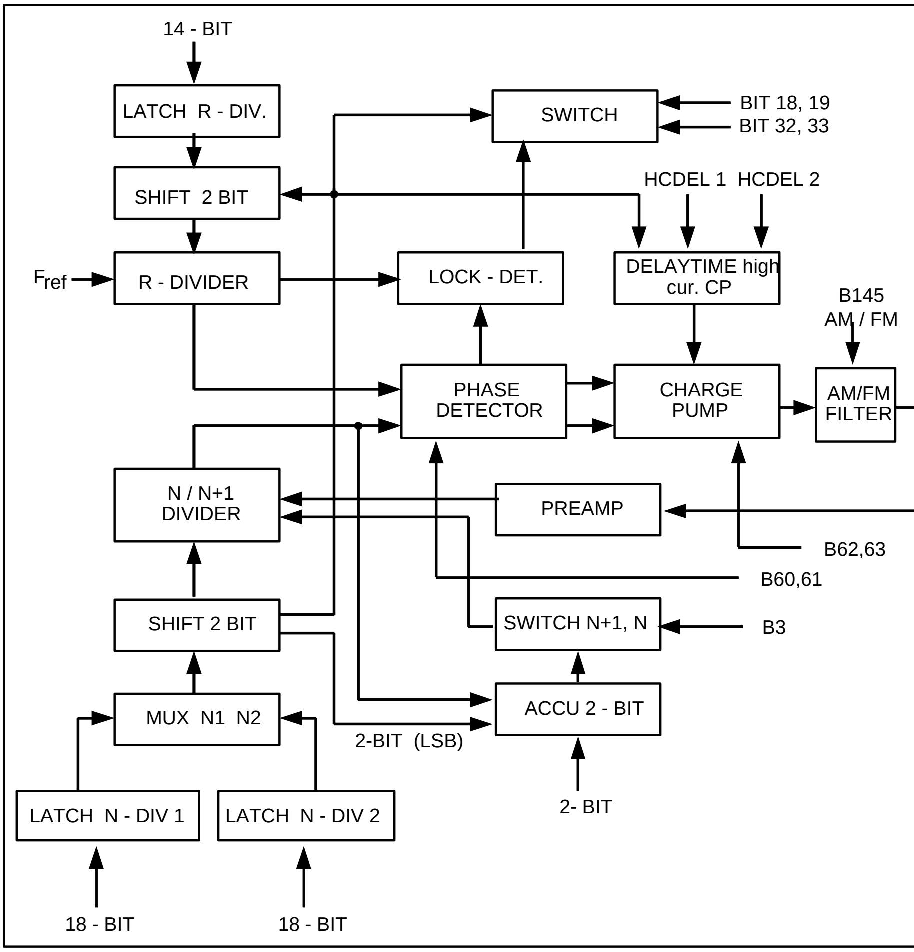
12-bit R-Divider
16-bit N/N+1-Divider
PFD (Phase Frequency Detector)
Charge pump (50 µA to 2000 µA)
2-bit accumulator
Active loop amplifier
Lock detector

DPLL2 (PLL3)

DPLL2 is a digital PLL containing the following stages:

12-bit R-Divider
16-bit N-Divider
PFD (Phase Frequency Detector)
Charge pump (50 µA to 2000 µA)
Active loop amplifier
Lock detector

Figure 11. Block Diagram of the PLL Core



High-speed Tuning Concept

If the PLL core operates in locked mode, PLL1 (DPLL1) is active (tuned function mode). In this mode, a high S/N ratio is provided, but the lock time is approximately 4 ms with f_{PDF} = 12.5 kHz (f_{PDF} is the phase-detector frequency) and Pd_{cu} = 2 mA (Pd_{cu} is the charge pump current). For a fast tuning response, PLL2 (fractional PLL) or PLL3 (DPLL2) is used during the tuning time. The switch between the PLLs is controlled via the lock-detect signal or with a 3-wire-bus protocol. In the lock-detect controlled mode all function blocks are switched automatically, so no software protocols are necessary. In the PLL2 and PLL3 mode, the f_{PDF} of 12.5 kHz is multiplied by four (f_{PDF} = 50 kHz). Due to the higher f_{PDF} frequency, a faster lock time is possible (approximately 1 ms for a tune from 98 MHz to 118 MHz).

The higher f_{PDF} for PLL2 and PLL3 is achieved by shifting the bits for N/R-divider two bits right. The bits are shifted simultaneously and synchronized with the phase-detector status. This shift is comparable with a f_{PDF} frequency multiplication by four. PLL2, the fractional PLL, uses the two shifted bits of the N-divider for the fractional control. These bits are needed in the accumulator to control the N/N+1-divider control signal. In PLL3 mode the two LSB bits of the N/R-divider are not used, so an offset of the output frequency may occur.

Control of Functions

All functions are controlled via 3-wire-bus protocols. The privileged control set is the lock-detect controlled mode for the PLL1 during lock time and PLL2 during tuning time. This function can be set by Bit 144 = 0 and Bit 33 = 1. Bits 18, 19, 32, 33 and 144 are the function mode bits. A detailed description of the bits meaning is found in the 3-wire-bus description.

For the calculation of the R/N-divider values, the PLL1 mode is valid, e.g., if the f_{ref} (reference frequency) in FM mode is f_{ref} = 150 kHz, the R-divider for f_{PDF} = 12.5 kHz is 150 kHz/ 12.5 kHz = 12. If the receiving frequency is f_{rec} = 98 MHz, the N-divider is (98 MHz + f_{IF})/ 12.5 kHz = 8695.

If the R-divider is shifted by two to the right, the R-divider is 3 and f_{PDF} is 50 kHz. If the N-divider is shifted by two bits to the right, the N-divider is 2173 and f_{rec} is 97.9625 MHz. This output frequency is valid if PLL3 is used. In case of PLL2, the two LSB of the N-divider are used for fractional control and the frequency f_{rec} is then 98 MHz.

REMARK: f_{IF} = 10.6875 MHz

High-speed Tuning

The fractional mode (Bit 144 = 0) in connection with the direct shift mode (Bit 32 = 0) allows very fast frequency changes with four times the step frequency (50 kHz $= 4 \times f_{PDF}$) at low frequency steps (e.g., f_{PDF} = 12.5 kHz). In direct shift mode, the R- and the N-divider are shifted by 2 bits to the right (this corresponds to a R- and N-divider division by 4 or a step frequency multiplication by 4).

Due to the 2-bit shift, a faster tuning response time of approximately 1 ms instead of 3-4 ms for a tune over the whole FM band from 87.5 MHz to 108 MHz is possible with f_{PDF} = 12.5 kHz.

If the FM receiving frequency is 103.2125 MHz (with e.g. f_{PDF} = 12.5 kHz and f_{IF} = 10.7 MHz), an N-divider of 9113 and an R-divider of 12 are necessary when using a reference-frequency (fref) of 150 kHz.

$$f_{VCO} = f_{IF} + f_{rec} = 10.7\ \text{MHz} + 103.2125\ \text{MHz} = 113.9125\ \text{MHz}$$

$$f_{PDF} = f_{VCO} / N = f_{ref} / R = 113.9125\ \text{MHz} / 9113 = 150\ \text{kHz} /12 = 12.5\ \text{kHz}$$

An important condition for the use of the fractional mode is an R-divider with an integer value after the division by 4 (R-dividers have to be a multiple of 4).

After a 2-bit shift (divider division by 4), the R-divider is now 3 (instead of 12) and the N-divider is 2278.25 (instead of 9113). The new N-divider of 2278.25 is also called ¼ fractional step because the modulo value of the N-divider is 0.25 = ¼. In total, there are 4 different fractional 2-bit shift steps: full, ¼, ½ and ¾ step.

If the fractional mode is switched off (Bit 144 = 1) during direct shift mode (Bit 32 = 0), the modulo value of the N-divider will be ignored (the new N-divider is then 2278 instead of 2278.25). This means that the PLL locks on the next lower multiple frequency of $4 \times f_{PDF}$ (in our case f_{PDF} = 12.5 kHz). The new VCO frequency (f_{VCO}) is then 113.9 MHz (instead of 113.9125 MHz in fractional mode).

Also the PLL has additionally a special fractional logic which allows a good spurious suppression in the fractional and direct shift mode. Activating the wire switch (Bit 60 = 1) and the correction charge pump (Bit 60 = 1) the spurious suppression is active.

Charge Pump Current Settings

Bit 62 (0 = 1 mA; 1 = 2 mA) allows to adjust the high current, which is active during a frequency change (if the delay time of the active HCDEL register is not switched off). A high charge pump current allows faster frequeny changes. After a frequency change, the current reduction is reduced (in locked mode) to the low current which is set by bit 63 (0 = 50 µA; 1 = 100 µA). A lower charge pump current guarantees a higher S/N ratio.

The high current charge pump can be switched off by the active HCDEL register bits. In this case, when HCDEL 1 is active and the bits 20 and 21 are 0 (HCDEL 1 delay time = off) or HCDEL 2 is active and the bits 22 and 23 are 0 (HCDEL 2 delay time = off), only the low current charge pump (current) is active in locked and in the frequency change mode.

AM Prescaler (Divider) Settings

The AM mixer is used for up-conversion of the AM reception frequency to the IF frequency. Therefore, an AM prescaler is implemented to generate the necessary LO from the VCO frequency. For the reception of the AM band, different prescaler (divider) settings are possible.

Table 30 lists the AM prescaler (divider) settings and the reception frequencies.

f_{VCO} = 98.2 MHz to 124 MHz

f_{IF} = 10.7 MHz

$f_{rec} = f_{VCO} - f_{IF}$

f_{VCO} = AM prescaler x $(f_{rec} + f_{IF})$

The following formula can also be useful by AM frequencies higher than 20 MHz:

f_{VCO} = AM prescaler x $(f_{rec} - f_{IF})$

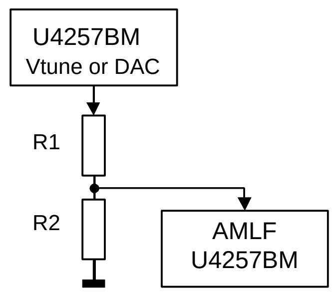
Table 30. AM Prescaler (Divider) Settings and the Reception Frequencies

Divider (AM Prescaler)	Minimum Reception Frequency [MHz]	Maximum Reception Frequency [MHz]
no divider	87.5	113.3
Divide by 2	38.4	51.3
Divide by 3	22.033	30.633
Divide by 4	13.85	20.3
Divide by 5	8.94	14.1
Divide by 6	5.667	9.967
Divide by 7	3.329	7.014
Divide by 8	1.575	4.8
Divide by 9	0.211	3.078
Divide by 10	0	1.7

External Voltage at AMLF (Pin 17)

By using two ICs, for example, it is possible to operate the AMLF (Pin 17) of the second IC either with the tuning voltage (Vtune [Pin 18]), the DAC 1 voltage [Pin 1] or the DAC 2 voltage [Pin 2] from the first T4260. For voltage reduction at the AMLF [Pin 17], a voltage factor ratio of 100/16 (R1/R2) is required.
This means that an applied voltage from 0.5 V at Pin 17 (AMLF) corresponds to a tuning voltage of 3.625 V.
It is recommended to use R1 with 100 kΩ and R2 with 16 kΩ. The allowed range of R1 is 10 kΩ to 1 MΩ and 1.6 kΩ to 160 kΩ for R2.

Figure 12. External Voltage at AMLF (Pin 17)



The maximum input voltage at the AMLF input (pin 17) depends on the applied supply voltage as well as on the gain and offset settings. To avoid any damages during the product's lifetime, the following formulas regarding SWAMLF voltage, gain and offset settings have to be observed (see also chapter Permitted DAC Conditions).

V_{SWAMLF} x ([R1 + R2] / R2) x DAC gain factor + DAC offset < V_S + 3 V

(R1 + R2) / R2 = 7.25

This means when having a gain factor of 2 and an offset value of 1 V, the applied SWAMLF voltage should be limited to a voltage lower than 0.83 V.

SWAMLF voltage < (V_S + 3 V - DAC offset) / (DAC gain factor x 7.25)

e.g.: maximum SWAMLF voltage = (10 V + 3 V - 1 V) / (2 x 7.25) = 0.83 V

It is also possible to reduce the gain or offset instead (or along with) the SWAMLF voltage.

Figure 13. Test Circuit

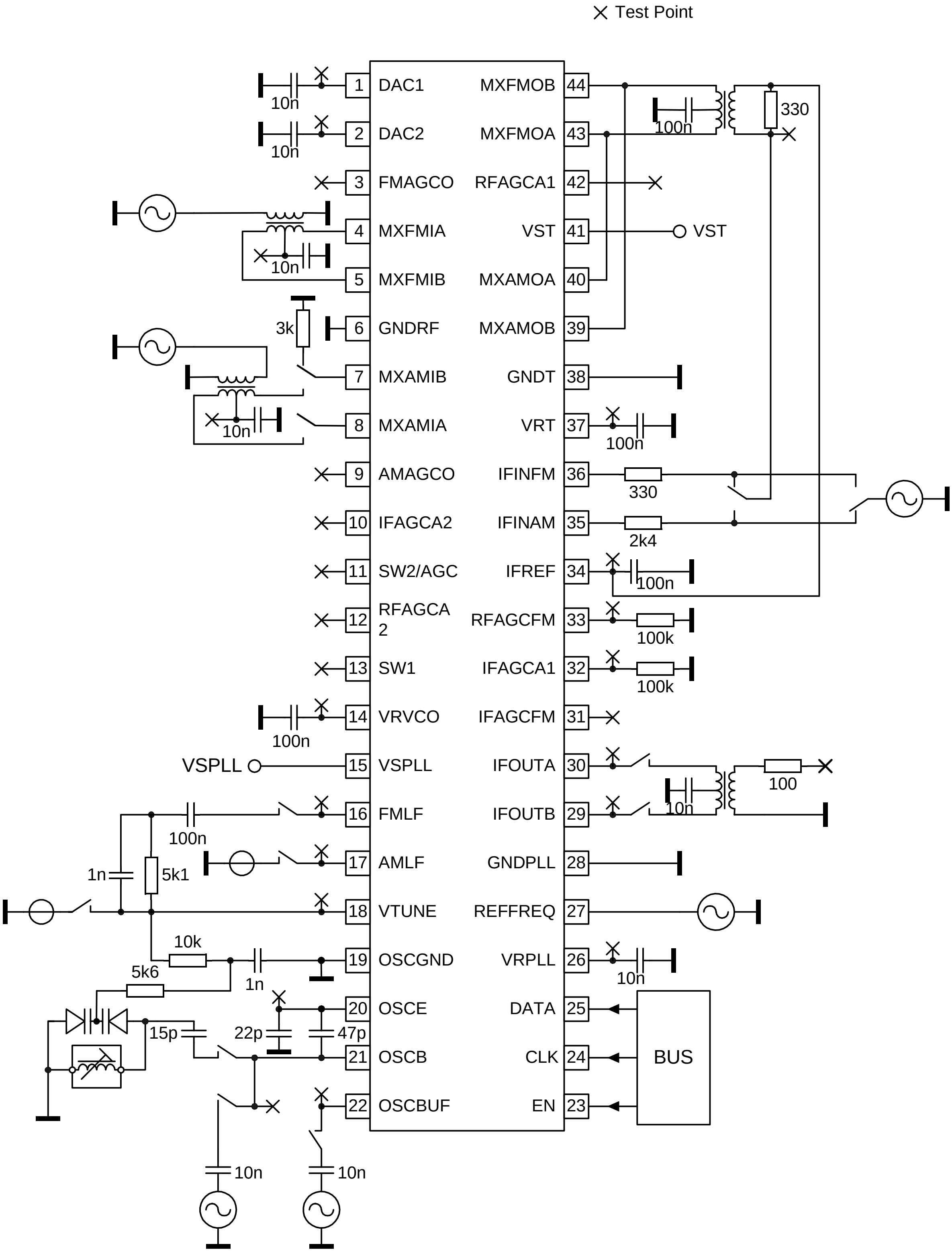
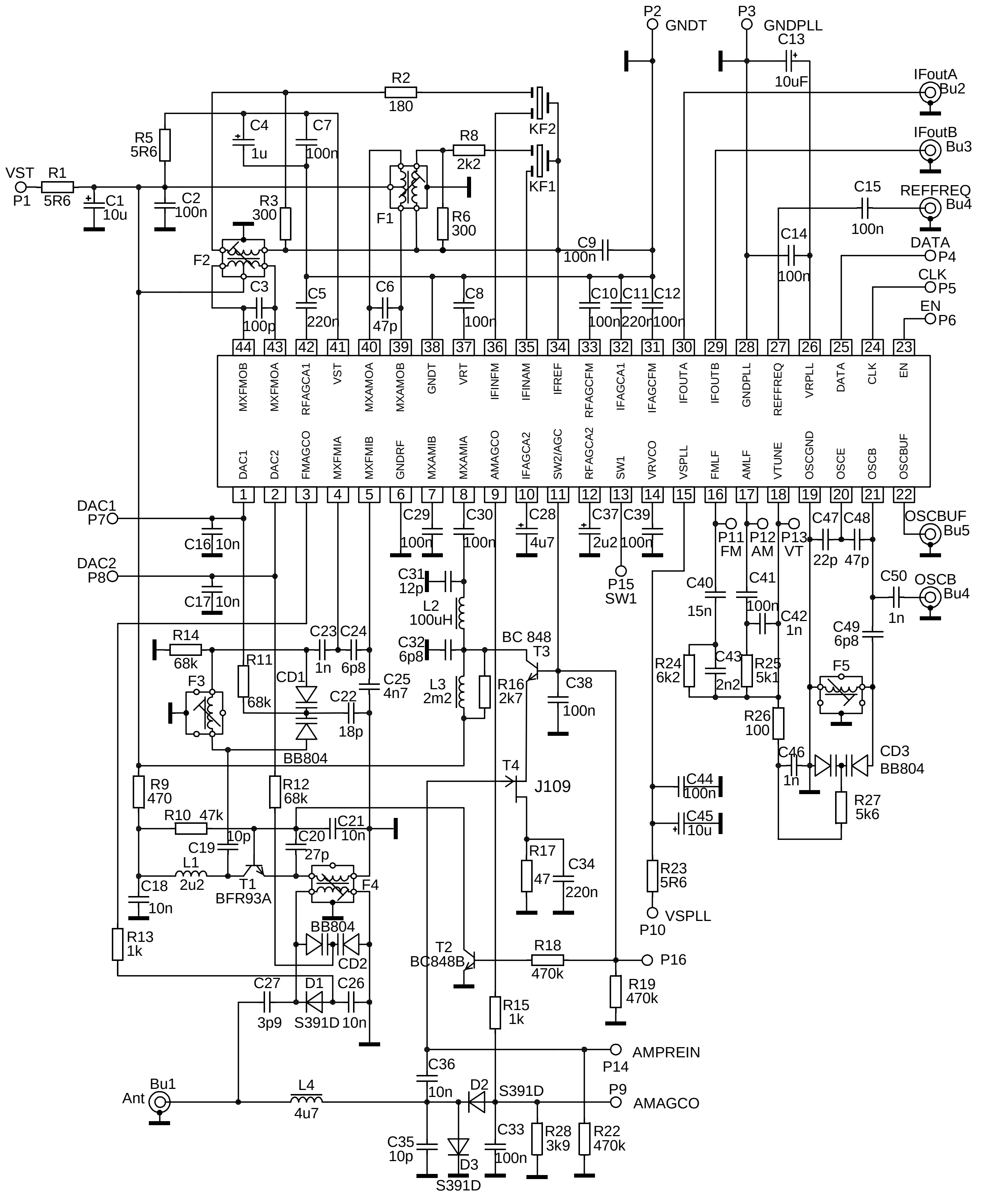


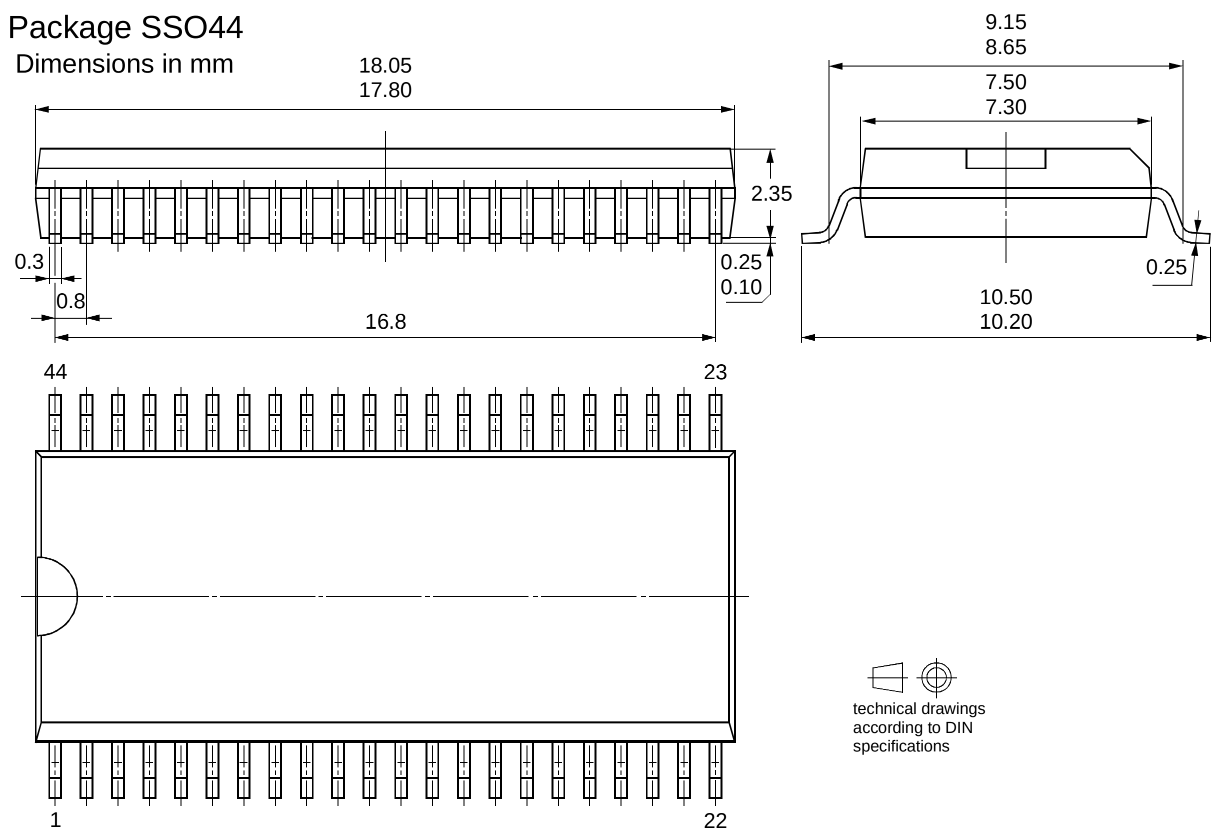
Figure 14. Application Circuit



Ordering Information

Extended Type Number	Package	Remarks
T4260IL	SSO44	Tube
T4260ILQ	SSO44	Taped and reeled

Package Information



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