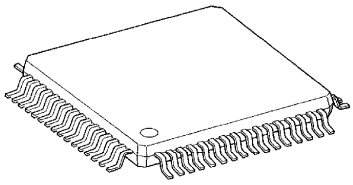
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB6513AF

VIDEO CAMERA CYLINDER MOTOR CONTROLLERS AND CAPSTAN MOTOR CONTROLLERS

The TB6513AF is a single-chip IC for video camera cylinder motor controllers and capstan motor controllers. The cylinder section is a soft-switching pre-driver based on 3 phase full-wave sensorless drive and 180°-trapezoidal wave drive control. The capstan section is a soft-switching predriver based on 3 phase full-wave drive and pseudo-sine wave drive control.



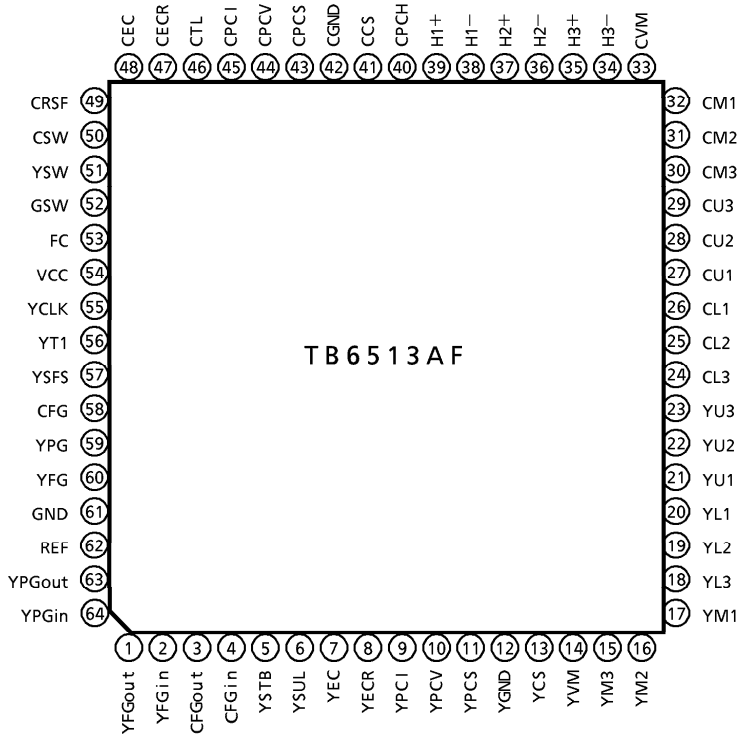
LQFP64-P-1010-0.50A

Weight : 0.34g (Typ.)

FEATURES

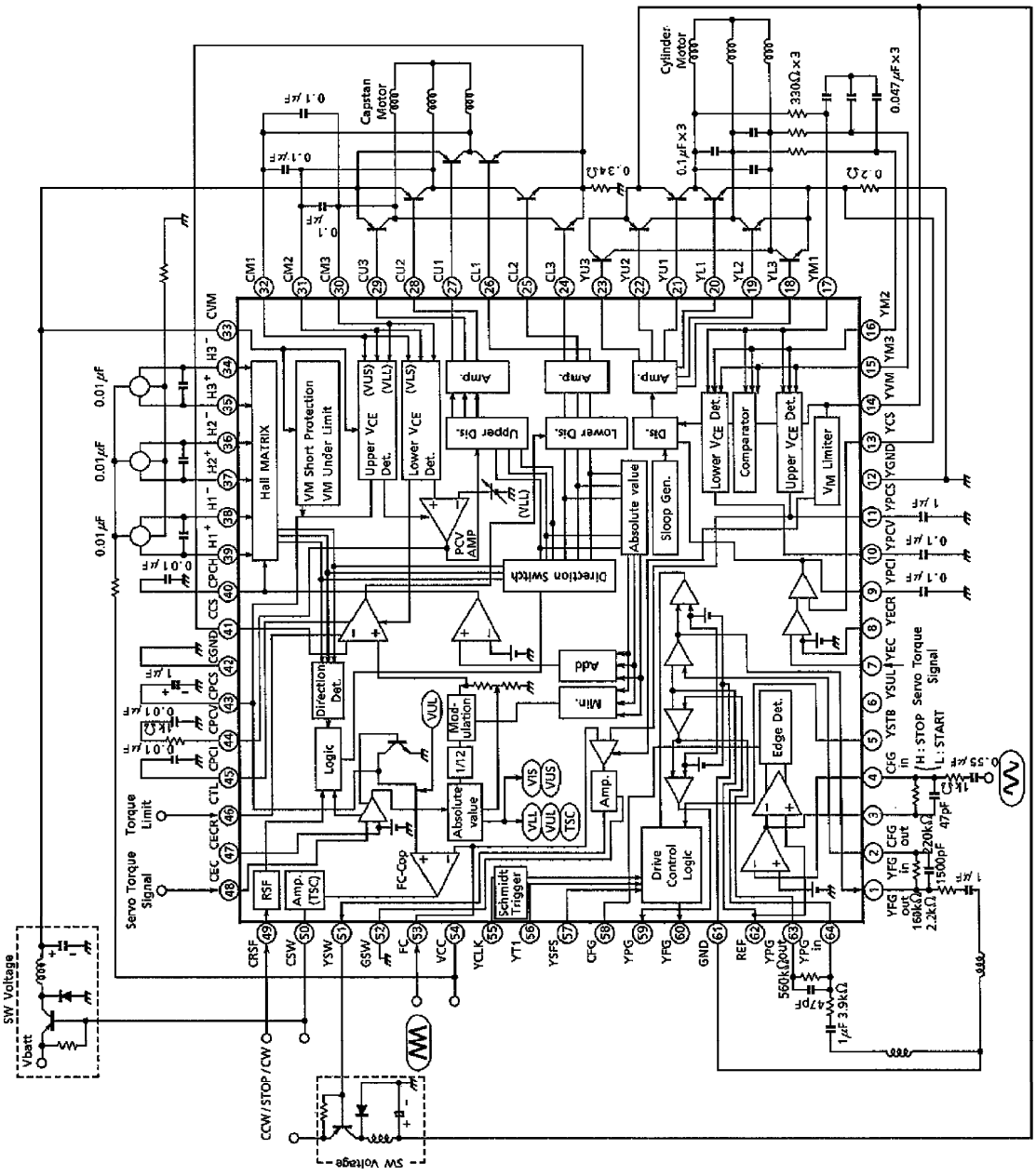
- Output Current : 10mA (MIN.) (at V_{CC} = 3.5V)
- Operating Voltage : V_{CC} = 3.0V~5.5V
- Output Voltage : V_M = 3.0~12V

PIN CONNECTION



961001EBA2

BLOCK DIAGRAM



TB6513AF – 2

961001EBA2'

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	YFGout	Cylinder part FG Amp. output terminal
2	YFGin	Cylinder part FG Input terminal
3	CFGout	Capstan part FG Amp. output terminal
4	CFGin	Capstan part FG Input terminal
5	YSTB	Cylinder part Stand-by Switch Input terminal
6	YSUL	Cylinder part Sloop Voltage terminal
7	YEC	Cylinder part Torque control Input terminal
8	YECR	Cylinder part torque control reference voltage Input terminal
9	YPCI	Cylinder part current feedback phase compensation
10	YPCV	Cylinder part voltage feedback phase compensation
11	YPCS	Cylinder part switching voltage control output terminal
12	YGND	Cylinder part GND terminal
13	YCS	Cylinder part current detective
14	YVM	Cylinder Motor Power Voltage terminal
15	YM3	Cylinder Moter Coil terminal
16	YM2	〃
17	YM1	〃
18	YL3	Cylinder Motor Low side Pre driver output terminal
19	YL2	〃
20	YL1	〃
21	YU1	Cylinder Motor Upper side Pre driver output terminal
22	YU2	〃
23	YU3	〃
24	CL3	Capstan Motor Low side Pre driver output terminal
25	CL2	〃
26	CL1	〃
27	CU1	Capstan Motor Upper side Pre driver output terminal
28	CU2	〃
29	CU3	〃
30	CM3	Capstan Motor Coil terminal
31	CM2	〃
32	CM1	〃
33	CVM	Capstan Motor Power voltage terminal

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
34	H3−	Capstan Motor Hall element Input terminal
35	H3+	〃
36	H2−	〃
37	H2+	〃
38	H1−	Capstan Motor Hall element Input terminal
39	H1+	〃
40	CPCH	Capstan part Hall Amp. phase compensation
41	CCS	Capstan part current detective input terminal
42	CGND	Capstan part GND terminal
43	CPCS	Capstan part switching voltage control terminal
44	CPCV	Capstan part voltage feedback phase compensation
45	CPCI	Capstan part current feedback phase compensation
46	CTL	Capstan part torque Limit
47	CECR	Capstan part torque control reference voltage
48	CEC	Capstan part torque control input terminal
49	CRSF	Capstan part direction control input terminal
50	CSW	Capstan part switching pre driver output terminal
51	YSW	Cylinder part switching pre-driver output terminal
52	GSW	Switching voltage part GND terminal
53	FC	Switching comparator triangular-wave input terminal
54	VCC	Power voltage supply terminal for Logic
55	YCLK	Cylinder part clock input terminal
56	YT1	Cylinder part testmode switch input terminal
57	YSFS	Cylinder part start frequency selecter
58	CFG	Capstan part FG wave output terminal
59	YPG	Cylinder part PG wave output terminal
60	YFG	Cylinder part FG wave output terminal
61	GND	FG, PG part GND terminal
62	REF	FG, PG part reference voltage terminal
63	YPGout	Cylinder part PG Amp. output terminal
64	YPGin	Cylinder part PG input terminal

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	6	V
Motor Supply Voltage	(Note 1)	V_M	14	V
Supply Input / Output Voltage	(Note 2)	V_{SWB}	14	V
Output Terminal Voltage	(Note 3)	V_N	14	V
Input Terminal Voltage	(Note 4)	V_I	− 0.3 ~V_{CC} + 0.3	V
Power Dissipation		P_D	0.95 (Note 5)	W
Operating Temperature		T_{opr}	− 20~75	°C
Storage Temperature		T_{stg}	− 55~125	°C

(Note 1) Pin No. = 14, 33
(Note 2) Pin No. = 50, 51
(Note 3) Pin No. = 15, 16, 17, 21, 22, 23, 27, 28, 29, 30, 31, 32
(Note 4) Pin No. = 2, 4, 5, 7, 8, 13, 41, 46, 47, 48, 49, 53, 55, 56, 57, 62, 64
(Note 5) NO HEAT SHINK

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{CC} = 3.5V)
Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1	Supply Current (1)	$I_{CC\,(1)}$	1	Operational, Cylinder, Capstan part	—	17.9	30	mA
2	Supply Current (2)	$I_{CC\,(2)}$	1	STB mode STOP (CAP) mode	—	10.6	20	mA
3	ECR Voltage	V_{ECR}	1		2.14	2.24	2.54	V
4	Torque Control Input Current	YI_{EC}	1	YEC = 0V	− 5	− 0.5	—	μA
5	Torque Cont, Input Offset Voltage	ΔEC	2		− 100	− 15	100	mV
6	Input / Output Gain	YGio	2		0.13	0.15	0.17	
7	Max Output Voltage	YCSmax	2	R_{YCS} = 0.27Ω	145	160	183	mV
8	Lower Side Output Voltage (1)	$V_{L\,(1)}$	3	YCS = 54mV	0.2	0.39	0.6	V
9	Lower Side Output Voltage (2)	$V_{L\,(2)}$	3	YECR = 2.24V, YEC = 0V	0.45	0.66	0.85	V
10	Upper Side Drive Current	I_U	4		—	—	− 10	mA
11	Lower Side Drive Current	I_L	4		10	—	—	mA
12	PCS Operation Point (1)	$V_{PCS\,(1)}$	5	YEC = YECR = 2.24V V_{PCS} = 1.75V	0.36	0.47	0.58	V
13	PCS Operation Point (2)	$V_{PCS\,(2)}$	5	YEC = 0V, YECR = 2.24V V_{PCS} = 1.75V	0.60	0.79	0.98	V
14	PCS Gain	YG_{PCS}	5		4.5	6.5	8.5	
15	SW Reg Drive Current (1)	$I_{SW\,(1)}$	5	VM1 = 6V, YEC = YECR = 2.24V	3	4.5	—	mA

Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
16	SW Reg Drive Current (2)	$I_{SW\ (2)}$	5	VM1 = 6V YEC = 0V, YECR = 2.24V	11	16.6	—	mA
17	SW Reg Comparator Offset Voltage	ΔV_{FC}	5		− 5	15	25	mV
18	FG Amp. Gain	G_{FG}	6	V_{p-p} = 1.5mV, f = 1kHz	45	—	—	dB
19	YFG High Level	YFG (H)	7	I_{YFG} = − 100μA	2.0	3.4	—	V
20	YFG Low Level	YFG (L)	7	I_{YFG} = 100μA	—	0.1	1.5	V
21	PG Amp. Gain	G_{PG}	6	V_{p-p} = 1.5mV, f = 1kHz	45	—	—	dB
22	PG Amp. Offset Voltage	ΔPGin	7		0.45	0.5	0.6	V
23	YPG High Level	YPG (H)	7	I_{YPG} = − 10μA	2.0	3.0	—	V
24	YPG Low Level	YPG (L)	7	I_{YPG} = 100μA	—	0.03	1.0	V
25	Stand-by Voltage	STB_{on}	8		2.15	—	—	V
26	Stand-by Release Voltage	STB_{off}	8		—	—	1.0	V
27	Stand-by Input Current	I_{STB}	8	V_{STB} = 0V	− 100	− 35	—	μA
28	Starting Frequency Selecter Control Voltage f = 15Hz	SFS (L)	9		—	—	1.05	V
29	Starting Frequency Selector Control Voltage f = 30Hz	SFS (H)	9		2.45	—	—	V
30	YVM Under Limit	YVML	5		1.87	2.5	3.13	V
31	YVM Short Protection	YVMS	5		0.26	0.76	1.00	V
32		I_{ML}	10	YVM = 6V	—	3	10	μA
33	Output Idel Voltage	YCSidle	2	R_{YCS} = 0.27Ω	—	0	5	mV

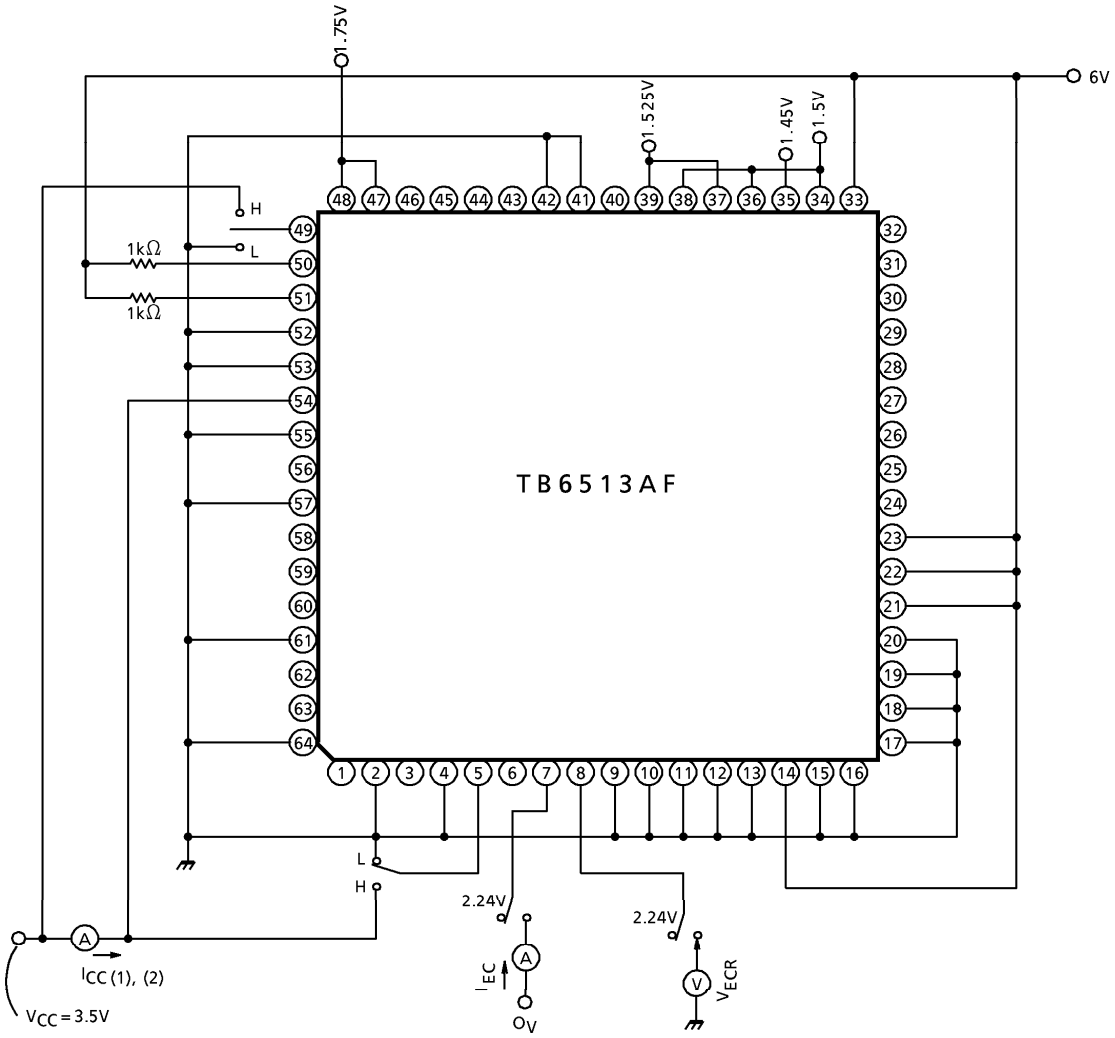
Capstan part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
34	Torque Control Input Current	CI_{EC}	11	CEC = CECR = 1.75V	− 2	− 1	—	μA
35	Torque Control Reference Voltage	CE_{CR}	11		1.55	1.73	1.95	V
36	Torque Control Input Voltage	CEC	12		0.5	—	3.0	V
37	Output MAX. Voltage	CCSmax	12	R_{CCS} = 0.34Ω	0.19	0.23	—	V
38	Torque Control Input / Output Gain	CGio	12		0.21	0.24	0.27	
39	Output Idle Voltage	CCSidle	12		—	0	4	mV
40	Torque Control Input Offset	CECofs	12		− 100	15	100	mV

Capstan part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
41	Torque Control Dead Zone	CECdz	12		30	77	130	mV
42	Low Side V_{CE} Voltage (1)	CVLL (1)	13	CCS = 60mV	0.22	0.28	0.50	V
43	Low Side V_{CE} Voltage (2)	CVLL (2)	13	CEC = 0V, CTL = 1.0V	0.40	0.50	0.80	V
44	Hall Element Input	Hin	14		1.2	—	2.0	V
45	Hall Element Input	Hofs	15		− 8	− 1	8	mV
46	TL-CS Offset	TLofs	16	CTL = 20mV	6	9.5	14	mV
47	Forward Rotation Control Voltage	Vf	17		—	—	0.87	V
48	Stop Control Voltage	Vs	17		1.27	—	2.23	V
49	Reverse Rotation Control Voltage	Vr	17		2.90	—	—	V
50	Ripple Channel	R	18	CCS = 60mV	8	8.5	18	%
51	Upper Side Drive MAX. Current	CI_U	19		10	24	—	mA
52	Low Side Drive MAX. Current	CI_L	19		—	− 16	− 10	mA
53	SW Power Voltage Input Offset	CSWofs	21		− 20	11	20	mV
54	SW Power Voltage Control Output Gain	CG_{PCS}	20		6	8	10	
55	SW Power Voltage Control Output Voltage (1)	VUD (1)	20	CEC = CECR, CPCS = 1.7V	0.3	0.40	0.65	V
56	SW Power Voltage Control Output Voltage (2)	VUD (2)	20	CEC = 0V, CTL = 0.2V CPCS = 1.7V	0.47	0.62	1.10	V
57	SW Power Voltage Output MAX. Current	CI_{SWB}	20	CEC = 0V, CTL = 0.2V	15	22	—	mA
58	FG Amp. Reference Voltage	CFG_{ref}	11		1.7	2.0	2.3	V
59	FG Amp. Loop Gain	CG_{FG}	22	External 1kΩ, 220kΩ Input $3mV_{p-p}$, 1kHz	45	50	—	dB
60	FG Amp. Output Voltage High Level	CFG_H	22		3	3.5	—	V
61	FG Amp. Output Voltage Low Level	CFG_L	22		—	0.01	0.5	V
62	V_M Under Limit	CV_{ML}	23		1.13	1.52	1.88	V
63	V_M Short Protection	CV_{MS}	23		0.26	0.45	1.00	V

TEST CIRCUIT 1. $I_{CC\,(1)}$, $I_{CC\,(2)}$, V_{ECR}, YI_{EC}



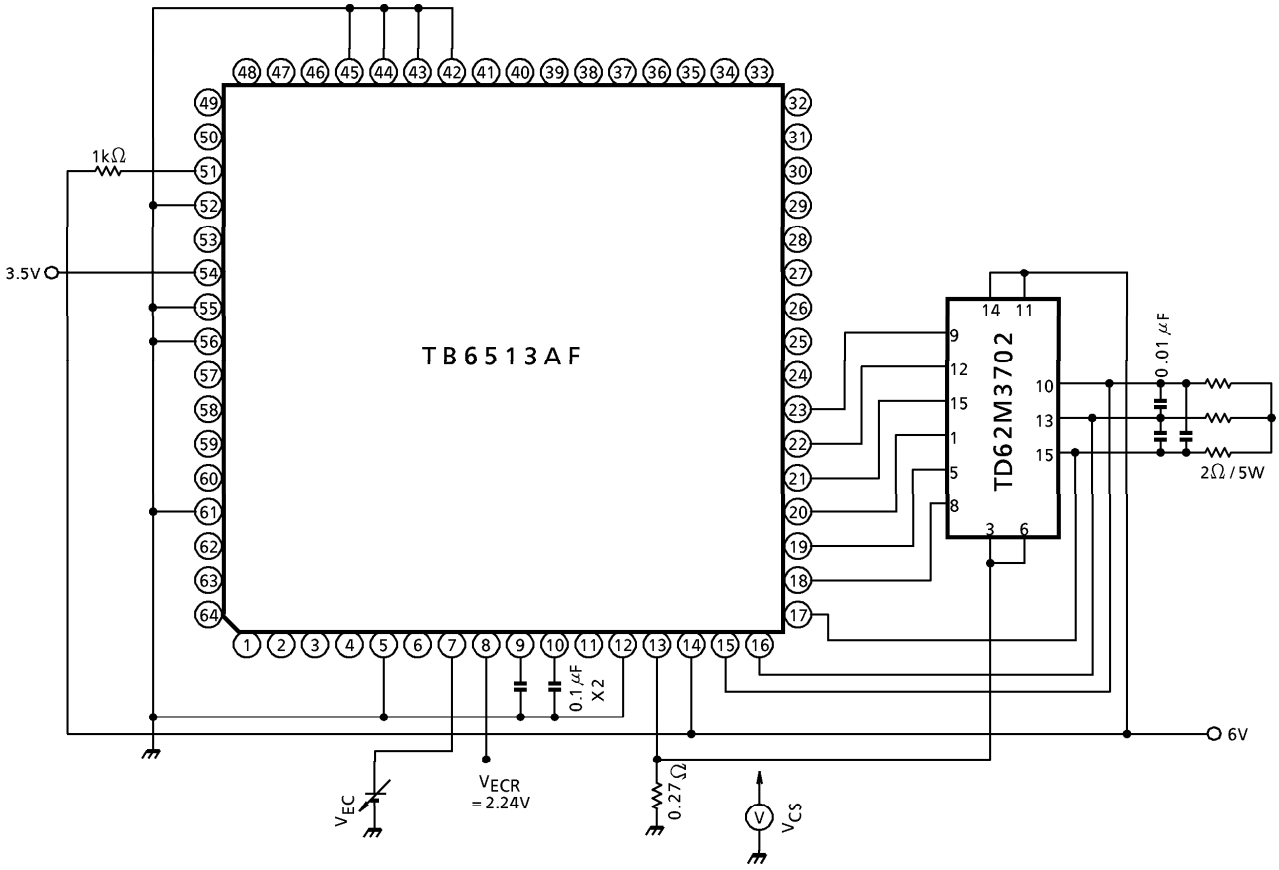
No.1 $I_{CC\,(1)}$
Set YSTB = 0V, YEC = 2.24V, YECR = 0V and CRSF = 0V, then measure the current to the V_{CC} terminal.

No.2 $I_{CC\,(2)}$
Set YSTB = 3.5V, YEC = YECR = 2.24V and CRSF = OPEN, then measure the current to the V_{CC} terminal.

No.3 V_{ECR}
Measure the potential of pin⑧.

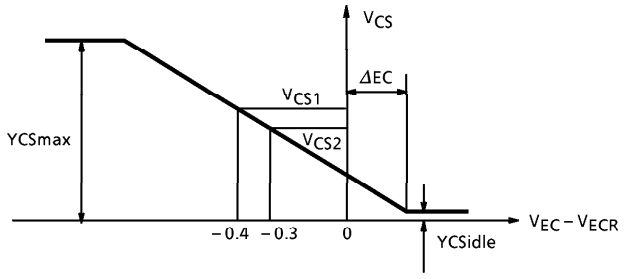
No.4 YI_{EC}
Set YEC = 0V and YECR = 2.24V, then measure the current to pin⑦.

TEST CIRCUIT 2. ΔEC, YGio, YCSmax, YCSidle



No.5 ΔEC, No.6 YGio, No.7 YCSmax, No.33 YCSidle

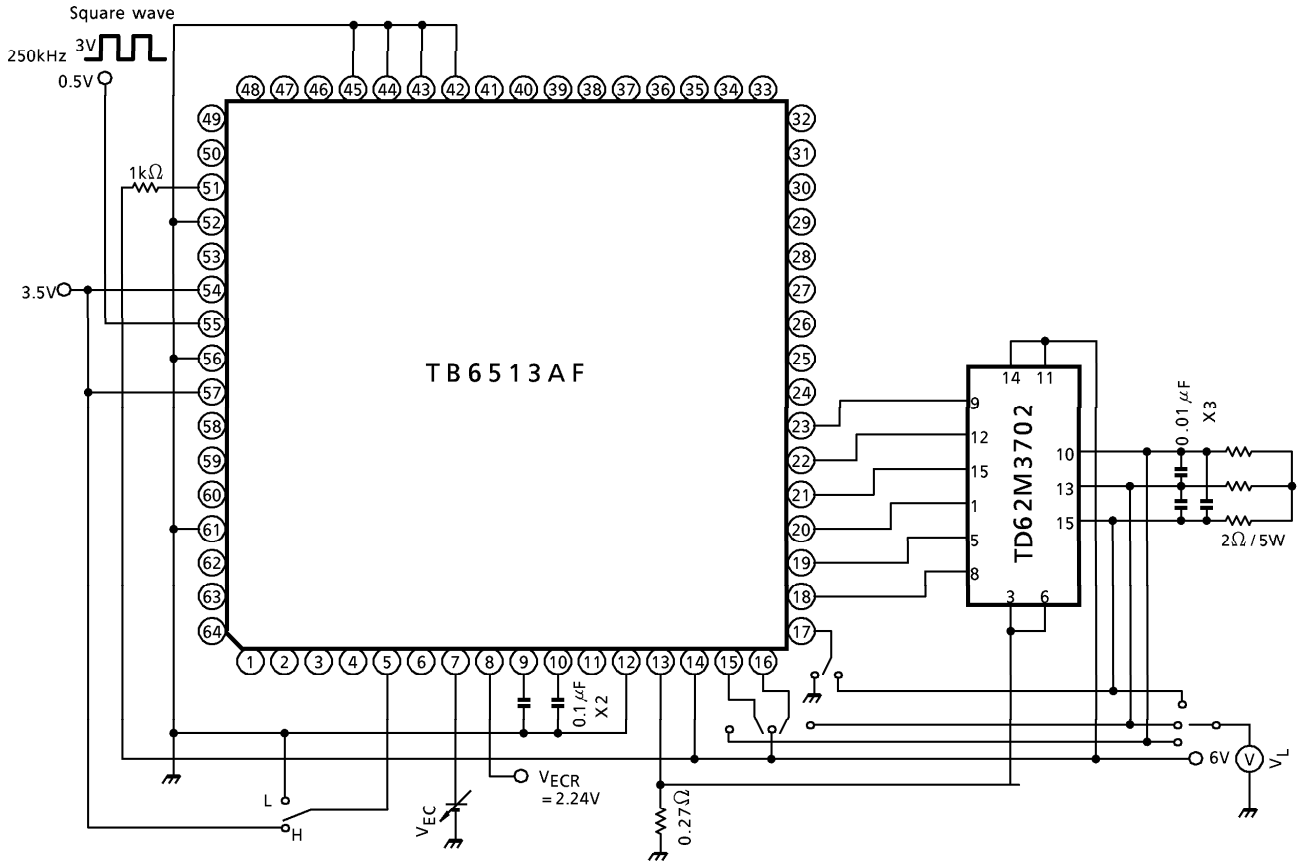
Set YECR = 2.24V, change YEC from 0V to 3V, then measure the potential of pin⑬.



$$\Delta EC = V_{EC} - V_{ECR} \quad (V_{CS} \approx 0V)$$

$$YGio = \frac{V_{CS1} - V_{CS2}}{0.1V}$$

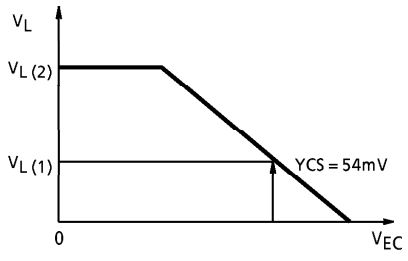
TEST CIRCUIT 3. $V_{L}(1)$, $V_{L}(2)$



No.8 $V_{L}(1)$, No.9 $V_{L}(2)$

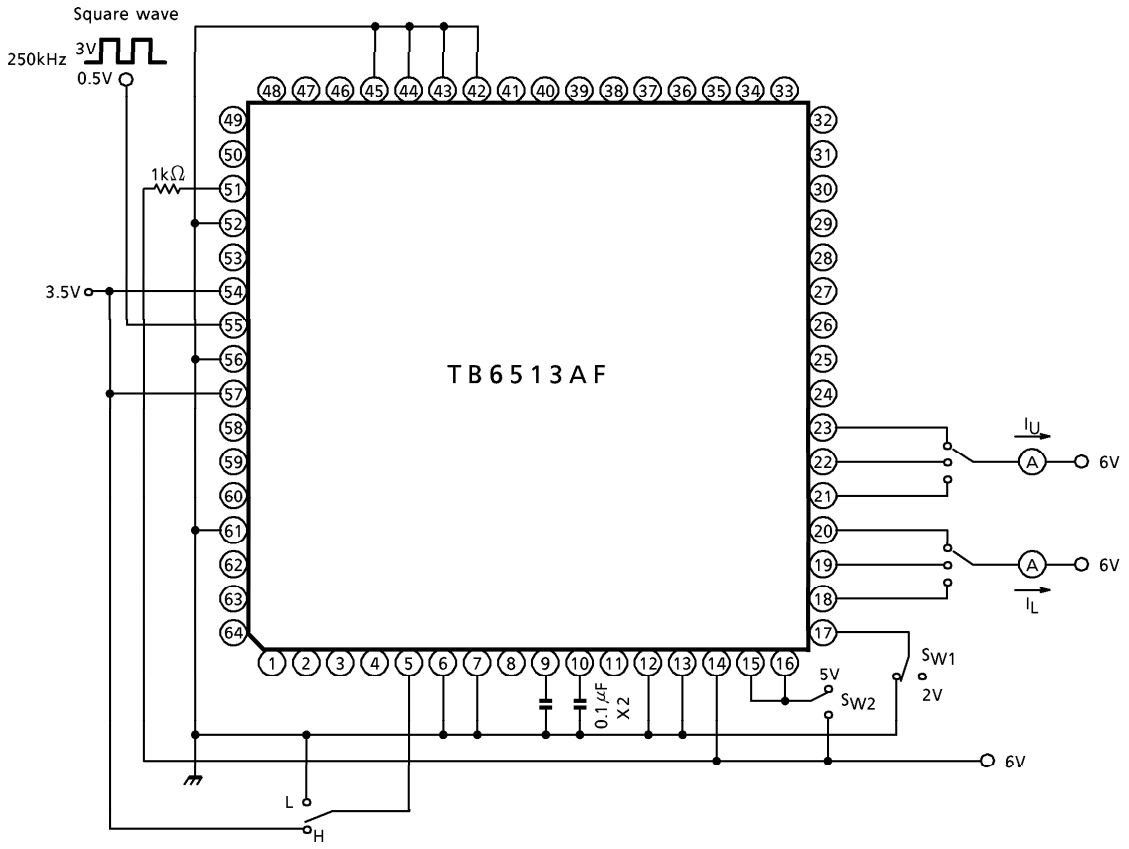
To set the drive angle, change the YSTB pin from high to low with YM1 = 0V, YM2 = 6V, and YM3 = 6V. Then input the number of clocks indicated below to the YCLK terminal.

After setting the drive angle, connect the YM1, YM2, and YM3 pins to PWTR and measure voltages at these terminals.



CLOCK	80	150	270
Terminal	YM3	YM1	YM2

TEST CIRCUIT 4. I_U, I_L

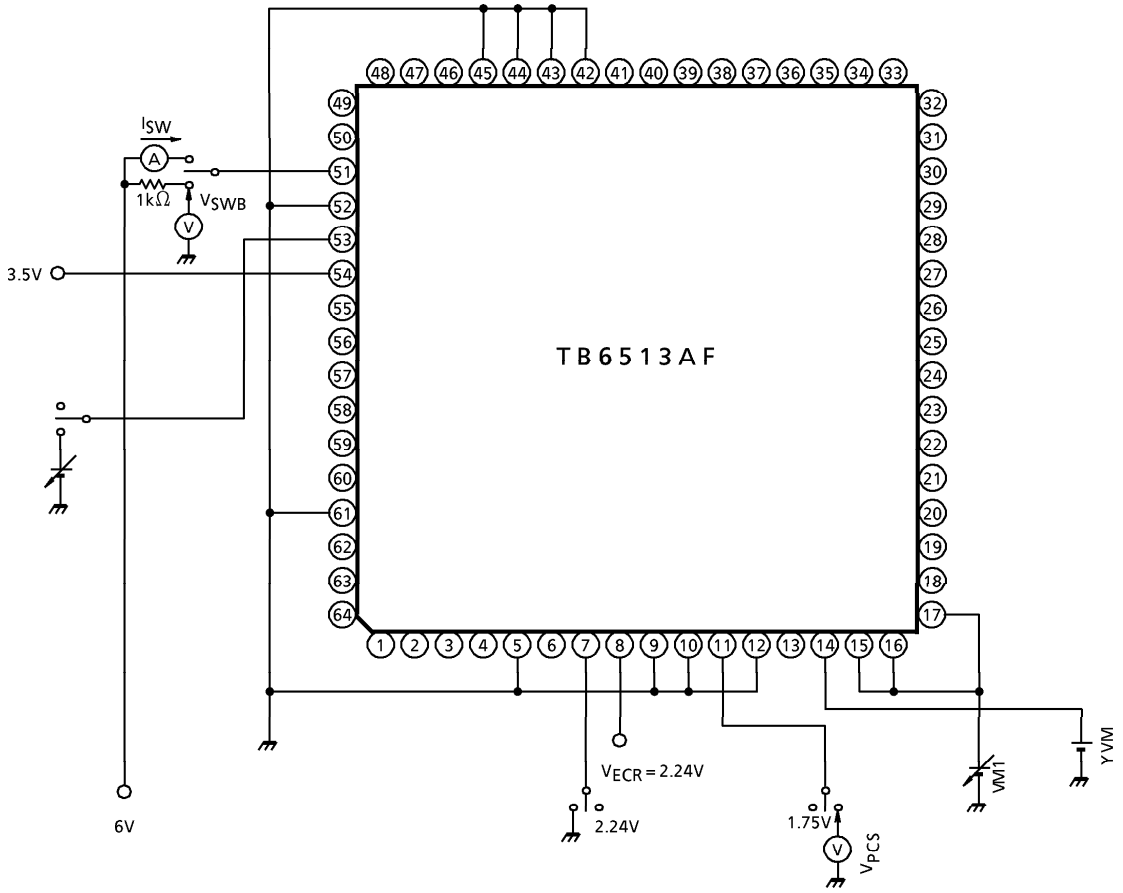


No.10 I_U, No.11 I_L

To set the drive angle, first change the YSTB terminal from high to low, then input the number of clocks indicated below to the YCLK terminal.

CLOCK	50		150		280	
Terminal	YU1	YL3	YU2	YL1	YU3	YL2
S_{W1}	0V	2V	0V	2V	0V	2V
S_{W2}	5V	6V	5V	6V	5V	6V

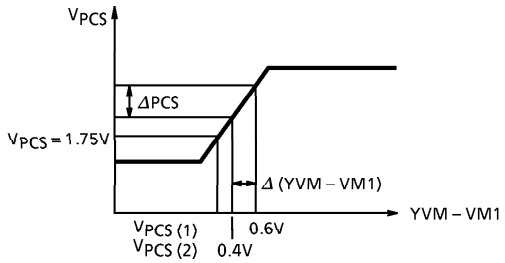
TEST CIRCUIT 5. $V_{PCS\,(1)}$, $V_{PCS\,(2)}$, YG_{PCS}, $I_{SW\,(1)}$, $I_{SW\,(2)}$, ΔV_{FC}, YVML, YVMS



No.12 $V_{PCS\,(1)}$
Set YVM = 6V and YEC = 2.24V, then measure VM1 when V_{PCS} = 1.75V.

No.13 $V_{PCS\,(2)}$
Set YVM = 6V and YEC = 0V, then measure VM1 when V_{PCS} = 1.75V.

No.14 YG_{PCS}
Set YVM = 6V and YEC = 2.24V, then determine YG_{PCS} from the amount that V_{PCS} voltage varies when (YVM – VM1) changes from 0.4V to 0.6V.



$$YG_{PCS} = \frac{\Delta PCS}{\Delta\,(YVM - VM1)}$$

No.15 I_{SW} (1)

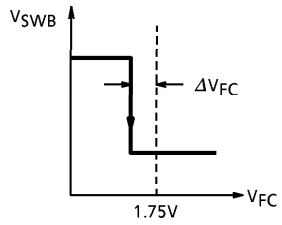
Set FC = 3V and YEC = 2.24V, then measure the current to the YSW terminal. (YVM = VM1 = 6V)

No.16 I_{SW} (2)

Set FC = 3V and YEC = 0V, then measure the current to the YSW terminal. (YVM = VM1 = 6V)

No.17 ΔV_{FC}

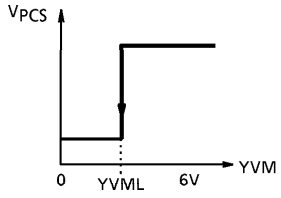
Set YPCS = 1.75V, then change FC from 0V and measure the difference between V_{FC} and V_{PCS} when V_{SWB} changes from high to low. (YVM = VM1 = 6V)



$$\Delta V_{FC} = V_{PCS} - V_{FC}$$

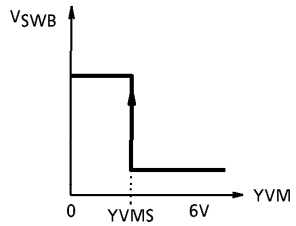
No.30 YVML

When FC = 3V, YEC = 2.24V, and VM1 = YVM − 1V, change YVM from 6V and measure YVML when V_{PCS} changes from high to low.

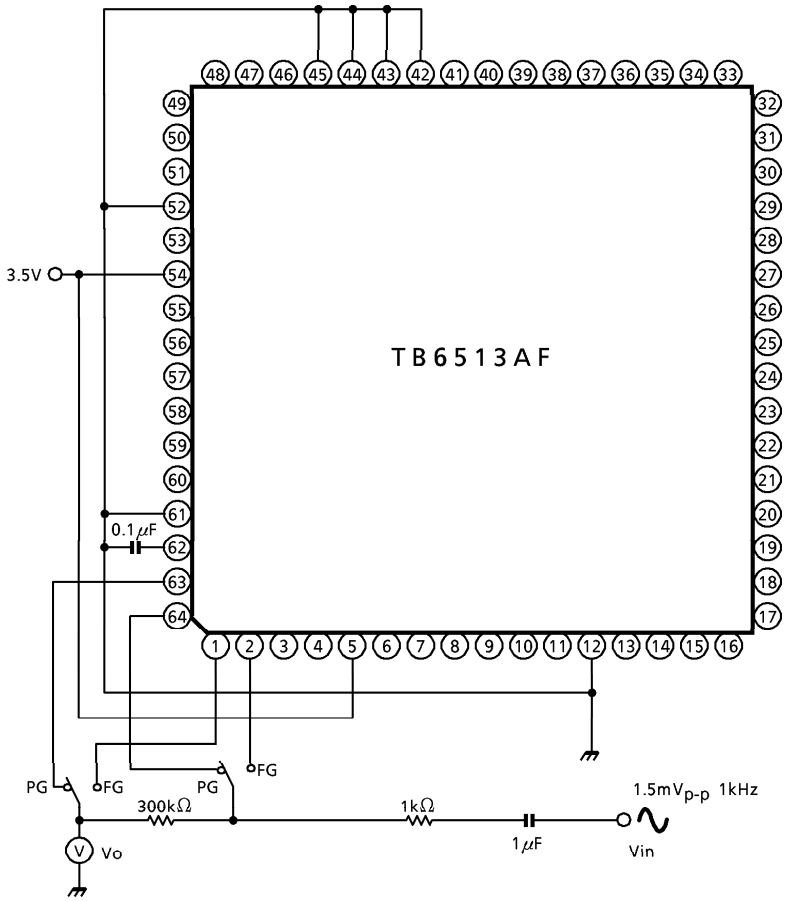


No.31 YVMS

Set FC = 3V, YEC = 0V, and VM1 = 6V, then change YVM from 6V and set YVMS when V_{SWB} changes from low to high.



TEST CIRCUIT 6. G_{FG}, G_{PG}



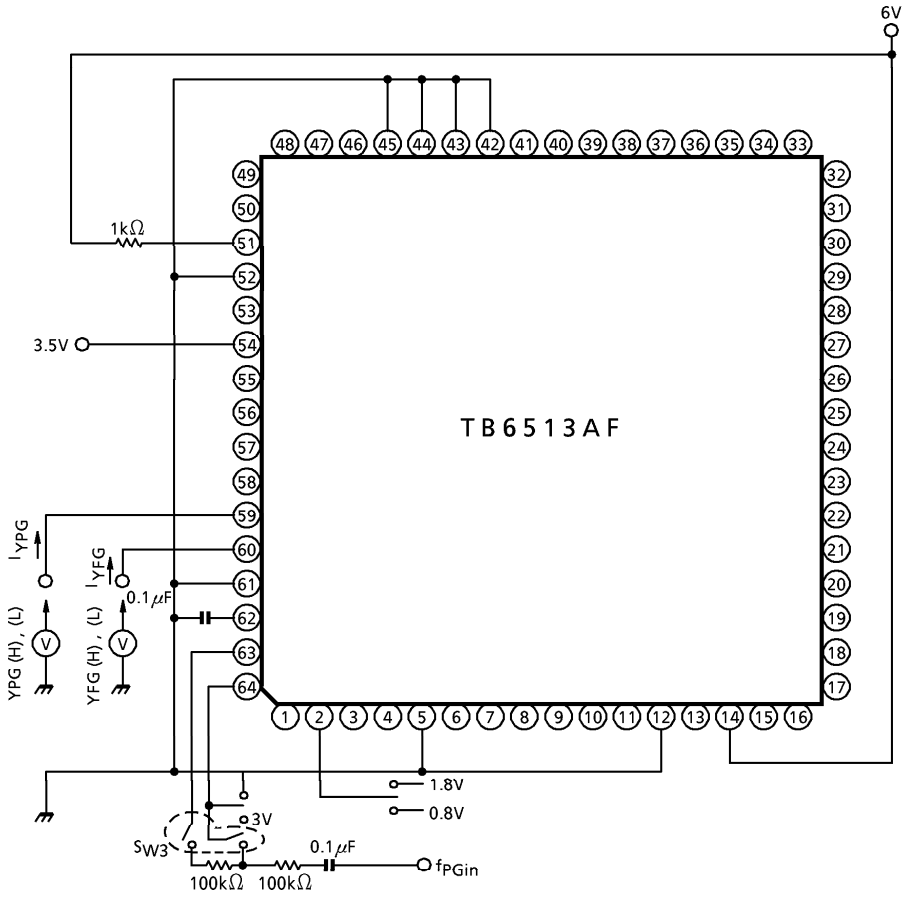
No.18 G_{FG}

Set SW to FG, then determine $G_{FG} = 20\ell og\ (Vo / Vin)$ by measuring Vo when $Vin = 1.5mV_{p\text{-}p}$, 1kHz.

No.21 G_{PG}

Set SW to PG, then determine $G_{PG} = 20\ell og\ (Vo / Vin)$ by measuring Vo when $Vin = 1.5mV_{p\text{-}p}$, 1kHz.

TEST CIRCUIT 7. YFG (H), YFG (L), ΔPGin, YPG (H), YPG (L)



No.19 YFG (H)

Apply 1.8V to YFGin and set YFG to high. Then measure the YFG potential when −100μA is input to I_{YFG}.

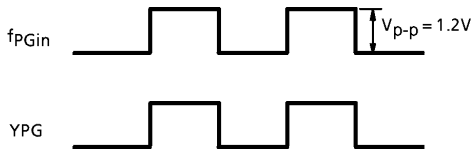
No.20 YFG (L)

Apply 0.8V to YFGin and set YFG to low. Then measure the YFG potential when 100μA is input to I_{YFG}.

No.22 ΔPGin

Turn SW3 on and input a 10kHz square wave from f_{PGin}. Set f_{PGin} to $1.2V_{p-p}$ (ΔPGin = 0.6V) and check that pin 59 is active.

Also, set V_{p-p} to 0.9V (ΔPGin = 0.45V) and check that terminal YPG is not active.



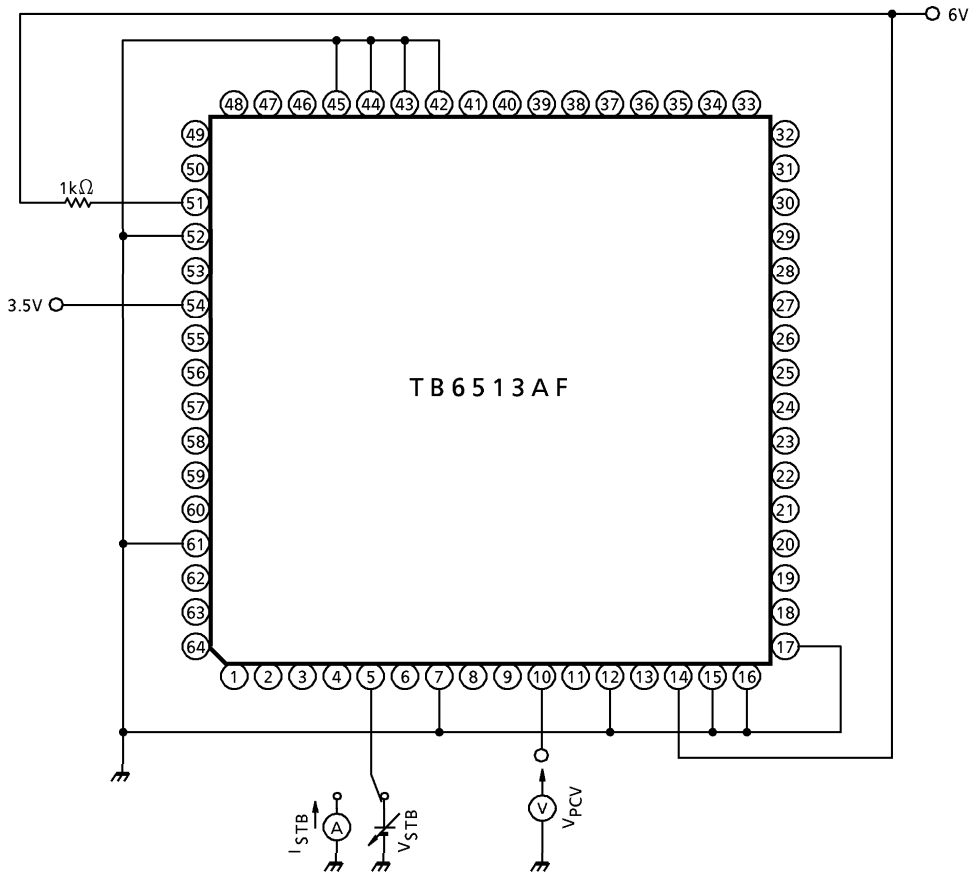
No.23 YPG (H)

Apply 3V to YPGin and set YPG to high. Then measure the YPG potential when a current of $I_{YPG} = -10\mu A$ is obtained.

No.24 YPG (L)

Apply 0V to YPGin and set YPG to low. Then measure the YPG potential when a current of $I_{YPG} = 100\mu A$ is obtained.

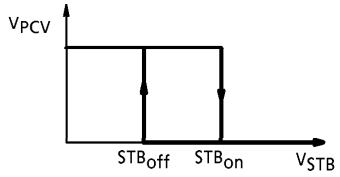
TEST CIRCUIT 8. STB_{on}, STB_{off}, I_{STB}



No.25 STB_{on}, No.26 STB_{off}

Change V_{STB} from 0V to 3.5V, and from 3.5V to 0V, and measure V_{PCV}.

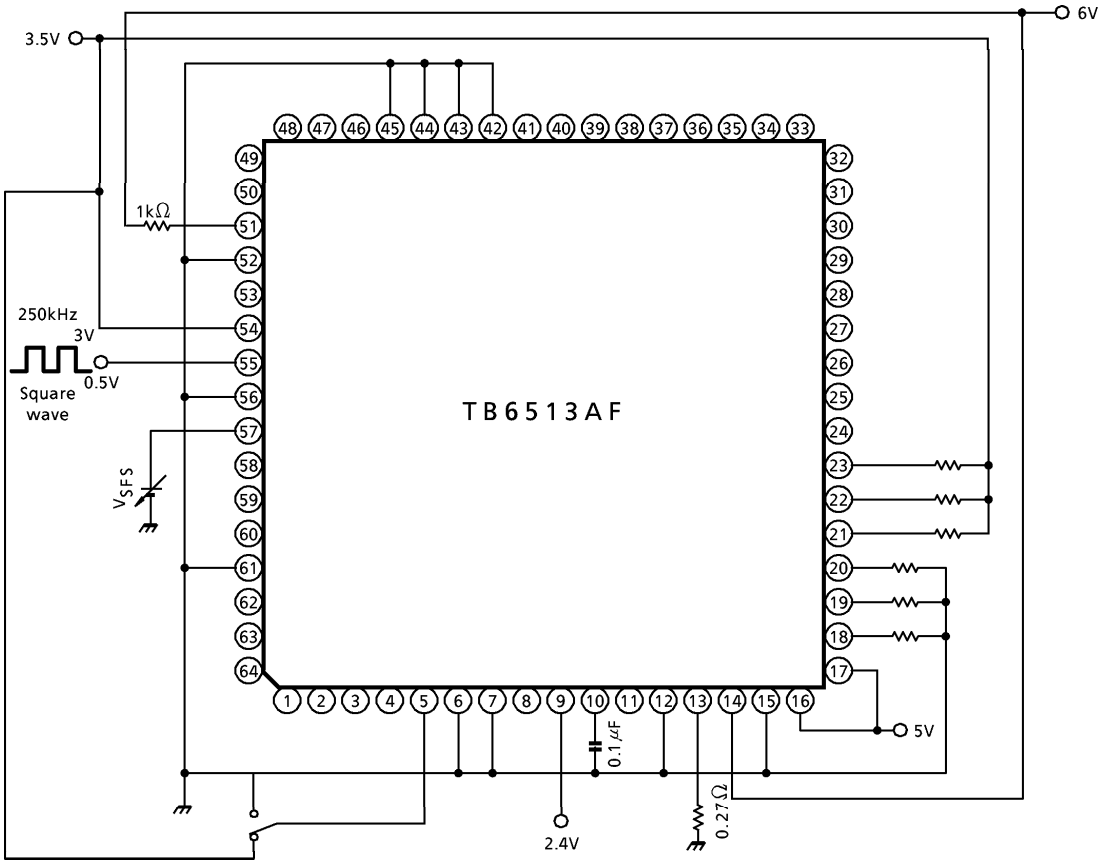
V_{STB} is STB_{on} when V_{PCV} changes from high to low. V_{STB} is STB_{off} when V_{PCV} changes from low to high.



No.27 I_{STB}

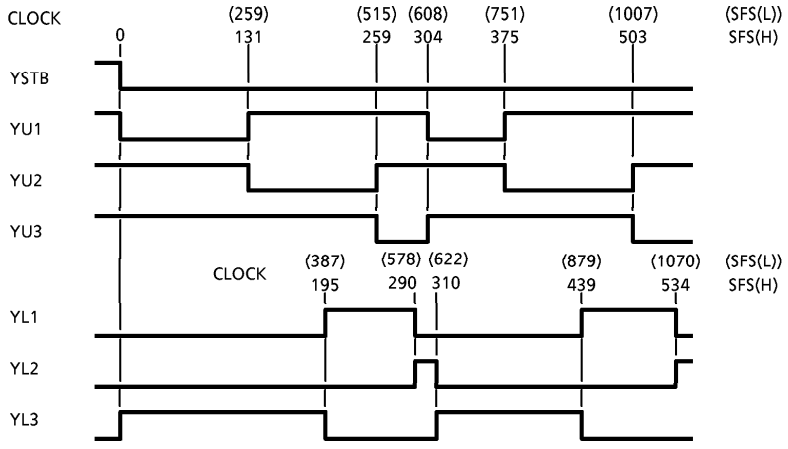
Measure I_{STB} when $V_{STB} = 0V$.

TEST CIRCUIT 9. SFS (L), SFS (H)

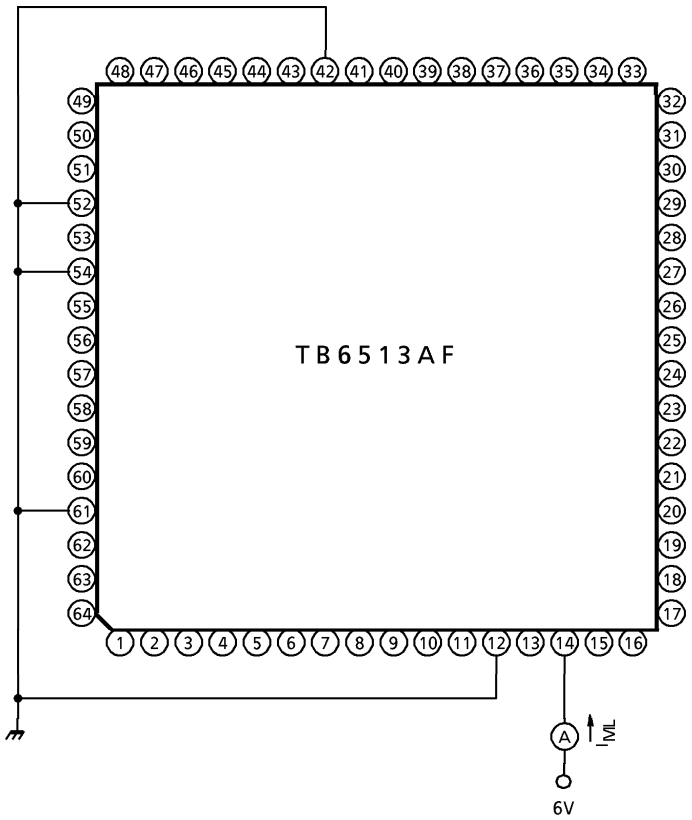


No.28 SFS (L), No.29 SFS (H)

Change V_{SFS} to 0V and to 3.5V, then measure the potential of YU1~3 and YL1~3.



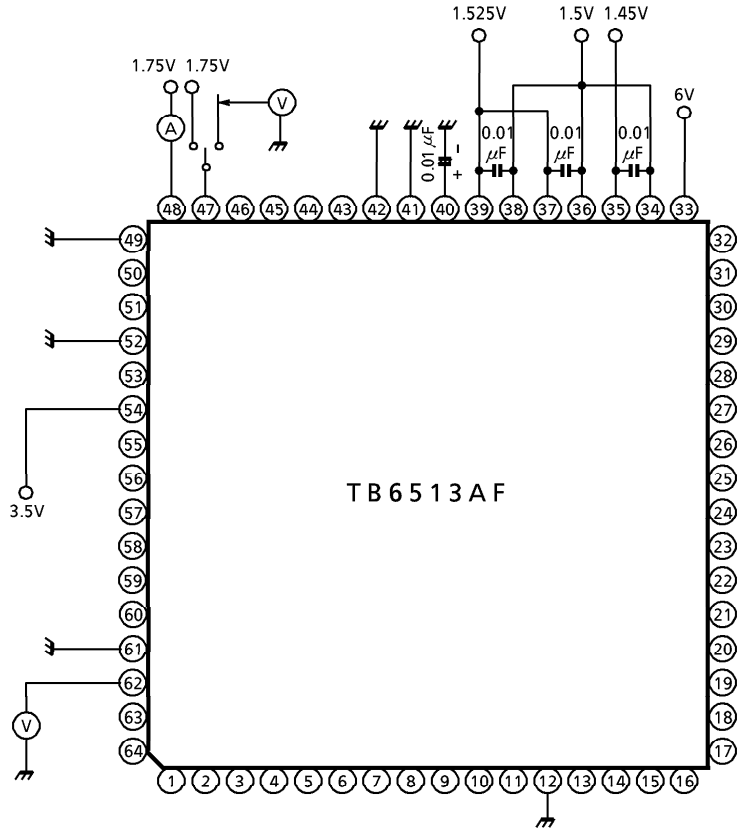
TEST CIRCUIT 10. I_{ML}



No.32 I_{ML}

Set YVM = 6V, then measure the current to pin⑭.

TEST CIRCUIT 11. CI_{EC}, CE_{CR}, CFG_{ref}



No.34 CI_{EC}

Set CEC = 1.75 and CECR = 1.75V, then measure the current to the CEC terminal.

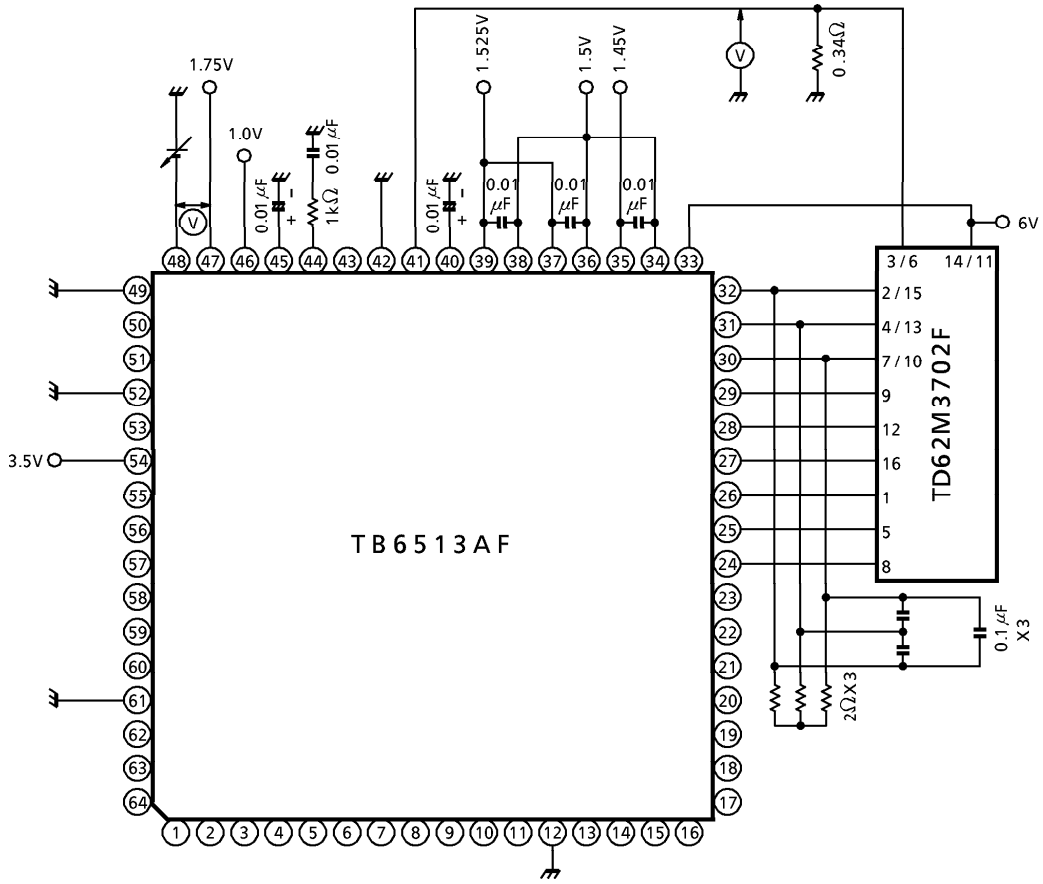
No.35 CE_{CR}

Measure the voltage of the CECR terminal.

No.58 CFG_{ref}

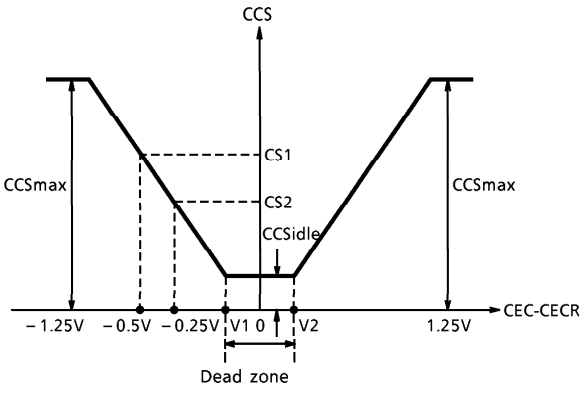
Measure the voltage of the REF terminal.

TEST CIRCUIT 12. CEC, CCSmax, CGio, CCSidle, CECofs, CECdz



No.36 No.37 No.38 No.39 No.40 No.41

Set CTL = 1.0V and CECR = 1.75V, change CEC from 0V to 3.5V, measure the potential of the CCS terminal, and check the voltage characteristics.



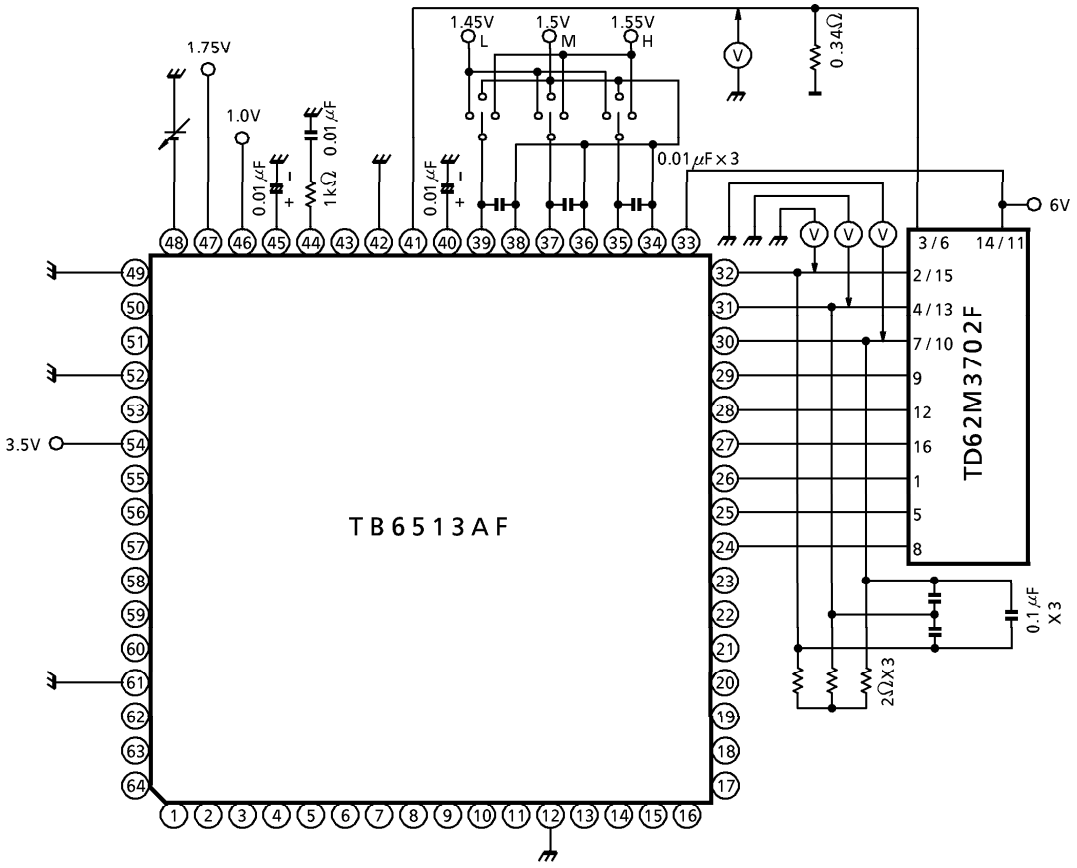
$$CGio = \frac{CS1 - CS2}{0.25V}$$

CCSidle : CS potential inside the dead zone

$$CECofs = \frac{V1 + V2}{2}$$

$$CECdz = V2 - V1$$

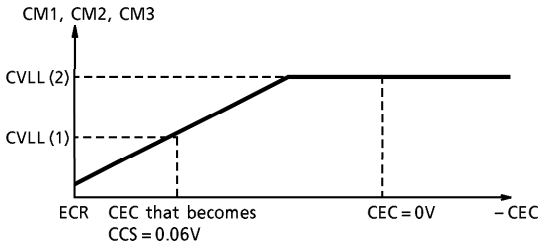
TEST CIRCUIT 13. CVLL (1), CVLL (2)



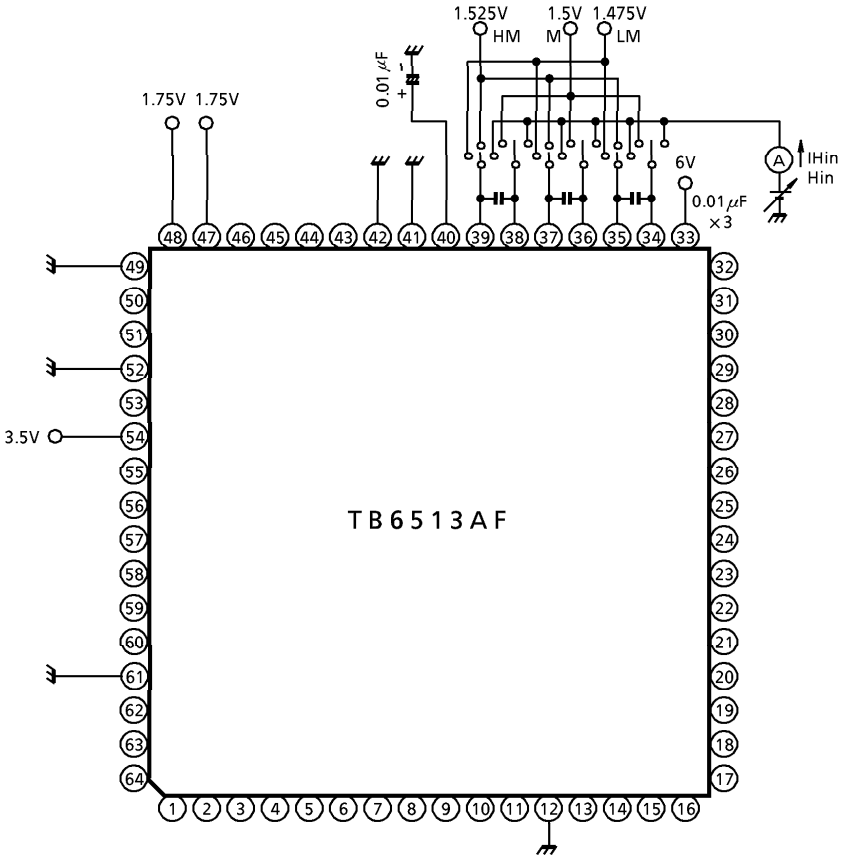
No.42 CVLL (1), No.43 CVLL (2)

Make the settings listed in the following table. Measure the potential at the CM1, CM2, and CM3 terminals when the CEC voltage is adjusted to 0V so that CCS = 0.06V, and when CEC = 0V.

	H1 +	H2 +	H3 +	PIN
1	H	L	M	CM1
2	M	H	L	CM2
3	L	M	H	CM3



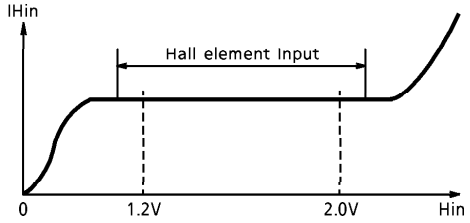
TEST CIRCUIT 14. Hin



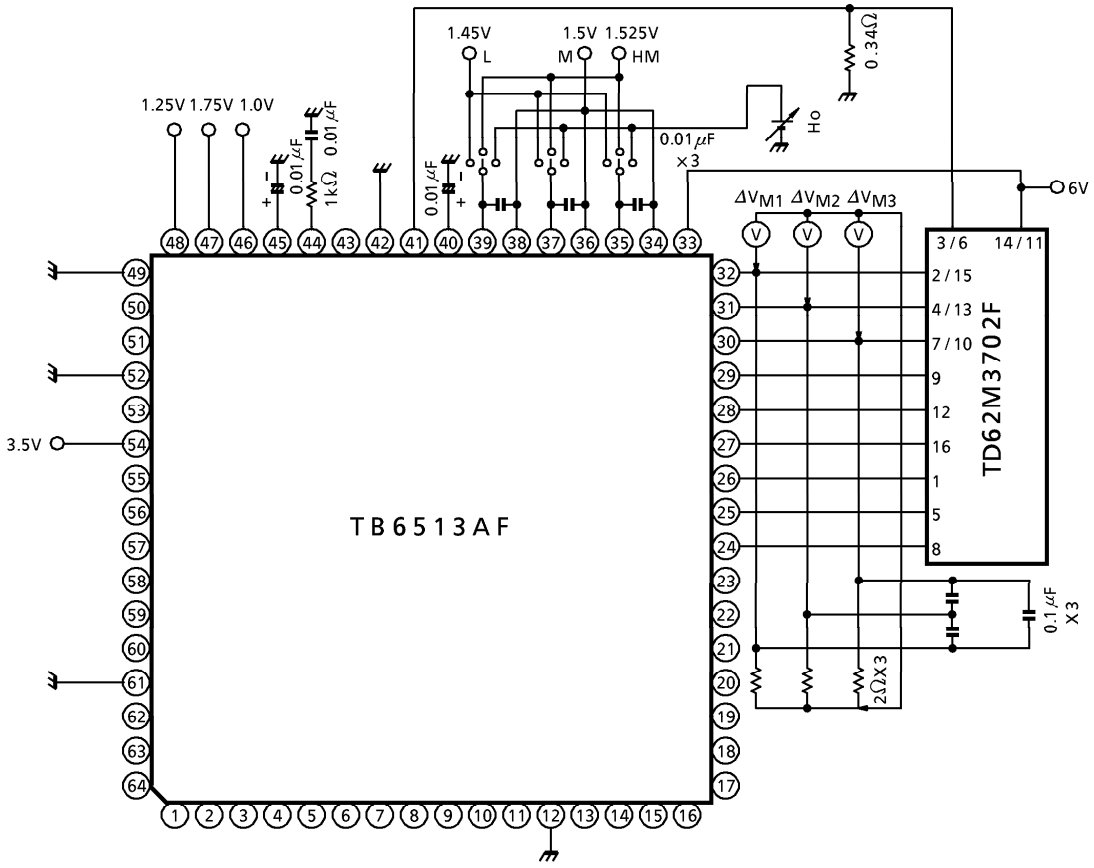
No.44 Hin

Make the settings listed in the following table. Measure the Hin voltage range in which IHin does not change rapidly versus the change in Hin.

	H1 +	H1 −	H2 +	H2 −	H3 +	H3 −
1	Hin	Hin	HM	M	LM	M
2	LM	M	Hin	Hin	HM	M
3	HM	M	LM	M	Hin	Hin



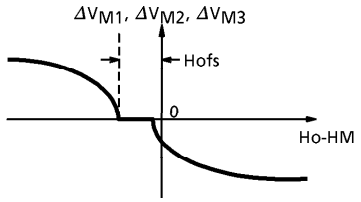
TEST CIRCUIT 15. Hofs



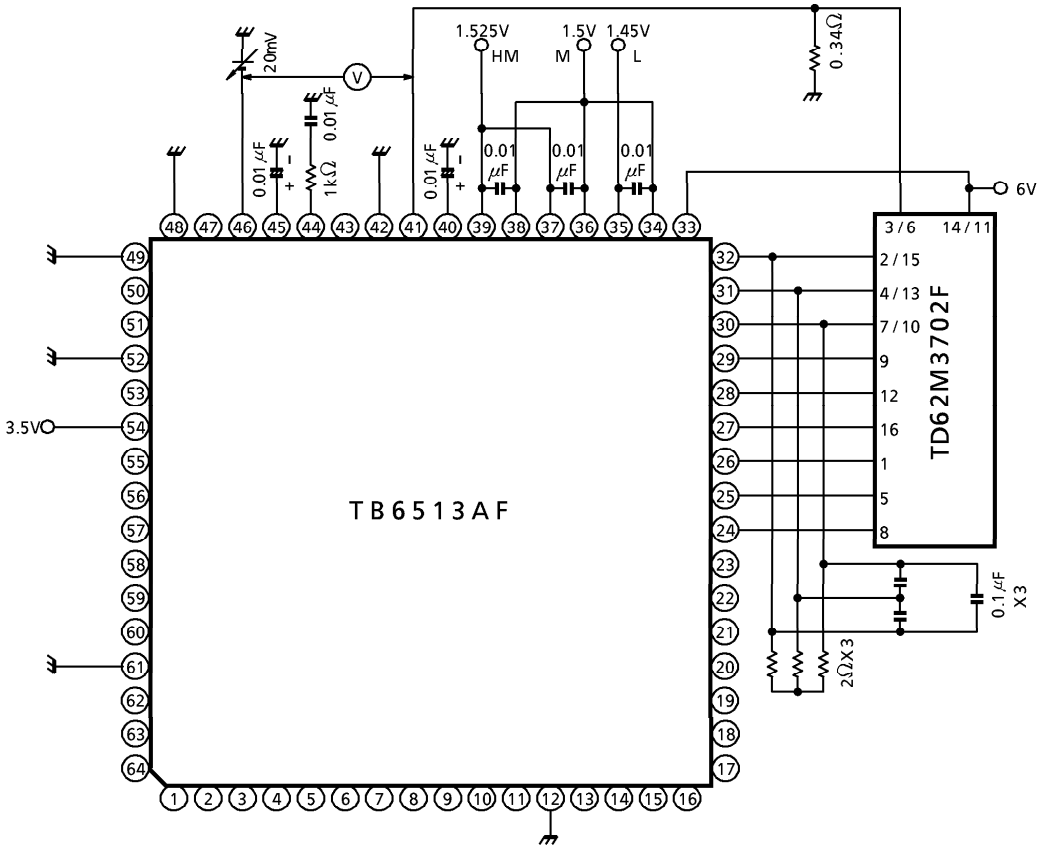
No.45 Hofs

Make the settings listed in the following table, and measure the Hall element input conversion offset.

	H1+	H2+	H3+	OFFSET
1	Ho	HM	L	$\Delta V_{M1}=0$ distance between H1+ and H2+
2	L	Ho	HM	$\Delta V_{M2}=0$ distance between H2+ and H3+
3	HM	L	Ho	$\Delta V_{M3}=0$ distance between H3+ and H1+

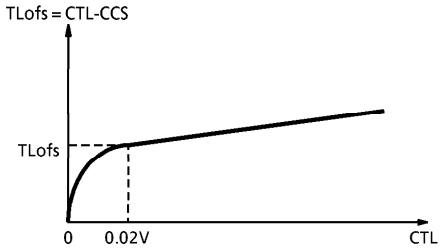


TEST CIRCUIT 16. TLofs

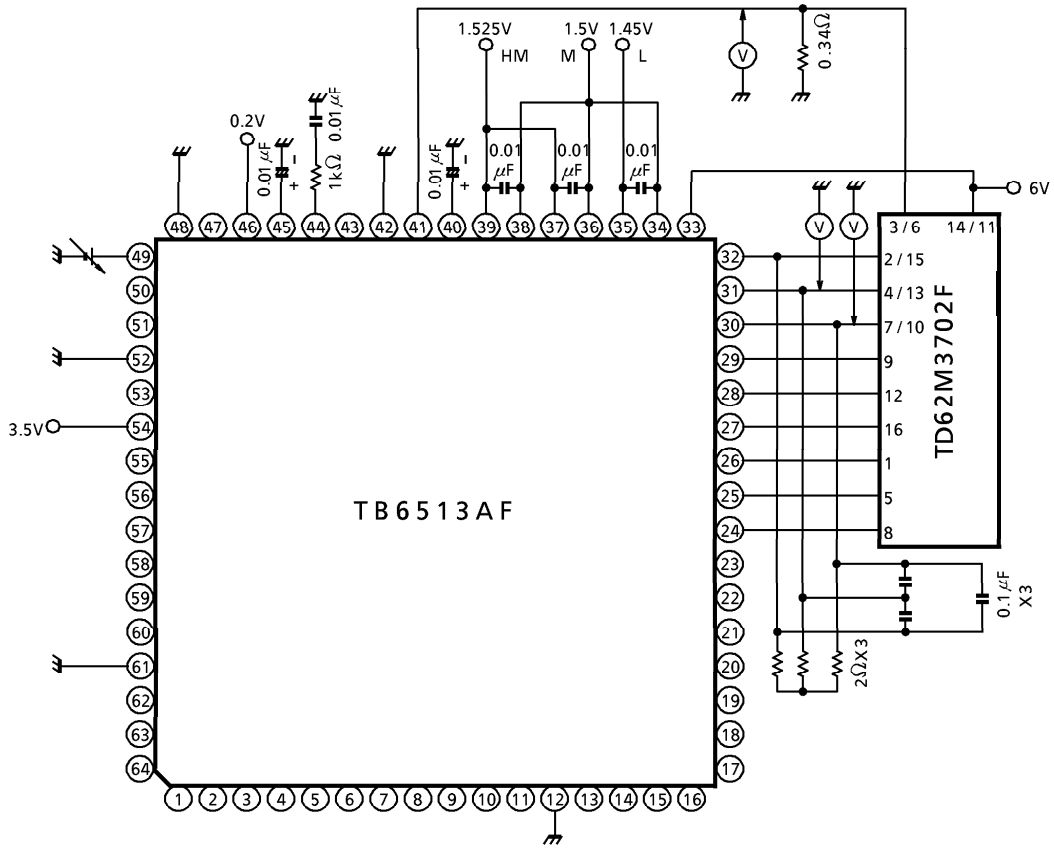


No.46 TLofs

Measure the potential differential (CTL-CCS) of the CTL and the CCS terminals when CTL = 0.02V.

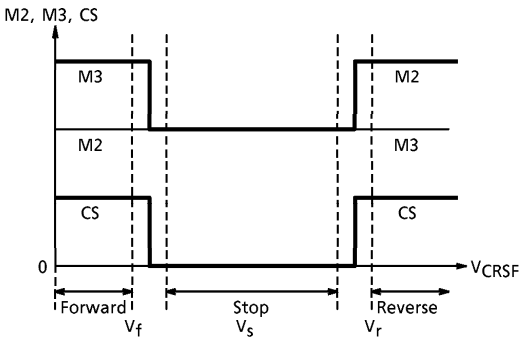


TEST CIRCUIT 17. Vf, Vs, Vr

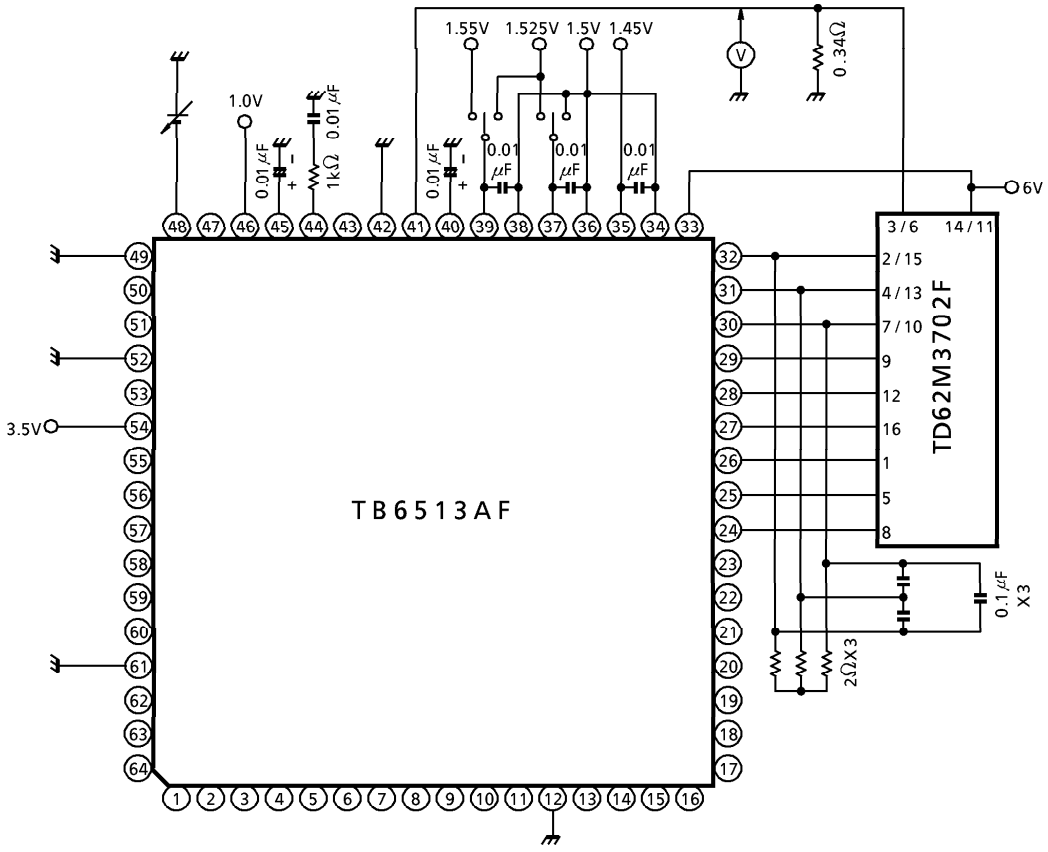


No.47 Vf, No.48 Vs, No.49 Vr

Change CRSF from 0V to 3.5V, obtain the characteristics in the following diagram, and measure the threshold voltage.



TEST CIRCUIT 18. R



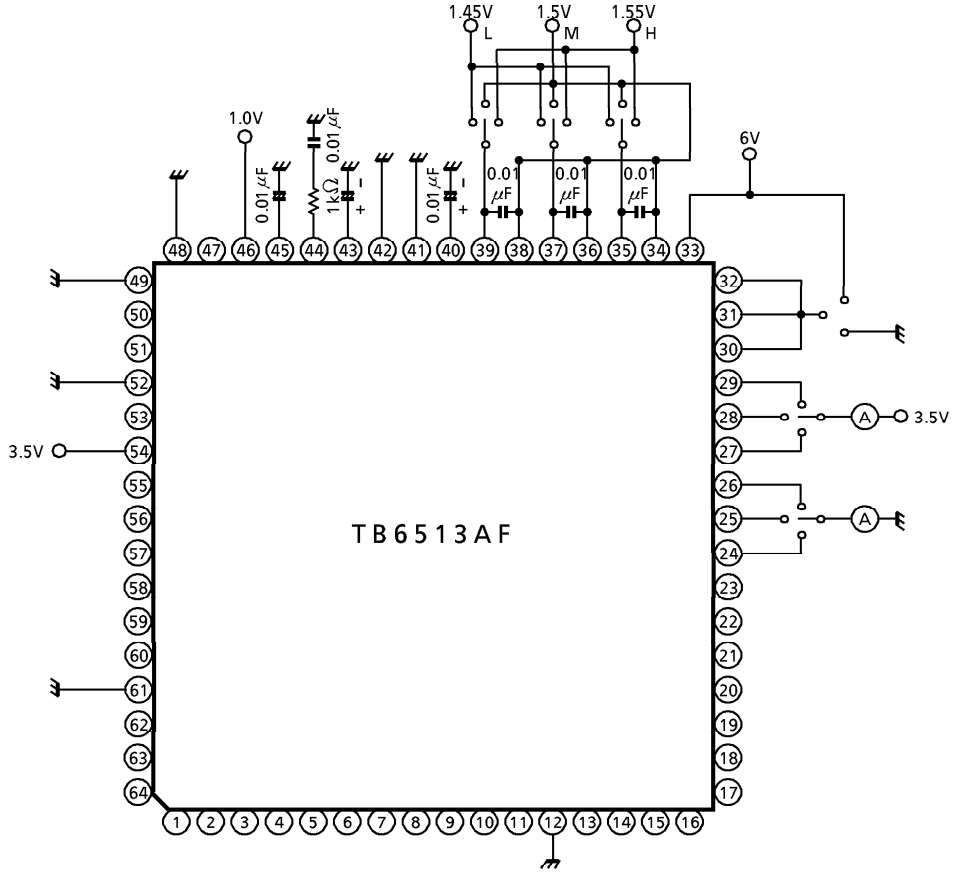
No.50 R

Adjust the CEC voltage so that CCS becomes 0.06V with H1+ = 1.525V and H2+ = 1.525V. Measure the CCS (CS_L) when H1+ = 1.525V and H2+ = 1.525V and measure the CCS (CS_H) when H1+ = 1.55V and H2+ = 1.5V.

Then determine

$$R = \frac{CS_H - CS_L}{CS_L}$$

TEST CIRCUIT 19. CI_U, CI_L

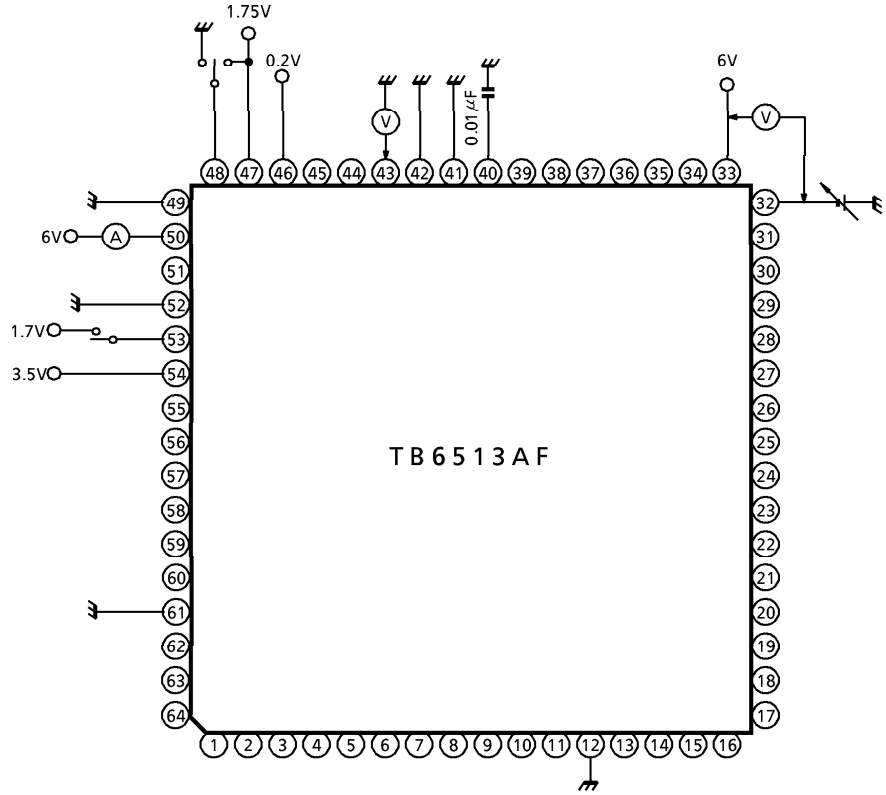


No.51 CI_U, No.52 CI_L

Make the settings in the following table, and measure the current to the CU1, CU2, and CU3 terminals, and to the CL1, CL2, and CL3 terminals.

	H1 +	H2 +	H3 +	M1, M2, M3	PIN
1	L	H	M	GND	CU1
2	M	L	H	GND	CU2
3	H	M	L	GND	CU3
4	H	L	M	V_M	CL1
5	M	H	L	V_M	CL2
6	L	M	H	V_M	CL3

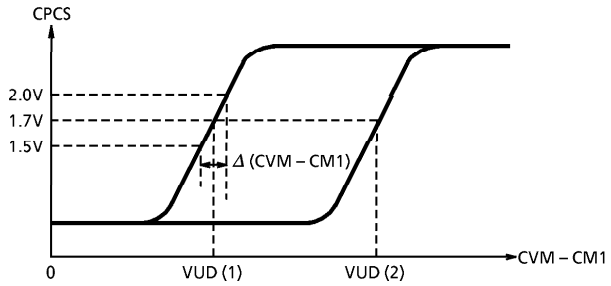
TEST CIRCUIT 20. CG_{PCS}, VUD (1), VUD (2), CI_{SWB}



No.54 CG_{PCS}, No.55 VUD (1), No.56 VUD (2)

Set CEC = 0V and change CM1 from 6V to 5V. Measure the potential differential (CVM – CM1) between the CVM terminal and the CM1 terminal when the potential of the CPCS terminal becomes 1.7V.

Set CEC = CECR = 1.75V, make the same measurements as above, and obtain the characteristics in the following diagram.

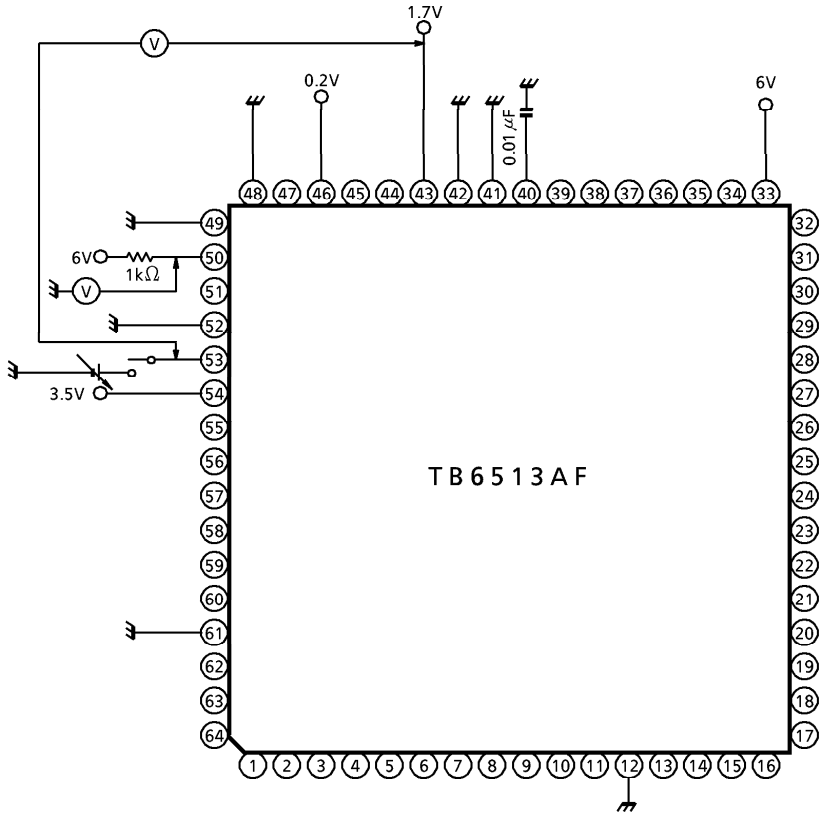


$$CG_{PCS} = \frac{2.0V - 1.5V}{\Delta (CVM - CM1)}$$

No.57 CI_{SWB}

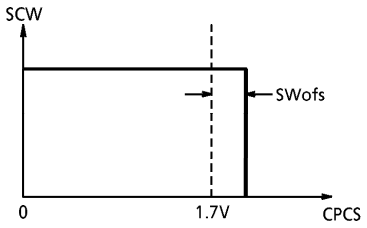
Set FC = 1.7V, CEC = 0V, and CM1 = 6V, measure the current to the SCW terminal.

TEST CIRCUIT 21. CSWofs

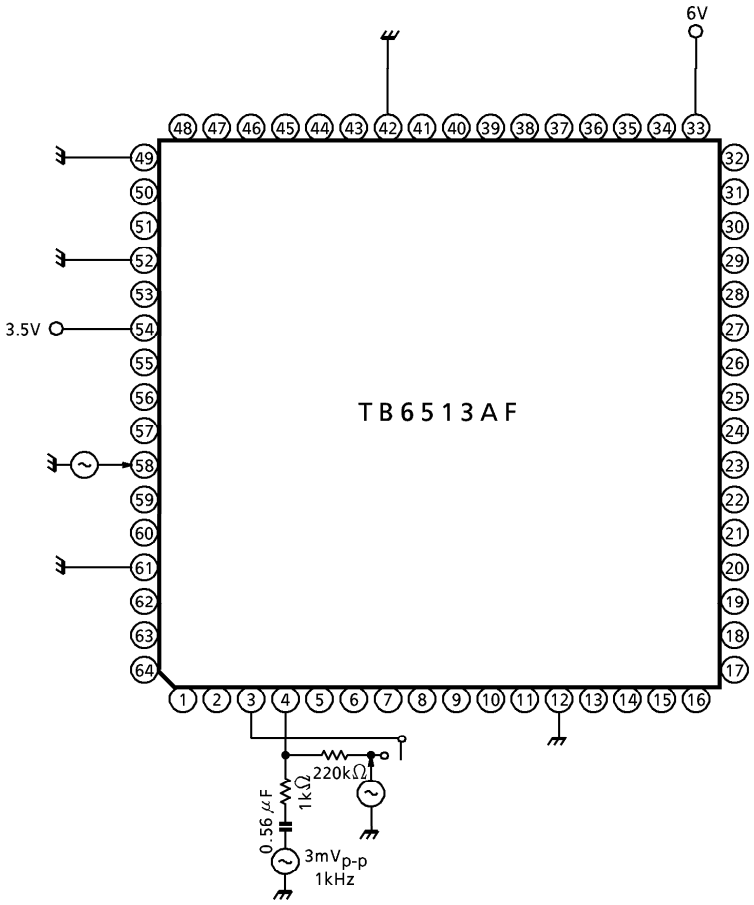


No.53 CSWofs

Set CPCS = 1.7V and change FC from 0V to 3.5V. Measure the potential differential (FC – CPCS) between the FC terminal and the CPCS terminal when SCW changes from high to low.



TEST CIRCUIT 22. CG_{FG}, CFG_H, CFG_L

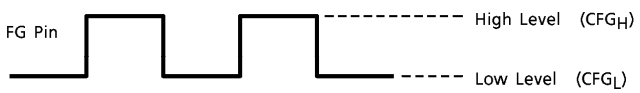


No.59 CG_{FG} No.60 CFG_H No.61 CFG_L

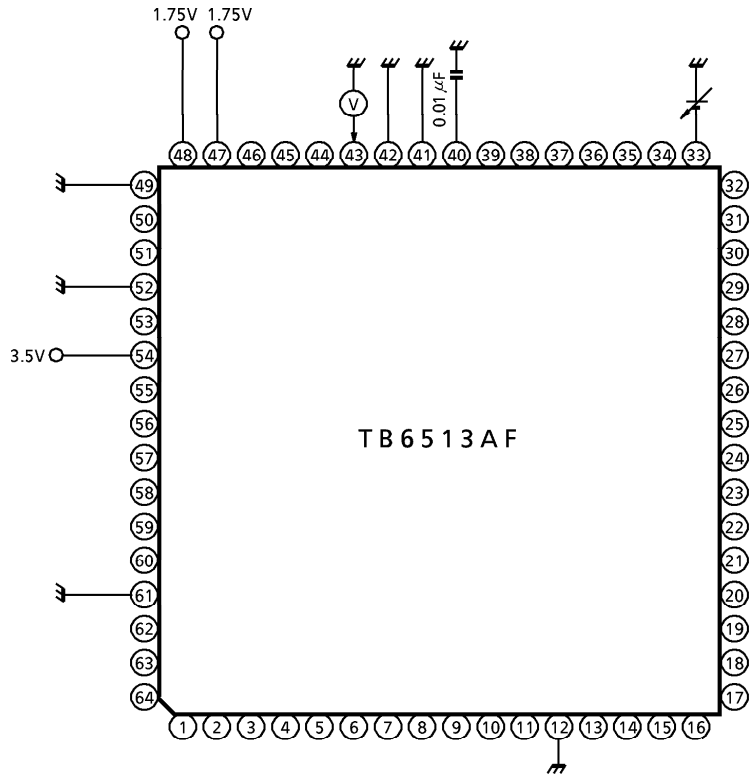
Set CFGout = Vo. When Vin = $3mV_{p-p}$ at 1kHz, measure Vo and determine the following :

$$CG_{FG} = 20\ell og\frac{Vo}{Vin}$$

Obtain the characteristics in the following diagram and measure the high-level and low-level potential of the CFG terminal output waveform.

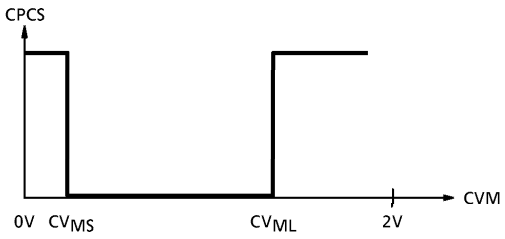


TEST CIRCUIT 23. CV_{ML}, CV_{MS}



No.62 CV_{ML} No.63 CV_{MS}

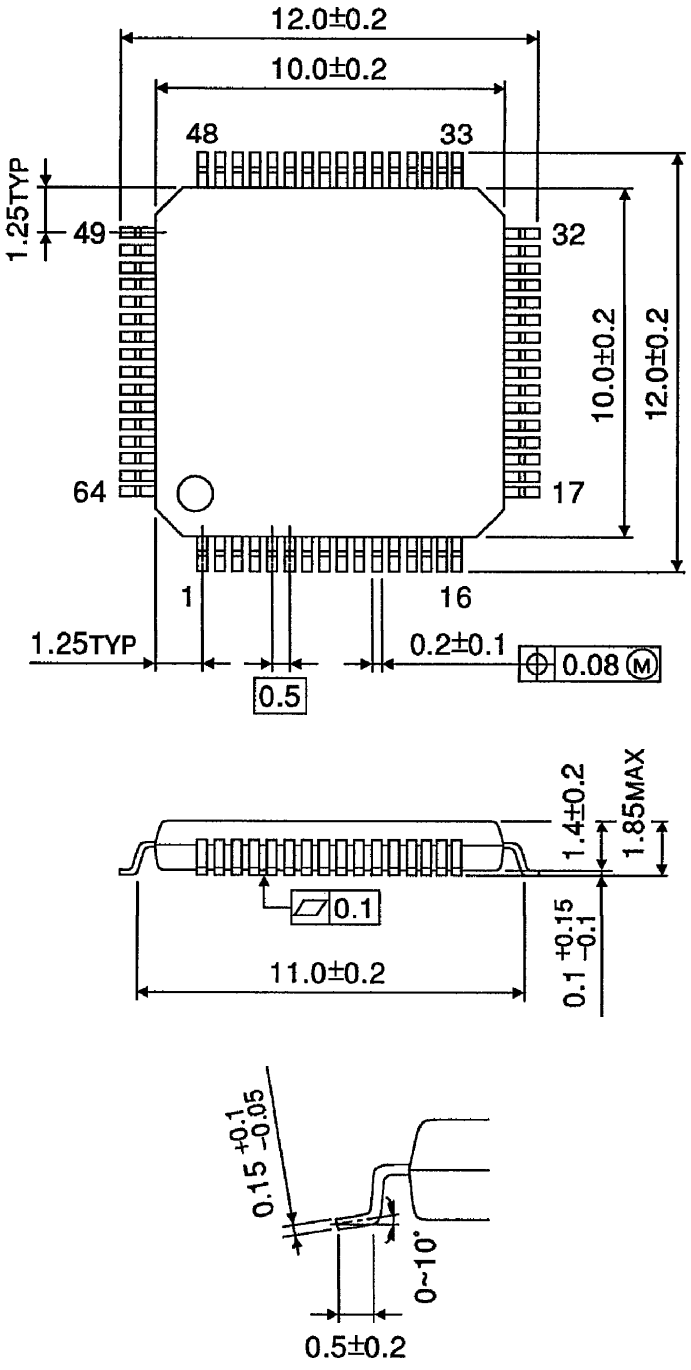
Change the CVM from 2V to 0V, obtain the characteristics in the diagram below, and measure the threshold voltage.



OUTLINE DRAWING

LQFP64-P-1010-0.50A

Unit : mm



Weight : 0.34g (Typ.)