

2,097,152 WORDS×40 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM402020SG is a 2,097,152 words by 40 bits dynamic RAM module which assembled 20 pcs of TC514400J on the printed circuit board.

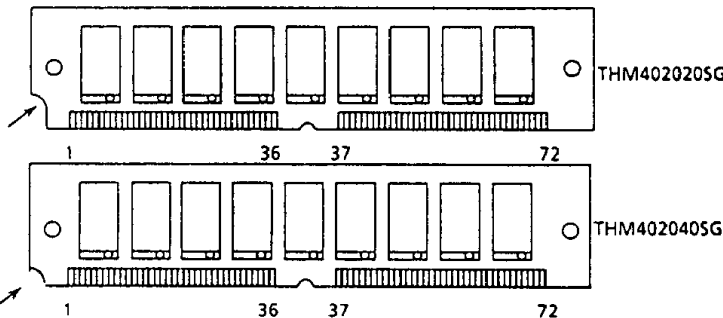
The THM402020SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

FEATURES

- 2,097,152 words by 40 bits organization
- Fast access time and cycle time
- Single power supply of 5V±10%
- Low power
5,885mW MAX. Operating (THMxxxxxx-80)
5,060mW MAX. Operating (THMxxxxxx-10)
110mW MAX. Standby
- Read-Modify-write, CAS before RAS refresh, RAS only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1024 Refresh cycles/16ms
- Gold Contact
- JEDEC OUTLINE : THM402020SG - 80, 10
- NON JEDEC OUTLINE : THM402040SG - 80, 10

	THM402020 SG-80	THM402020 SG-10
t _{RAC} RAS Access Time	80ns	100ns
t _{AA} Column Address Access Time	40ns	50ns
t _{CAC} CAS Access Time	20ns	25ns
t _{RC} Cycle Time	150ns	180ns
t _{PC} Fast Page Mode Cycle Time	50ns	60ns

PIN CONNECTION (TOP VIEW)



PIN NAMES

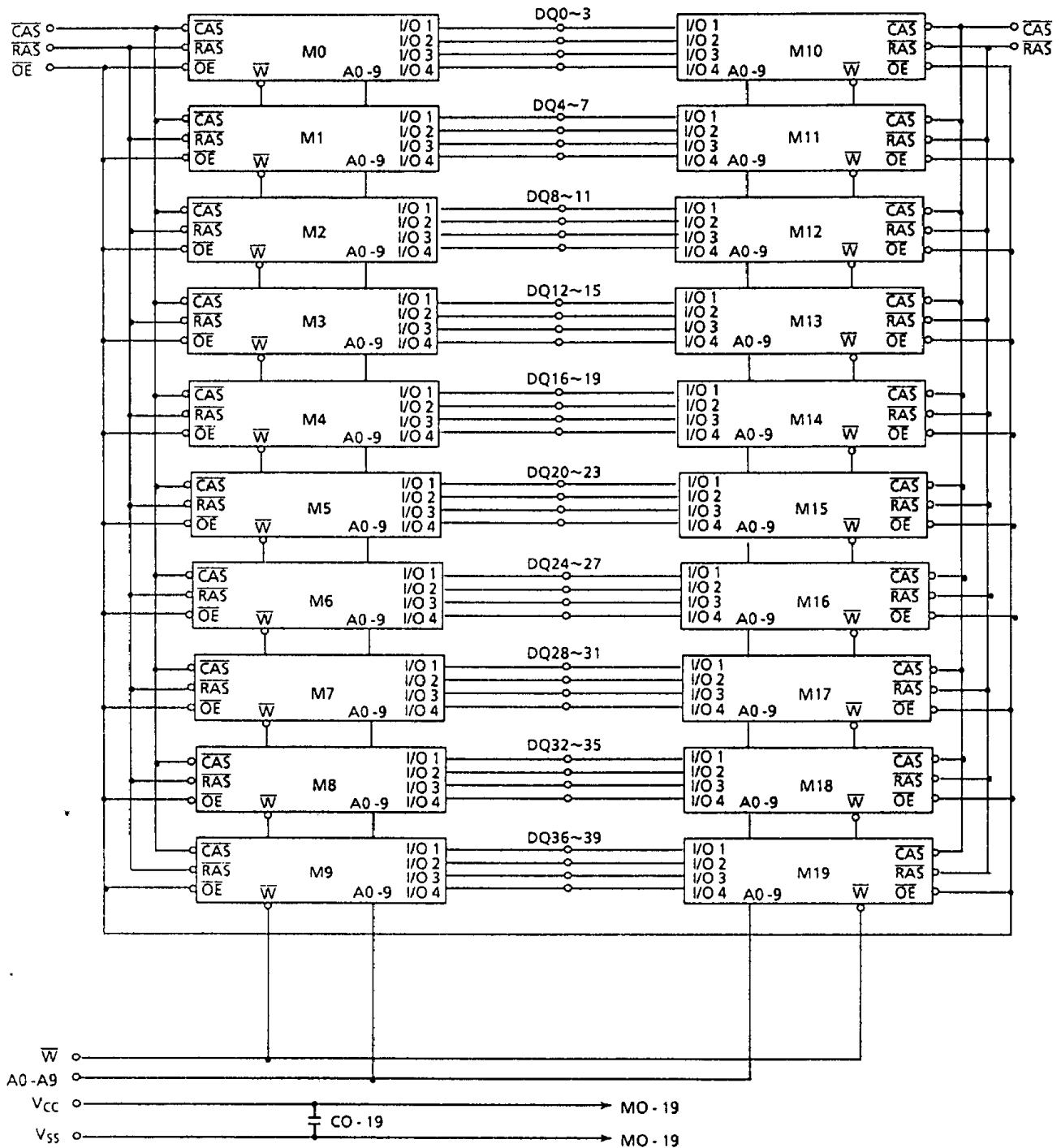
A0~A9	Address Inputs
DQ0~DQ39	Data Inputs/Outputs
CAS0, CAS1	Column Address Strobe
RAS0, RAS1	Row Address Strobe
W	Read/Write Input
OE	Output Enable
V _{CC}	Power (+ 5V)
V _{SS}	Ground
PD	Presence Detect Pin

	1	36	37	72		
1	V _{SS}	13 A1	25 DQ13	37 DQ19	49 DQ22	61 DQ33
2	DQ0	14 A2	26 DQ14	38 DQ20	50 DQ23	62 DQ34
3	DQ1	15 A3	27 DQ15	39 V _{SS}	51 DQ24	63 DQ35
4	DQ2	16 A4	28 A7	40 CAS0	52 DQ25	64 DQ36
5	DQ3	17 A5	29 DQ16	41 NC	53 DQ26	65 DQ37
6	DQ4	18 A6	30 V _{CC}	42 NC	54 DQ27	66 DQ38
7	DQ5	19 OE	31 A8	43 CAS1	55 DQ28	67 PD0
8	DQ6	20 DQ8	32 A9	44 RAS0	56 DQ29	68 PD1
9	DQ7	21 DQ9	33 NC	45 RAS1	57 DQ30	69 PD2
10	V _{CC}	22 DQ10	34 NC	46 DQ21	58 DQ31	70 PD3
11	NC	23 DQ11	35 DQ17	47 W	59 V _{CC}	71 DQ39
12	A0	24 DQ12	36 DQ18	48 V _{SS}	60 DQ32	72 V _{SS}

	- 80	- 10
PD0	NC	NC
PD1	NC	NC
PD2	NC	V _{SS}
PD3	V _{SS}	V _{SS}

THM402020SG-80, 10

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	- 1.0~7.0	V	1
Output Voltage	V_{OUT}	- 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	- 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	- 55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	6.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	- 1.0	-	0.8	V	2

THM402020SG-80, 10

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I_{CC1}	OPERATING CURRENT					
	Average Power Supply Operating Current (\overline{RAS} , \overline{CAS} , Address Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	THM402020SG-80	-	1070	mA	3,4,5
		THM402020SG-10	-	920		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	-	40	mA		
I_{CC3}	\overline{RAS} ONLY REFRESH CURRENT					
	Average Power Supply Current, \overline{RAS} Only Mode (\overline{RAS} Cycling, $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC} \text{ MIN.}$)	THM402020SG-80	-	1070	mA	3,5
		THM402020SG-10	-	920		
I_{CC4}	FAST PAGE MODE CURRENT					
	Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, \overline{CAS} Address Cycling: $t_{PC} = t_{PC} \text{ MIN.}$)	THM402020SG-80	-	720	mA	3,4,5
		THM402020SG-10	-	620		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	-	20	mA		
I_{CC6}	\overline{CAS} BEFORE \overline{RAS} REFRESH CURRENT					
	Average Power Supply Current, \overline{CAS} Before \overline{RAS} Mode (\overline{RAS} , \overline{CAS} Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	THM402020SG-80	-	1070	mA	3
		THM402020SG-10	-	920		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins not under Test = 0V)	-200	200	μA		
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)	-20	20	μA		
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	-	V		
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	-	0.4	V		

THM402020SG-80, 10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM402020 SG-80		THM402020 SG-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to \overline{RAS}	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to \overline{RAS}	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to \overline{RAS} Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to \overline{CAS} Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to \overline{RAS}	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	\overline{CAS} to \overline{WRITE} Delay Time	50	-	60	-	ns	13
t_{RWD}	\overline{RAS} to \overline{WRITE} Delay Time	110	-	135	-	ns	13
t_{AWD}	Column Address to \overline{WRITE} Delay Time	70	-	85	-	ns	13
t_{CPWD}	\overline{CAS} Precharge to \overline{WRITE} Delay Time	75	-	90	-	ns	13
t_{CSR}	\overline{CAS} Set-Up Time (\overline{CAS} before \overline{RAS} Cycle)	5	-	5	-	ns	
t_{CHR}	\overline{CAS} Hold Time (\overline{CAS} before \overline{RAS} Cycle)	15	-	20	-	ns	
t_{RPC}	\overline{RAS} to \overline{CAS} Precharge Time	0	-	0	-	ns	
t_{CPT}	\overline{CAS} Precharge Time (\overline{CAS} before \overline{RAS} Counter Test Cycle)	40	-	50	-	ns	
t_{ROH}	\overline{RAS} Hold Time referenced to \overline{OE}	10	-	20	-	ns	
t_{OEA}	\overline{OE} Access Time	-	20	-	25	ns	
t_{OED}	\overline{OE} to Data Delay	20	-	25	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from \overline{OE}	0	20	0	20	ns	10
t_{OEH}	\overline{OE} Command Hold Time	20	-	25	-	ns	
t_{WRP}	\overline{WRITE} to \overline{RAS} Precharge Time (\overline{CAS} before \overline{RAS} Cycle)	10	-	10	-	ns	
t_{WRH}	\overline{WRITE} to \overline{RAS} Hold Time (\overline{CAS} before \overline{RAS} Cycle)	10	-	10	-	ns	

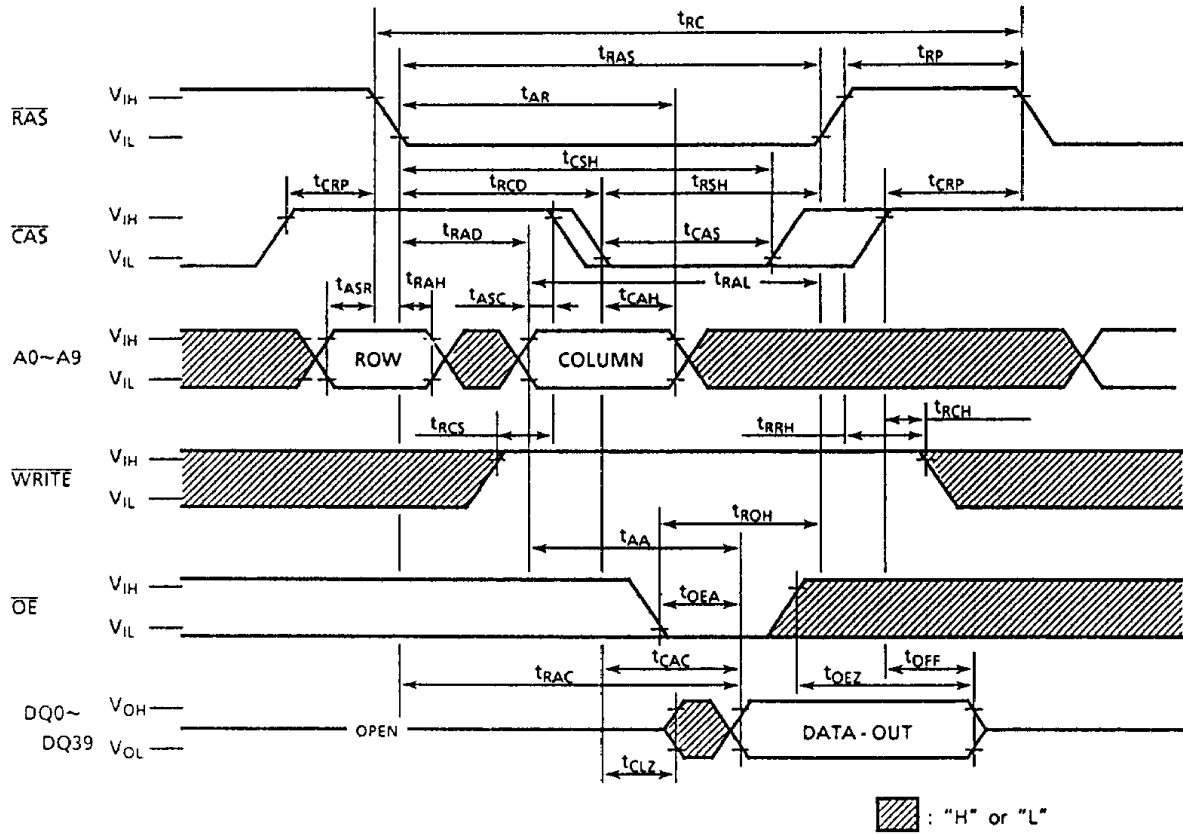
CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $f = 1\text{MHz}$, $T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C11	Input Capacitance (A0~A9)	-	130	pF
C12	Input Capacitance (\overline{W} , \overline{OE})	-	130	pF
C13	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	-	70	pF
C14	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	-	70	pF
CDQ	I/O Capacitance (DQ0~DQ39)	-	35	pF

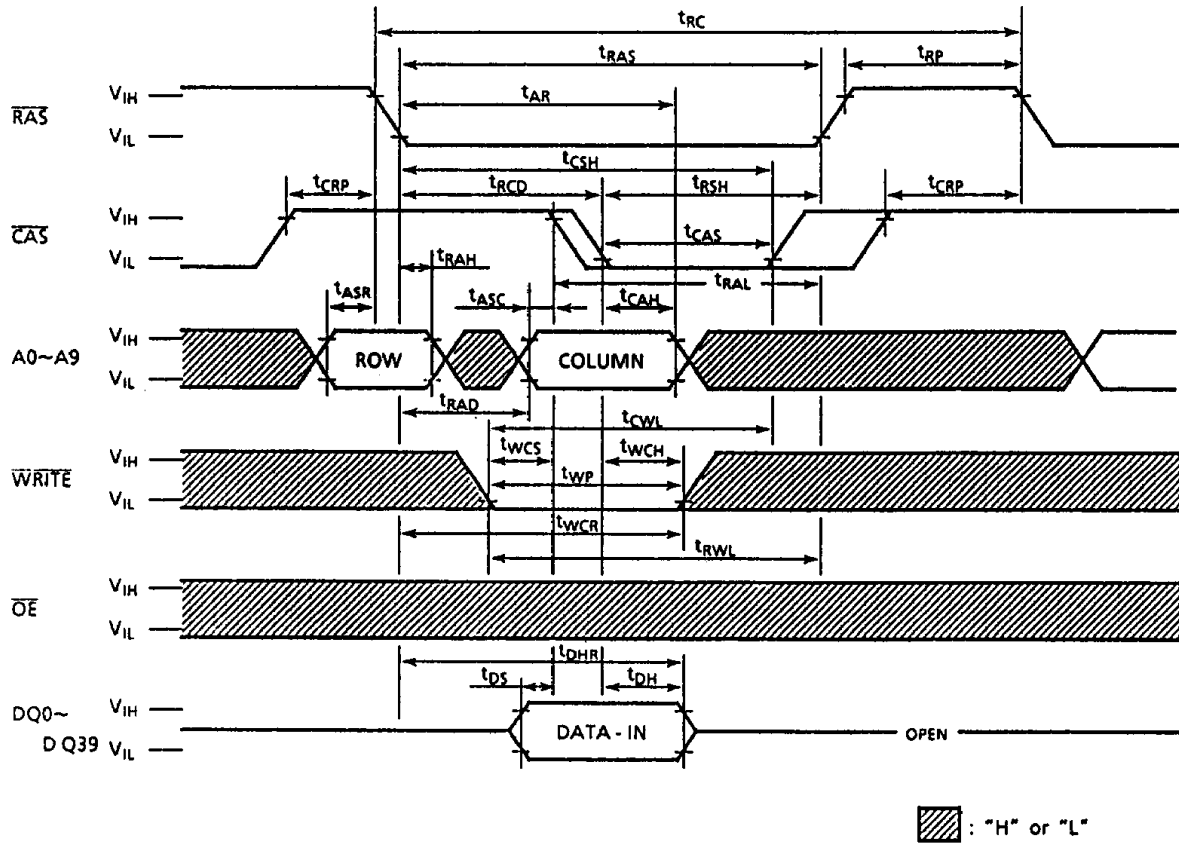
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. ICC_1 , ICC_3 , ICC_4 , ICC_6 depend on cycle rate.
4. ICC_1 , ICC_4 depend on output loading. Specified value are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200 μ s is required after power-up followed by 8 \overline{RAS} cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CAS} before \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required.
7. AC measurements assume $t_r = 5$ ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WRITE} leading edge in read-write cycles.
13. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RCD}(\text{max.})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
15. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RAD}(\text{max.})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .

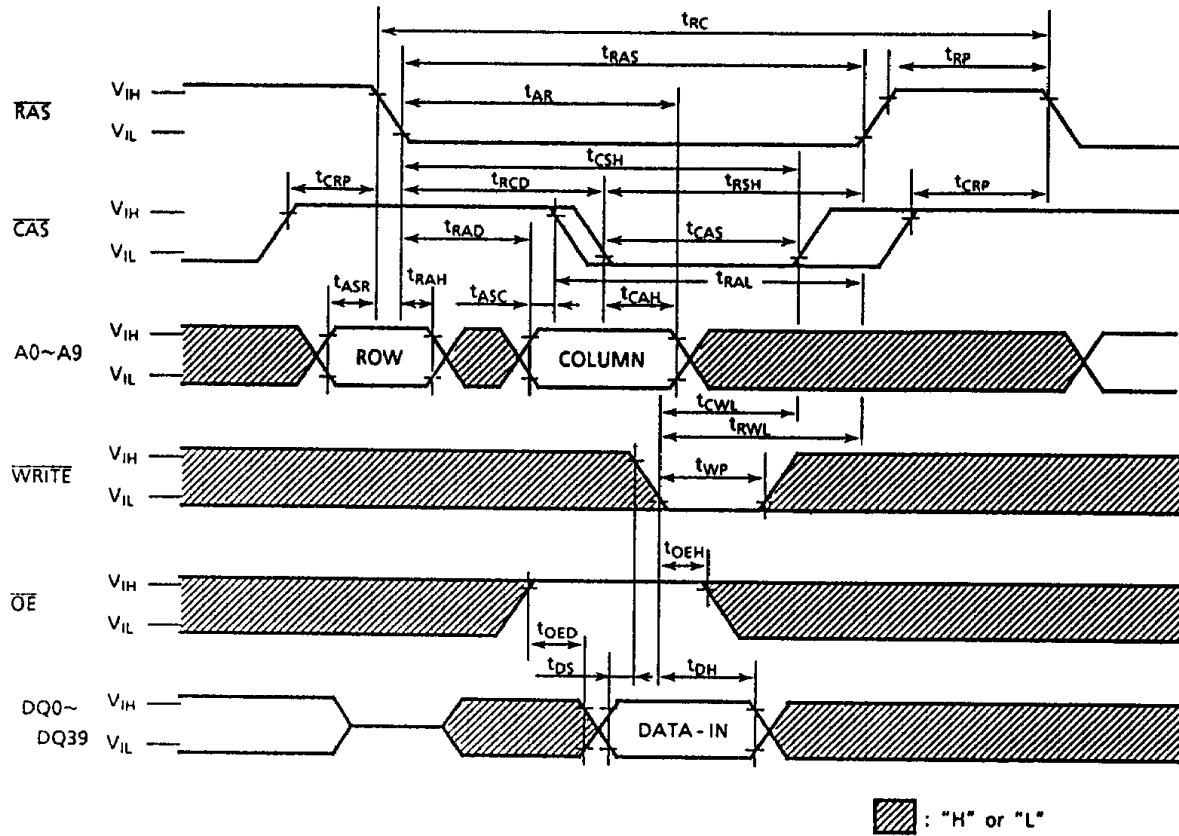
READ CYCLE



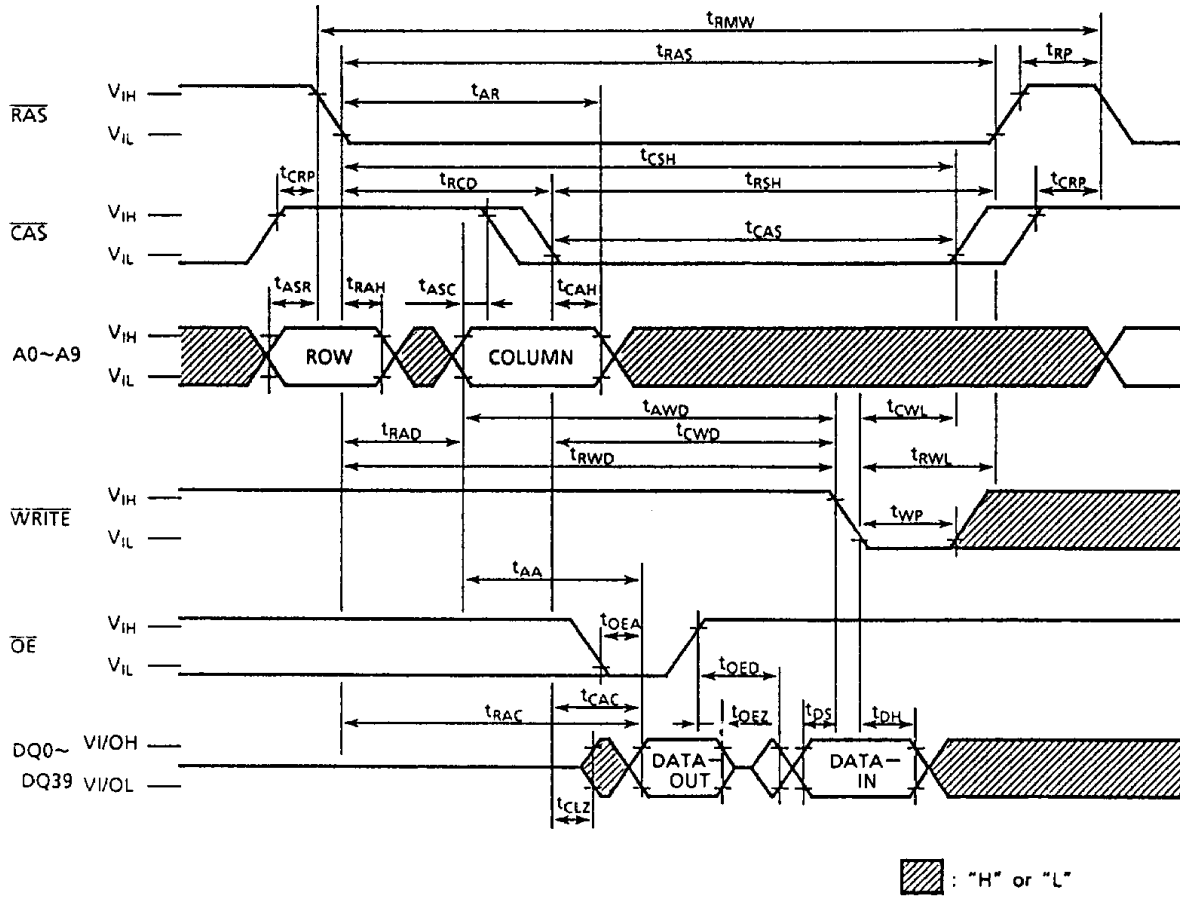
WRITE CYCLE (EARLY WRITE)



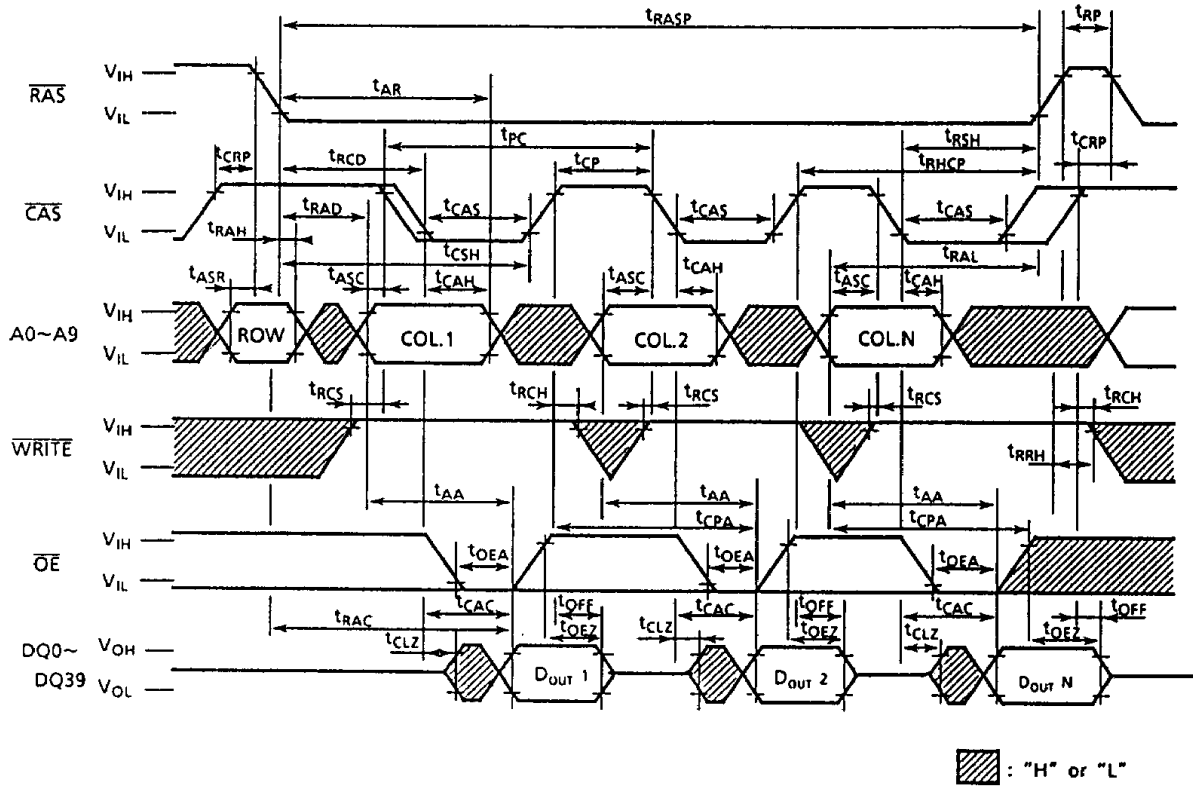
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



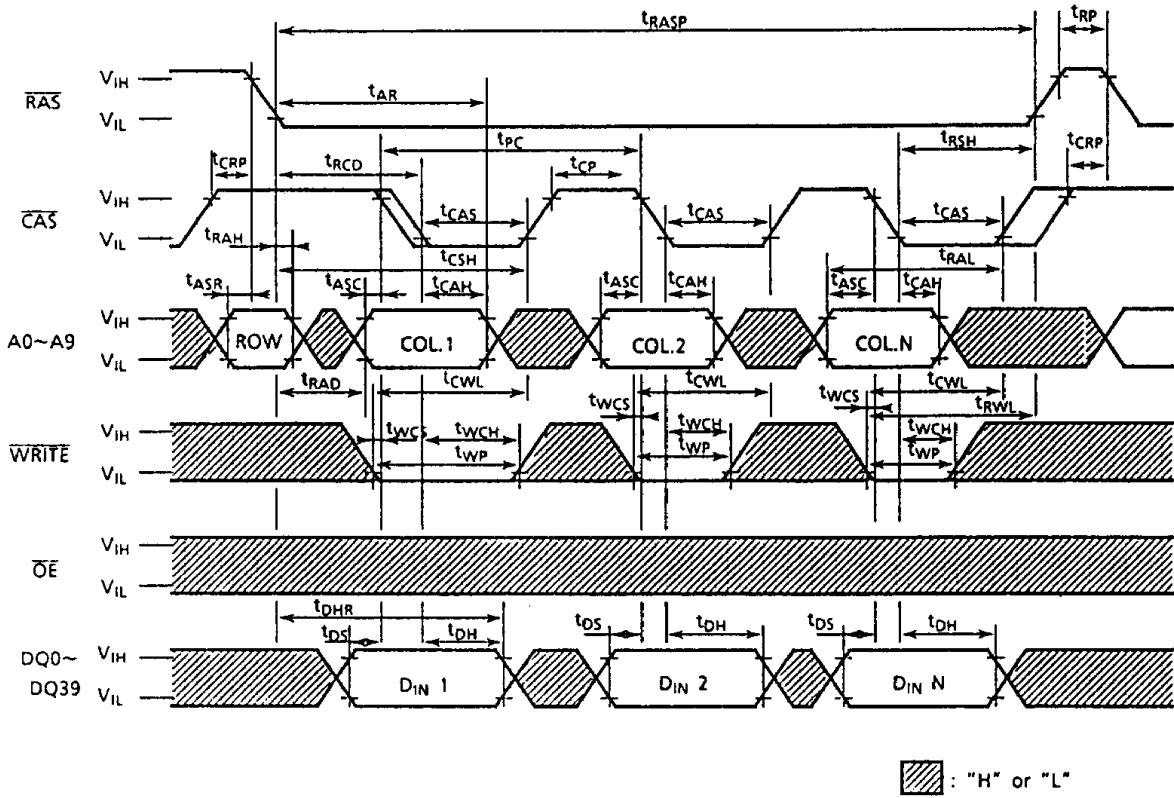
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

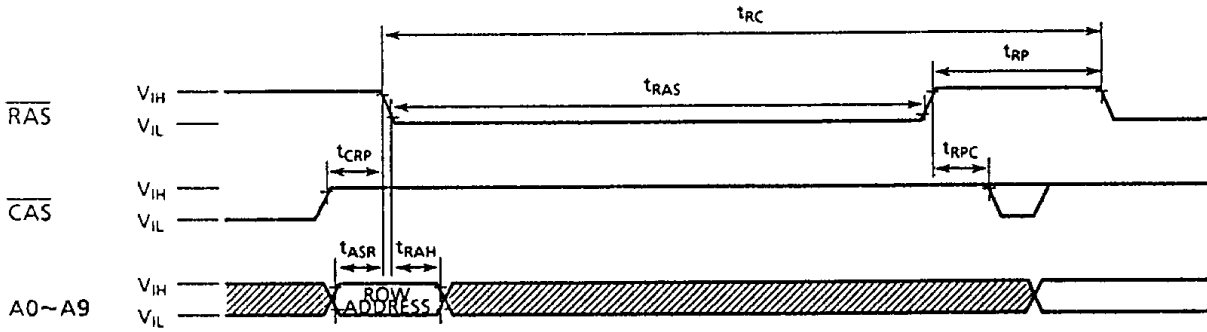


FAST PAGE MODE WRITE CYCLE



THM402020SG-80, 10

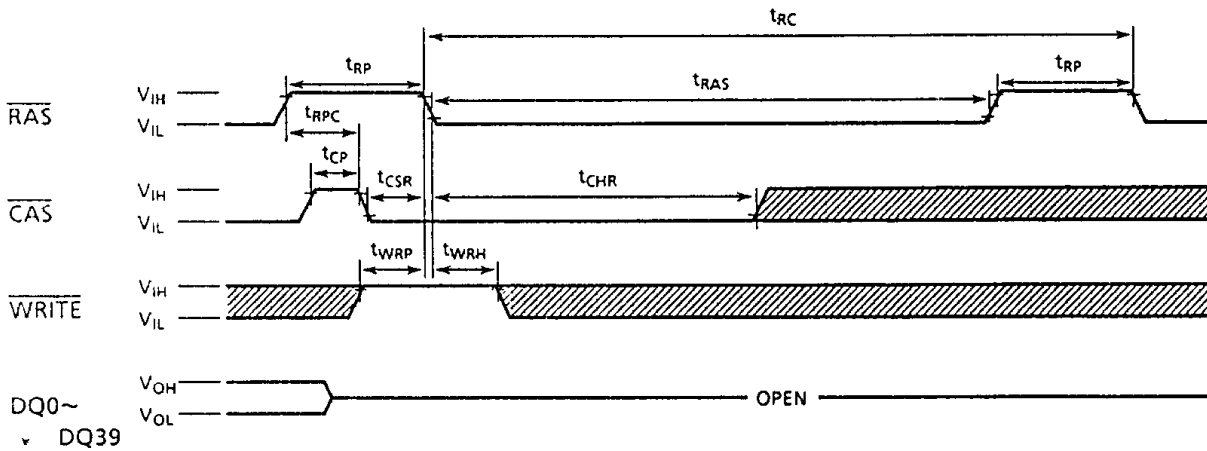
RAS ONLY REFRESH CYCLE



NOTE : $\overline{\text{WRITE}}, \overline{\text{OE}} = \text{"H" or "L"}$

: "H" or "L"

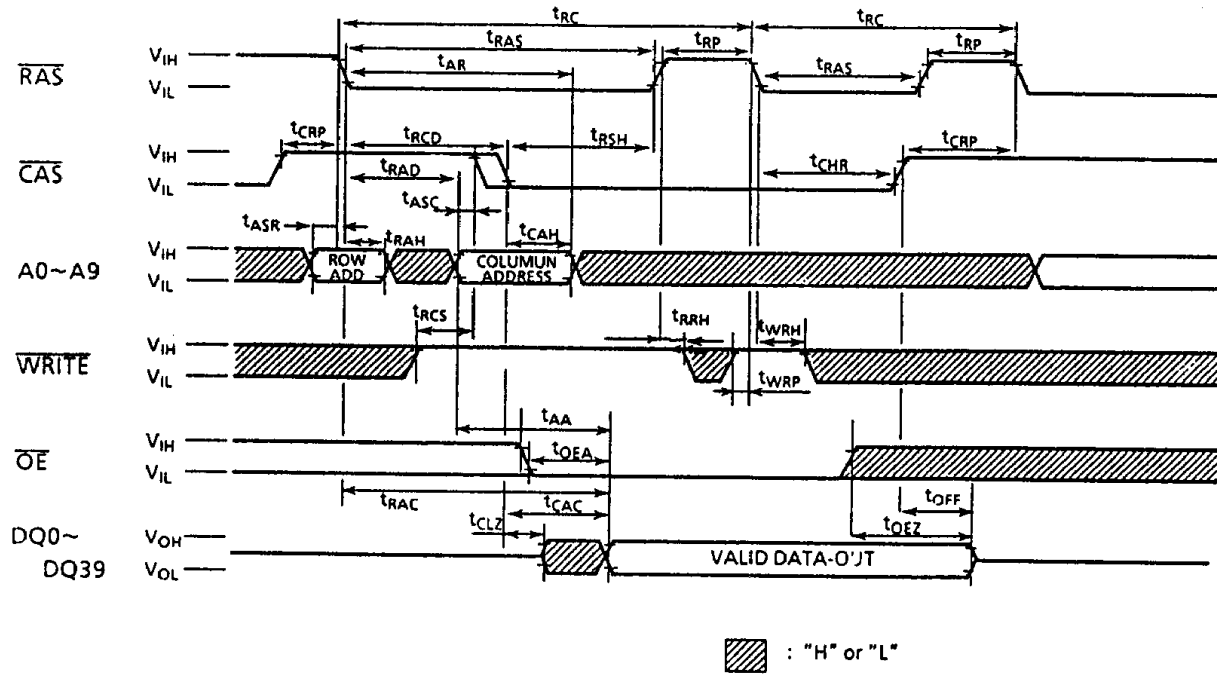
CAS BEFORE RAS REFRESH CYCLE



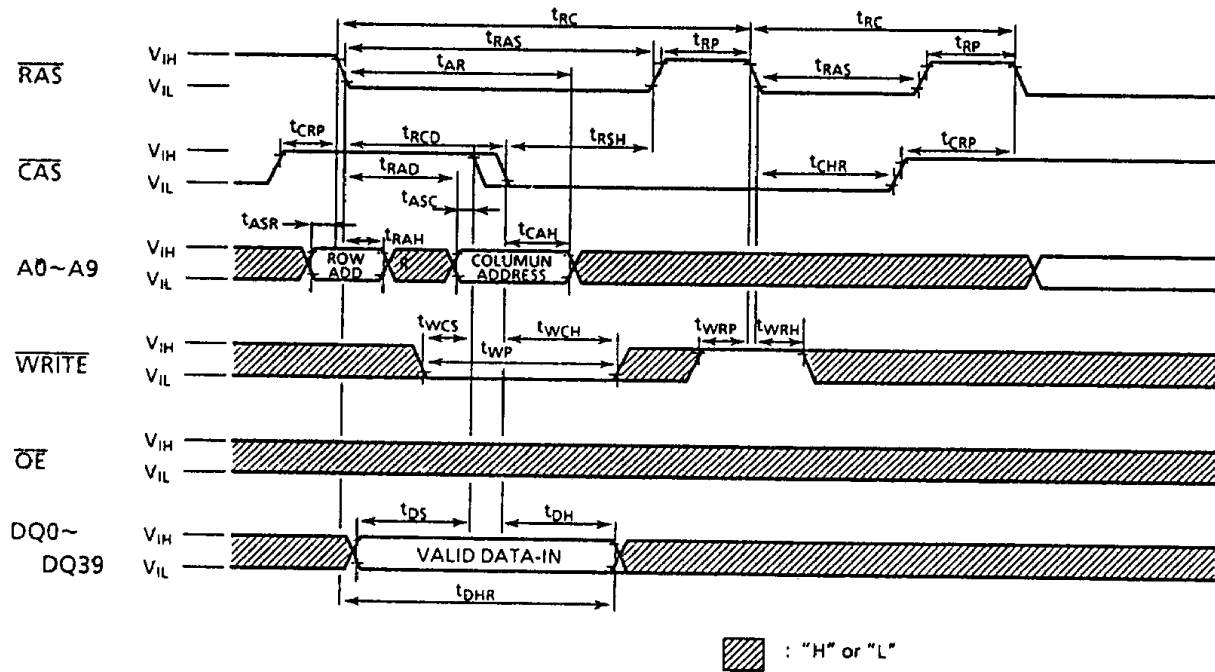
NOTE : $\overline{\text{OE}}, \text{A0} \sim \text{A9} = \text{"H" or "L"}$

: "H" or "L"

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

