

Description

μPD71086 and μPD71087 are 8-bit, bidirectional bus buffer/drivers with three-state outputs. The system bus outputs are noninverted (μPD71086) or inverted (μPD71087). These devices are used to expand CPU bus drive capability. The input/output lines are isolated from \overline{OE} and $\overline{BUFR/W}$ switching noise.

Features

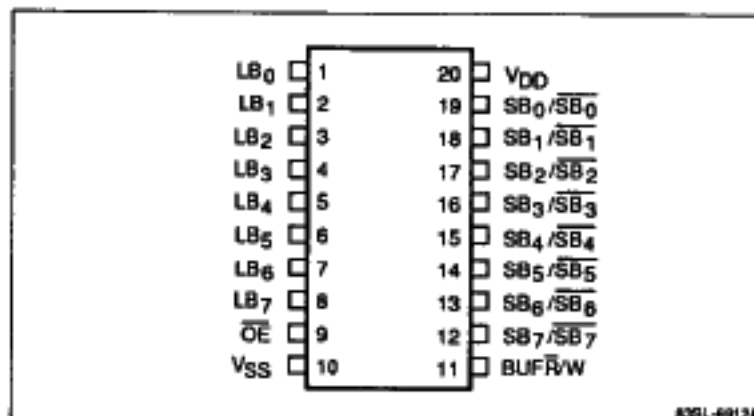
- CMOS technology
- Bidirectional 8-bit parallel bus buffer
- Three-state output
- High system bus-drive capability ($I_{OL} = 12 \text{ mA}$)
- Compatible with μPD70108/116, μPD70208/216, and other CMOS or NMOS designs
- μPD71086: noninverted system bus output
μPD71087: inverted system bus output
- Single +5 V ± 10% power supply
- Industrial temperature range: -40 to +85°C

Ordering Information

Part Number	Package	Output
μPD71086C	20-pin plastic DIP (300 mil)	Noninverted
G	20-pin plastic SOP	
μPD71087C	20-pin plastic DIP (300 mil)	Inverted
G	20-pin plastic SOP	

Pin Configurations

20-Pin Plastic DIP and SOP



Pin Identification

Symbol	Function
LB_7-LB_0	CPU local I/O data bus, bits 7-0
$SB_7-SB_0/\overline{SB}_7-\overline{SB}_0$	System I/O data bus, bits 7-0; noninverted (μPD71086) or inverted (μPD71087)
\overline{OE}	Output enable input
$\overline{BUFR/W}$	Buffer read/write input
V_{DD}	+5 V power supply
V_{SS}	Ground

PIN FUNCTIONS

LB₇-LB₀ (Local Data Bus)

LB₇-LB₀ are three-state inputs/outputs that connect to the CPU local data bus. They move data between the CPU and memory, I/O, or other peripherals. Data read/write mode is controlled by the BUF \bar{R}/W signal input.

SB₇-SB₀/SB $\bar{7}$ -SB $\bar{0}$ (System Data Bus)

SB₇-SB₀/SB $\bar{7}$ -SB $\bar{0}$ are three-state inputs/outputs that connect to the system bus, along with the memory, I/O, or other peripherals. The μPD71086 causes no signal inversion, the μPD71087 inverts the signal. Input/output condition is determined by BUF \bar{R}/W status. See table 1.

OE (Output Enable)

OE input controls the output buffers. When OE is high, all output buffers go to the high-impedance state. When OE is low, data is output from the buffers specified by the BUF \bar{R}/W signal.

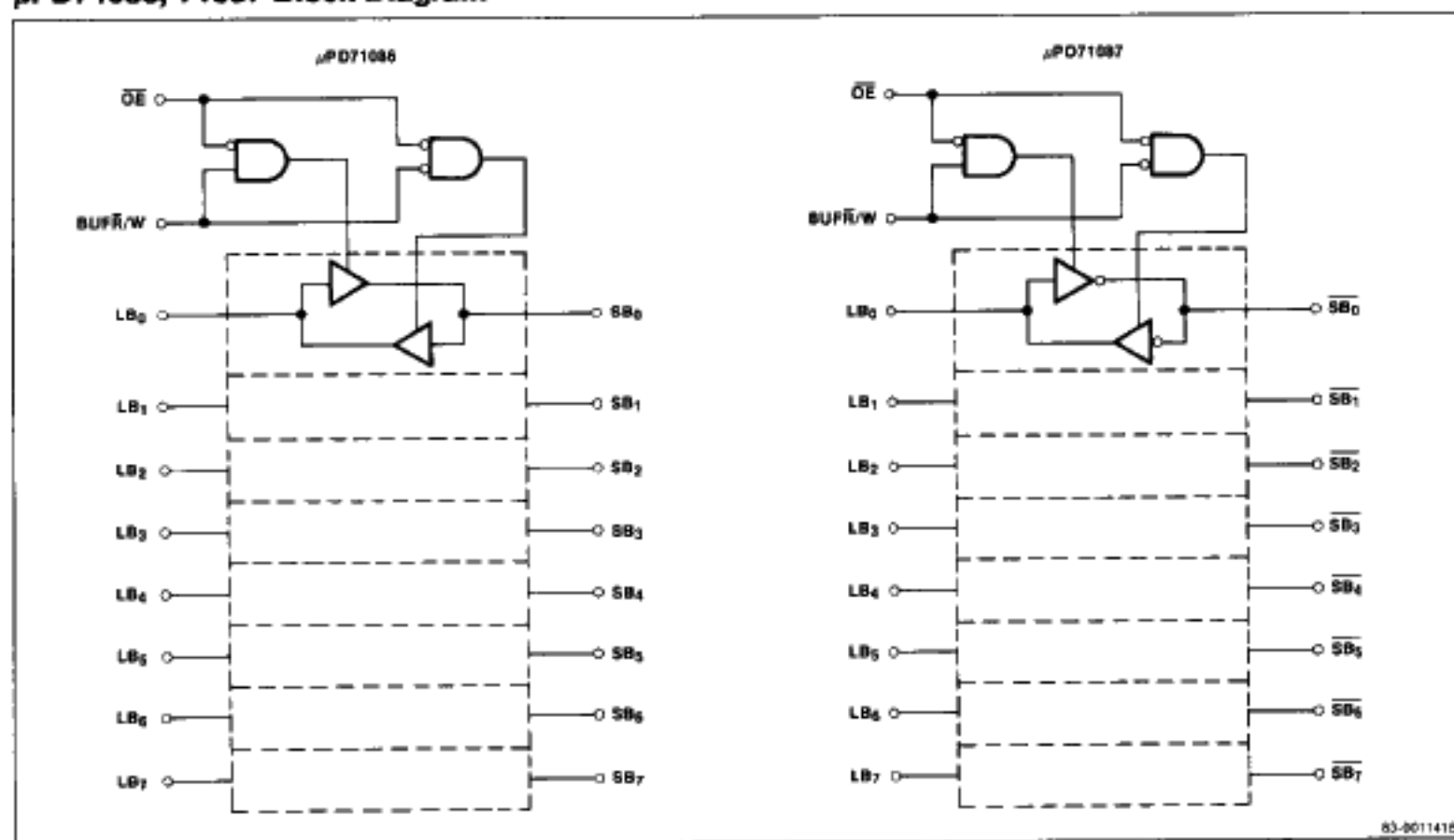
BUF \bar{R}/W (Buffer Read/Write)

The data read/write mode is controlled by the BUF \bar{R}/W signal input. When BUF \bar{R}/W is high, LB lines are inputs and SB lines are outputs. When BUF \bar{R}/W is low, SB lines are inputs and LB lines are outputs. See table 1.

Table 1. Data Read/Write Mode

OE	BUF \bar{R}/W	LB Pins	SB/SB $\bar{}$ Pins	Mode
Low	Low	Output	Input	System bus to local bus
Low	High	Input	Output	Local bus to system bus
High	Don't care	High-Z	High-Z	

μPD71086, 71087 Block Diagram



83-9011415

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$; $V_{SS} = 0\text{ V}$

Power supply voltage, V_{DD}	-0.5 to +7.0 V
Input voltage, V_I	-1.0 to $V_{DD} + 1.0\text{ V}$
Output voltage, V_O	-0.5 to $V_{DD} + 0.5\text{ V}$
Power dissipation, P_D	
DIP	500 mW
SOP	200 mW
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Capacitance

$T_A = 25^\circ\text{C}$; $V_{DD} = +5\text{ V}$

Parameter	Symbol	Min	Max	Units	Conditions
Input capacitance	C_{IN}	24		pF	$f_c = 1\text{ MHz}$

DC Characteristics

$T_A = -45$ to +85°C; $V_{DD} = 5\text{ V} \pm 10\%$

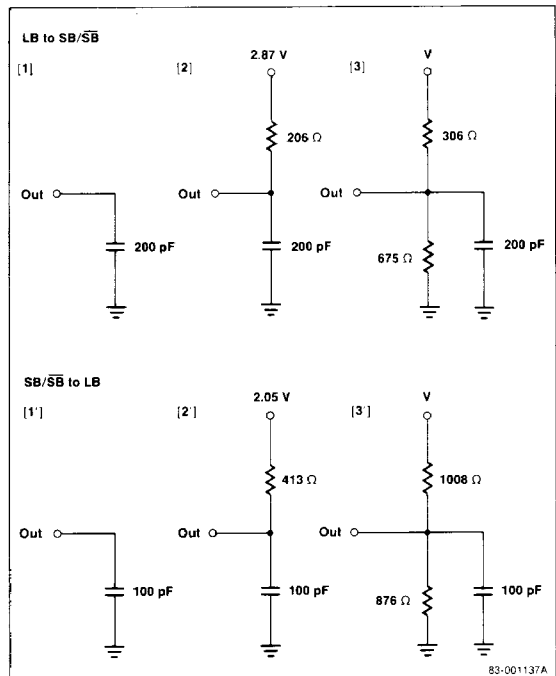
Parameter	Symbol	Min	Max	Units	Conditions
Input voltage high	V_{IH}	2.2		V	
Input voltage low	V_{IL}	0.8		V	
Output voltage high	V_{OH}	$V_{DD} - 0.8$		V	$I_{OH} = -4\text{ mA}$
Output voltage low	V_{OL}	0.45		V	LB, $I_{OL} = 4\text{ mA}$
Output voltage low	V_{OL}	0.45		V	SB, $I_{OL} = 12\text{ mA}$
Input leakage current	I_{IL}	-1.0	1.0	μA	$V_I = V_{DD}, V_{SS}$
Leakage current, high impedance	I_{OFF}	-10	10	μA	$\overline{OE} = V_{DD}$
Power supply current (static)	I_{DD}	80		μA	$V_I = V_{DD}, V_{SS}$
Power supply current (dynamic)	I_{DDdyn}	40		mA	$f_{in} = 2\text{ MHz}$

AC Characteristics

$T_A = -40$ to 85°C; $V_{DD} = 5\text{ V} \pm 10\%$

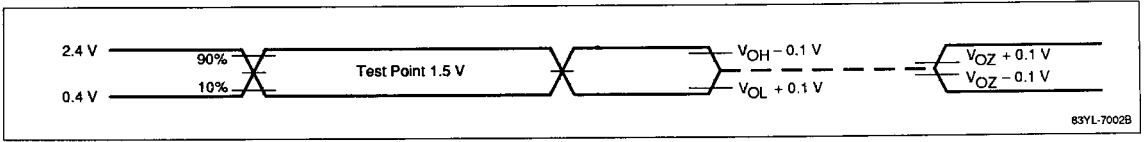
Parameter	Symbol	Min	Max	Units	Conditions
Input to output delay	t_{DIO}	5	40	ns	Load (1), (1') and (2), (2')
BUF \overline{R} /W hold time from \overline{OE}	t_{HCTRW}	5		ns	
BUF \overline{R} /W setup time to \overline{OE}	t_{SRWCT}	10		ns	
Data float time from \overline{OE}	t_{FCTO}	5	30	ns	Load (3) and (3')
Data output delay from \overline{OE}	t_{DCTO}	10	40	ns	
Signal rise time	t_R		20	ns	0.8 to 2.0 V
Signal fall time	t_F		12	ns	2.0 to 0.8 V

Loading Circuit for AC Test



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AC Test Voltages



Timing Waveforms

