FREEDM PRODUCT FAMILY

TECHNICAL OVERVIEW

PRELIMINARY

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REVISION HISTORY

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CONTENTS

1 INTRODUCTION

Significant developments have occurred in networking industry recently that are driving the need for a greater communications capacity in the wide area network (WAN). One of the driving forces is the need for more bandwidth to inter-connect two or more LANs across a metropolitan area network (MAN) or WAN. This bandwidth requirement has advanced to the point that it is straining the networking capacity provided by existing equipment. As such, network equipment such as frame relay switches, multi-service ATM switches, integrated access devices (IAD), and remote access concentrators are pushed to provide more network bandwidth by supporting more physical links, logical channels and latency sensitive data such as voice and video.

This document describes how the FREEDM product family and other high density physical layer devices from PMC-Sierra address the need for more bandwidth for WAN equipment such as frame relay switch, multi-service ATM switch, and remote access concentrator by significantly improve the port density for a wide range of communication equipment. The document answers the following questions:

- What function do the FREEDM product variants fulfill in the overall system architecture?
- What are the primary applications and equipment that the FREEDM devices are designed for?
- What PMC-Sierra products and other components interwork with the FREEDM product family.

This document is a companion of, but subordinate to the FREEDM datasheets:

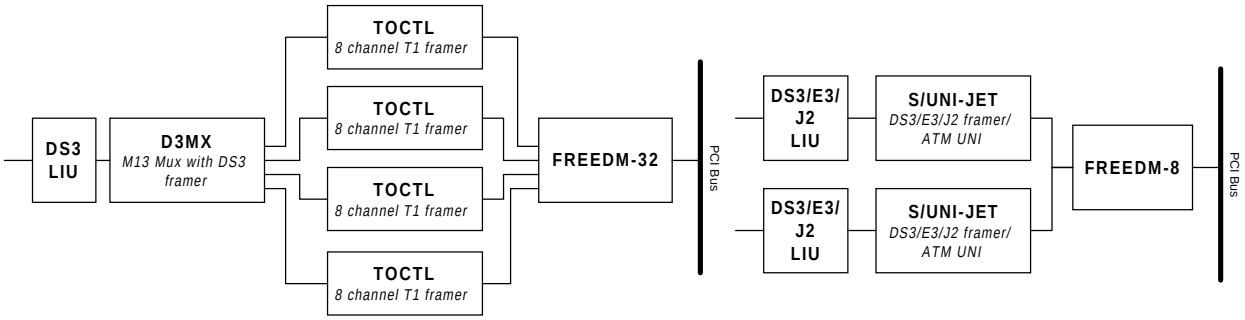
- FREEDM-32P672 Datasheet, PMC-990262
- FREEDM-32A672 Datasheet, PMC-990263
- FREEDM-84P672 Datasheet, PMC-990445
- FREEDM-84A672 Datasheet, PMC-990114

If there appear to be differences, contradictions, or omissions in this Technical Overview the reader is advised that the datasheets take precedence.

2 FREEDM PRODUCT FAMILY

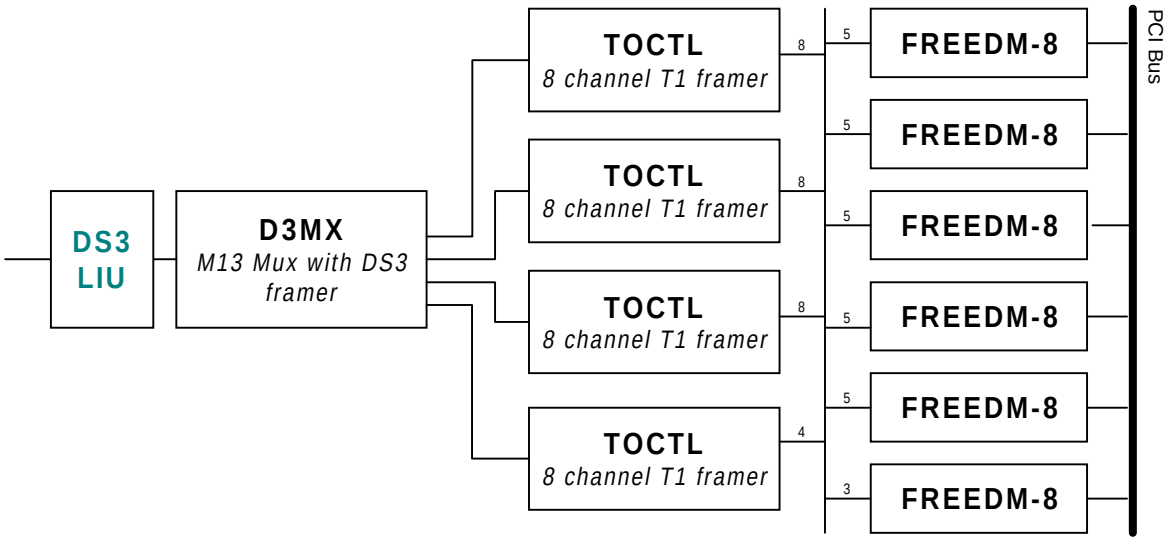
In 1997, PMC-Sierra introduced the high performance packet processor, FREEDM-32 and FREEDM-8, to address remote internet access bandwidth limitations. These devices increased the port density of frame relay switches, routers and remote access concentrators such that more physical links and HDLC channels can be supported on the same board space as before.

The FREEDM-32 and FREEDM-8 support multiple physical link configurations, ranging from 8 or 32 links at 56 Kbit/s each to 2 High Speed Serial Interfaces (HSSI) at 52 Mbps each. The density and flexibility offered by FREEDM-32 and FREEDM-8 enable a network designer to develop a single platform that can be reused across multiple port cards with different physical interfaces. For example, FREEDM-32 can be used with 4 TOCTL and a D3MX to support a channelized DS3 interface. FREEDM-8 can be used with two S/UNI-JET devices to support 2 unchannelized DS3/E3/J2 interfaces.

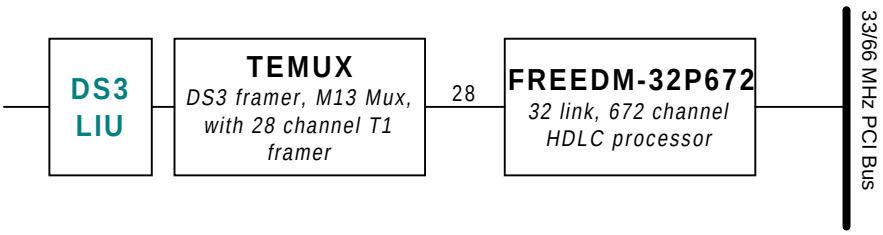


The explosive growth of Internet traffic and the popularity of WAN services such as the frame relay service are collectively pushing network architects to design higher and higher density port cards. The challenge is often compounded by the need to implement the higher density port card on the same form-factor and within the same power budget as its lower density predecessor.

PMC-Sierra introduces the second generation FREEDM products to enable the design of high density, low power and low latency port cards for frame relay, routers and remote access concentrator equipment. For a remote access concentrator, the number of devices required to support a fully channelized DS3 with 672 HDLC channels can be drastically reduced by using a FREEDM-32P672 and a TEMUX in place of 6 FREEDM-8, 4 TOCTL and a D3MX.

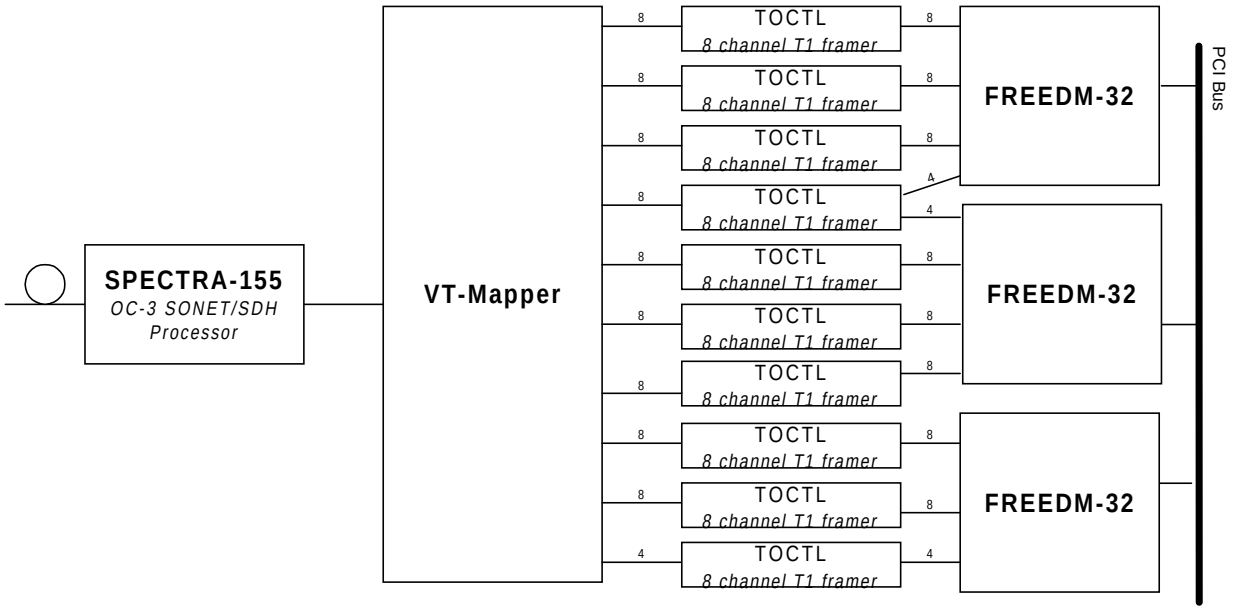


First generation solution

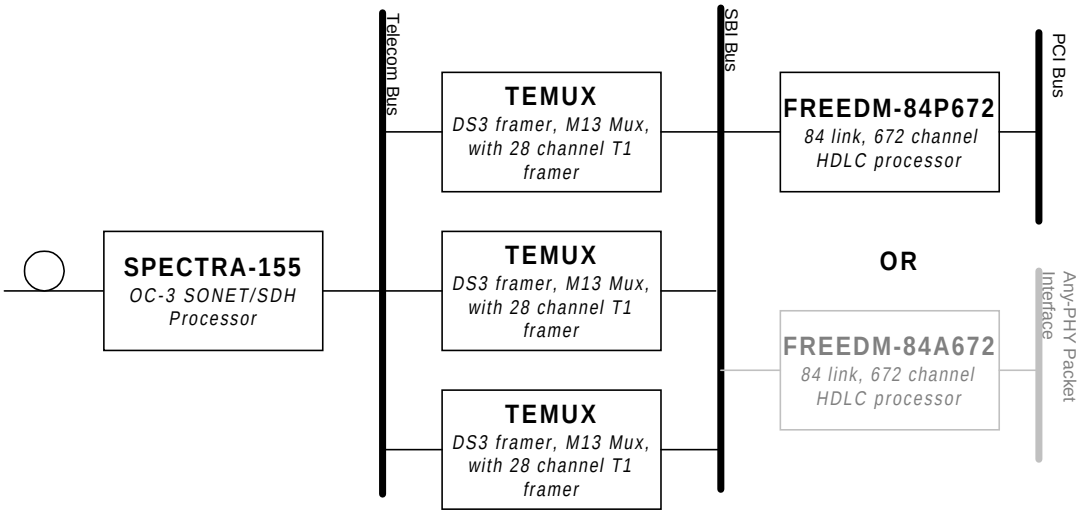


Second generation solution

For a frame relay switch, the number of devices to support a channelized OC-3 down to DS1 (84 HDLC channels) can be reduced by using SPECTRA-155, 3 TEMUX and a FREEDM-84P672 in place of SONET/SDH processor, VT-mapper, 11 TOCTL and 3 FREEDM-32.



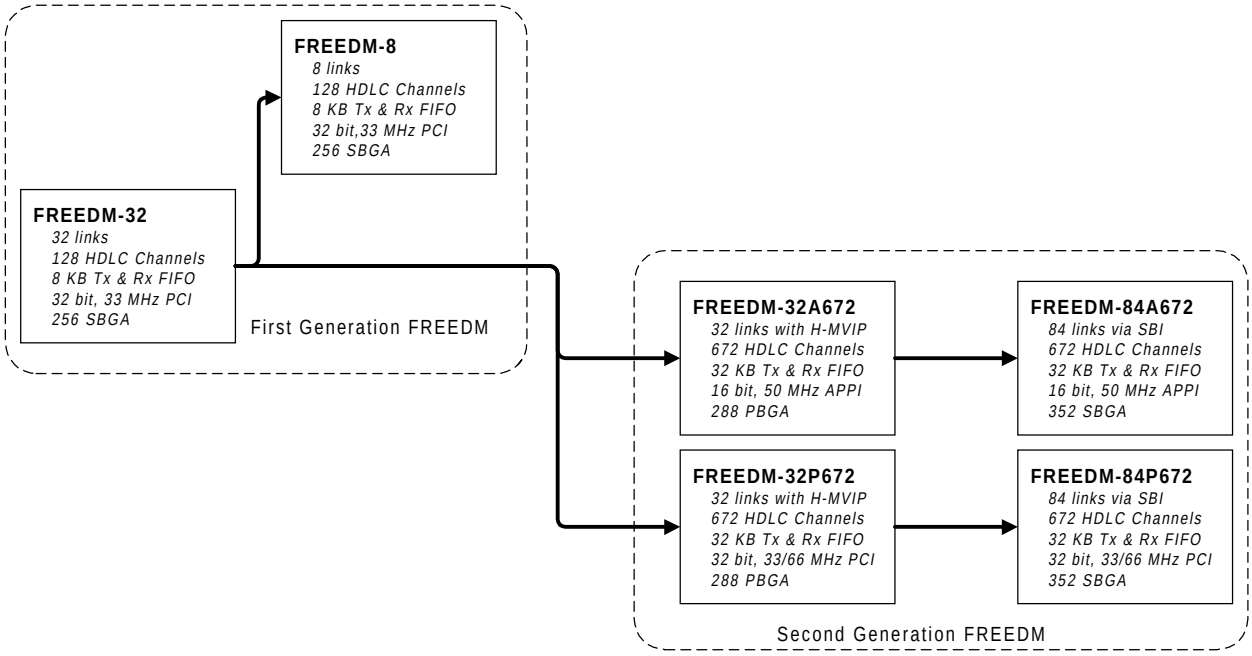
First generation solution



Second Generation Solution

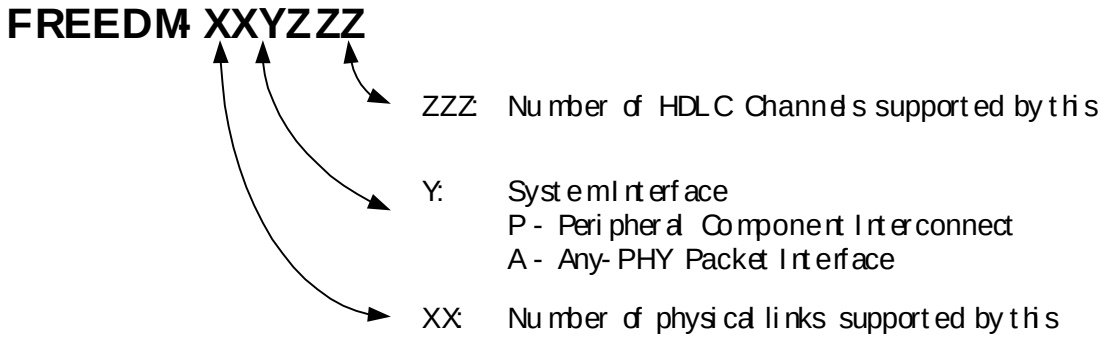
2.1 FREEDM Product Family

The members of the FREEDM product family are presented below:



Naming convention

For the first generation devices, the trailing number refers to the number of physical links supported by that device. The second generation devices are identified using the following naming convention:



There are 4 product variants in the second generation FREEDM product family. These product variants are specifically designed to address the unique requirements of different networking equipment. For example, the dial-access equipment terminates a large number of communication sessions with remote users. A fully channelized DS3

link carries 28 T1s and each T1 in turn carries 24 DS0 timeslots. Therefore, the total number of DS0s in a fully channelized DS3 is 672. If each DS0 carries an independent PPP session, a total of 672 HDLC channels will be required to support a fully channelized DS3 port card. The FREEDM-32P672 supports 32 physical link and 672 HDLC channels and is ideal for a channelized DS3 card using the PCI as its system bus interface.

At the edge of the WAN network where frame relay and multiservice ATM switches are located, the primary challenge is to support as many physical links as possible. A physical link can be T1/J1, E1, fractional DS3/E3 or an unchannelized DS3/E3. Unlike the dial-access equipment, only a fraction of the links are channelized. Therefore it is not necessary for these equipment to assign one HDLC channel per DS0. FREEDM-84A672 and FREEDM-84P672 are ideal for the frame relay and multiservice ATM switches as they support 84 links and 672 HDLC channels on a single device.

2.1.1 Selection Criteria

This section presents a general method to determine which one of the FREEDM product family is more suitable for a given application. This method requires the designer to specify the following selection criteria:

1. What is the preferred system bus type?
2. How many physical links are required?
3. How many HDLC channels are required?
4. What is the aggregate bandwidth?

By answering the above questions, the designer can use the reference guide to select the most appropriate FREEDM device to use.

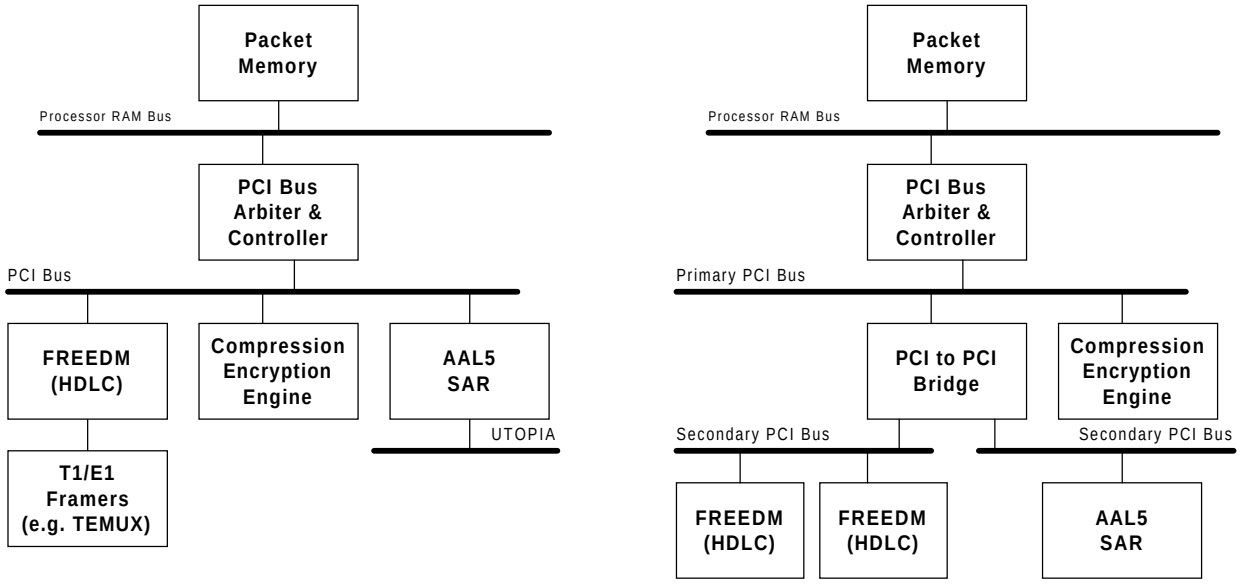
2.1.1.1 System Bus

	FREEDM-8	FREEDM-32	FREEDM-32A672	FREEDM-32P672	FREEDM-84A672	FREEDM-84P672
PCI Bus	32 bit 33 MHz 5V I/O	32 bit 33 MHz 5V I/O	N/A	32 bit 33/66 MHz 3.3V I/O	N/A	32 bit 33/66 MHz 3.3V I/O
APPI Bus	N/A	N/A	16 bit 50 MHz 3.3V I/O	N/A	16 bit 50 MHz 3.3V I/O	

FREEDM supports two system bus options: The industry standard Peripheral Component Interconnect (PCI) Bus and PMC-Sierra's Any-PHY Packet Interface (APPI).

PCI Bus

PCI is a popular bus that can be used to interconnect devices that are compliant to the PCI Bus Specification. A system architecture that is based on the PCI bus can use off the shelf standard components to implement the required functions.

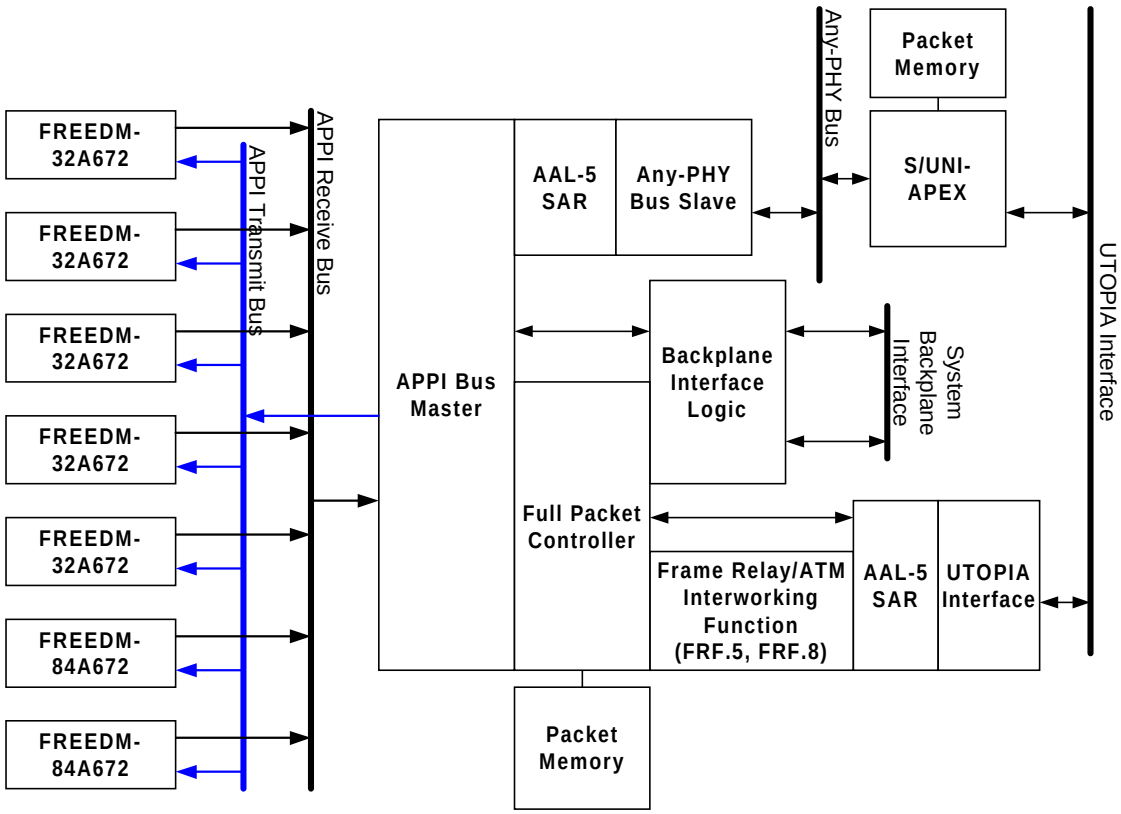


With several peer entities sharing a common bus, it is important to conduct a thorough analysis of the bus performance in order to ensure that a design can meet its target performance. The performance of the PCI bus depends on several variables, such as number of peer devices on a bus segment, packet length, memory read/write latency cycles, DMA overhead cycles and bus arbitration cycles. A number of applications notes are prepared to help the designer analyze and model FREEDM's performance on the PCI bus.

Any-PHY Packet Interface (APPI)

PMC-Sierra developed the APPI bus as a high bandwidth, low latency system bus interface. Modeled after the popular POS-PHY interface used in PPP-over-SONET applications, the APPI is a 16 bit, 50 MHz bus that can support up to 800 Mbps of raw bandwidth. The APPI uses very few overhead cycles to transmit and receive packets and therefore it is suitable for designs that need to scale up to OC-12 (622 Mbps) worth of bandwidth.

Like POS-PHY and UTOPIA bus interfaces, the APPI is a master/slave bus. An external bus master can interface with up to 7 FREEDM-32A672 and FREEDM-84A672 devices to send and receive packets. As the transmit APPI bus operations are independent from the receive operations, the external bus master can be implemented as two physical devices.



By using the APPI as the gateway to the HDLC channels and physical links, the system designer has a number of options to interface with the upper-layer components of the system:

1. Any APPI-to-backplane bridge can be designed by combining the APPI interface logic with the system backplane interface logic. If the traffic shaper at the upstream of the backplane interface can support shaping on a per packet fragment basis, then there is no need for local full packet storage. Alternatively, if the traffic shaper can only shape on a complete packet basis, then local packet storage is required.

2. The S/UNI-APEX is a full-function “packet aware” traffic manager and switch. It supports up to 2,048 channels via an Any-PHY Cell Interface and manages up to 16M byte of data buffer. The S/UNI-APEX can be used with one or more FREEDM-32A672 and FREEDM-84A672 to support many high density,

high bandwidth HDLC applications. A “cut-through” AAL-5 SAR is required to translate the packet fragments from FREEDM to and from the cell interface supported by S/UNI-APEX.

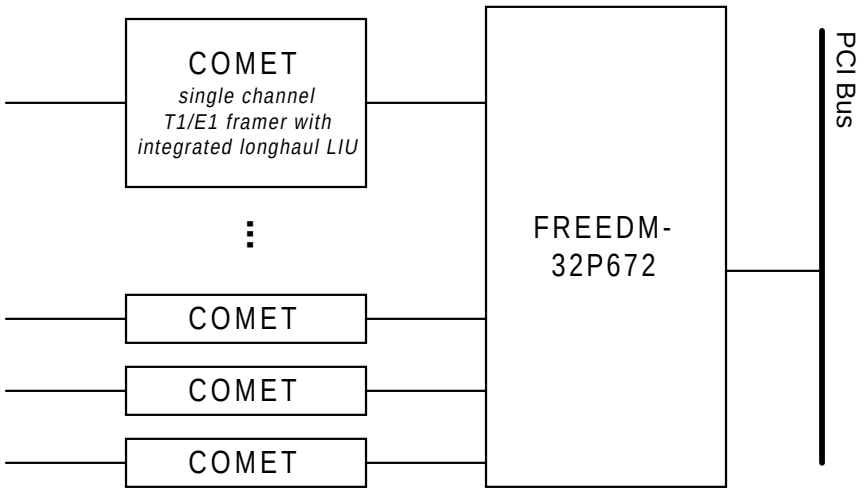
3. In a frame-relay-to-ATM interworking device, the designer can use FREEDM-32A672 or FREEDM-84A672 to perform HDLC functions on the frame relay packets. The de-framed data is then passed to an interworking function block that translates the frame relay packet into ATM cells in accordance with implementation agreements such as Frame Relay Forum’s FRF.5 Networking Interworking, FRF.8 Service Interworking or ATM Forum’s FUNI specifications.

2.1.1.2 Physical Link

	FREEDM-8	FREEDM-32	FREEDM-32A672	FREEDM-32P672	FREEDM-84A672	FREEDM-84P672
Low-speed direct link	8	32	32	32	84 via SBI	84 via SBI
High-speed direct link	2	2	3	3	3 direct or 3 via SBI	3 direct or 3 via SBI
H-MVIP bus	N/A	N/A	32 at 2MHz 8 at 8MHz	32 at 2MHz 8 at 8MHz	N/A	N/A
SBI bus	N/A	N/A	N/A	N/A	19.44MHz SBI	19.44 MHz SBI

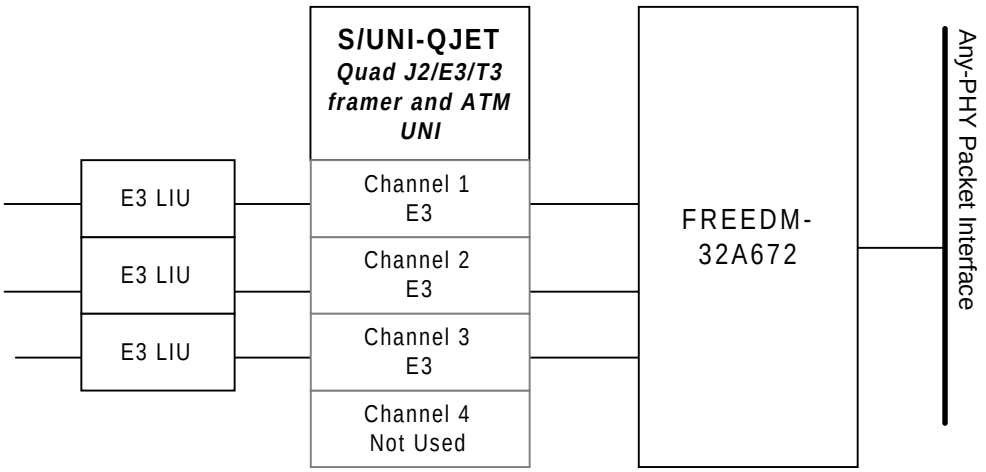
Low-speed direct links

Low-speed-direct links are links that are less than 10 Mbps in bandwidth. Examples of low speed direct link include T1, J1, E1, JT2 and serial links such as V.35 and xDSL. A channelized DS3 contains a bundle of 28 T1s multiplexed using the M13 scheme. In this case, the number of low-speed links is 28. The following figure shows COMET devices connecting to the clock and data interfaces of FREEDM-32P672 as low-speed-direct links.



High-speed direct links:

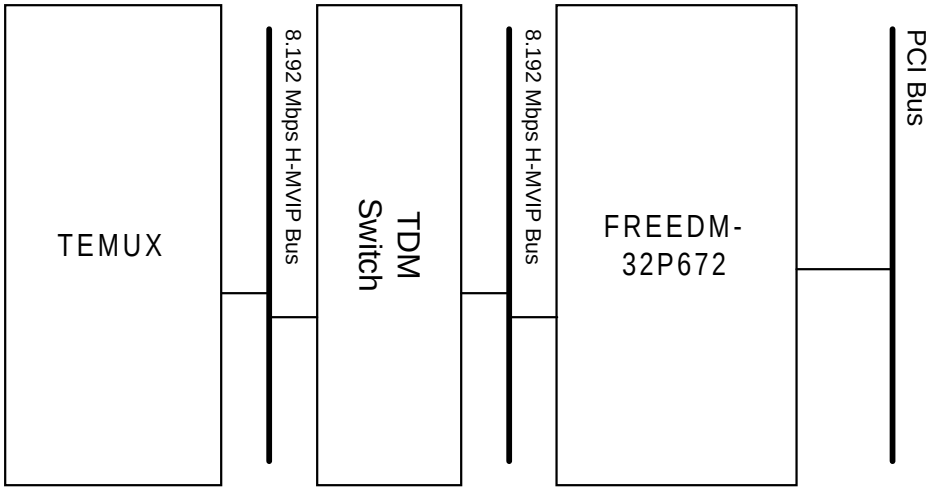
High-speed direct links are physical interfaces that are greater than 10 Mbps and less than 52 Mbps each. Examples of high speed direct links include unchannelized DS3, unchannelized E3 and HSSI. The following figure shows a FREEDM-32A672 supporting 3 unchannelized E3 links and a FREEDM-84A672 support 3 fractional DS3 links.



H-MVIP Bus

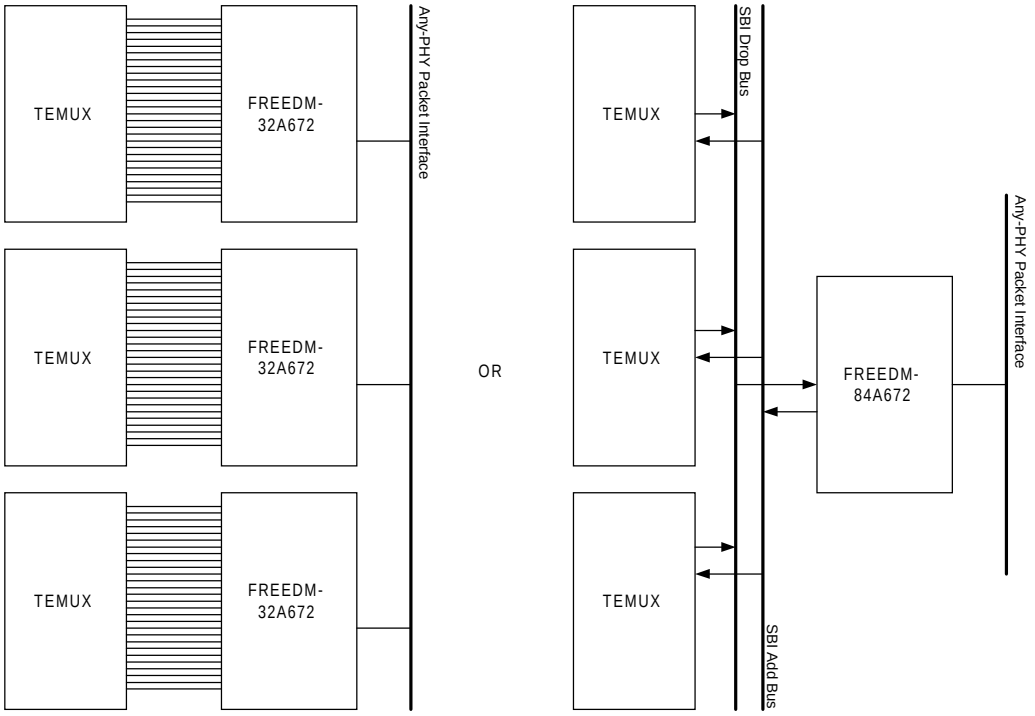
High Speed Multi-Vendor Interface Protocol (H-MVIP) defines a synchronous, time division multiplexed, bus of Nx64 Kbit/s constant bit rate data streams. Each 64 Kbit/s data stream carries an 8-bit bye of HDLC traffic and is characterized by 8KHz framing. H-MVIP supports higher bandwidth applications on existing telephony networks by fitting more time-slots into a 125 µS frame. The FREEDM-32A672 and FREEDM-32P672 support H-MVIP data rates of 2.048 Mbps and 8.192 Mbps with 32 or 128 time-

slots per frame and associated clocking frequencies of 4.192 and 16.384 MHz respectively. The following example shows TEMUX and FREEDM-32P672 interfacing to a TDM switch fabric via an 8.192 Mbps H-MVIP bus.



SBI Bus

The Scaleable Bandwidth Interconnect (SBI) is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links. The parallel SBI bus reduces the complexity of interconnecting multiple low-speed direct links between the physical layer device and the data link layer device. The following example shows two ways to support 84 T1 links: On the left hand side 3 TEMUX are connected to 3 FREEDM-32A672 via 84 sets of low-speed direct links. The large number of physical links between the physical layer device and the data link layer device can be replaced with the parallel SBI bus as illustrated on the right hand side of this figure.



The SBI multiplexing structure is modeled on the SONET/SDH standards. The SONET/SDH virtual tributary structure is used to carry T1/J1 and E1 links. Unchannelized DS3 payloads follow a byte synchronous structure modeled on the SONET/SDH format. A design that uses FREEDM-84A672 and 3 TEMUX can support 3 unchannelized DS3 or 84 T1/J1 links or 63 E1 links. Different interfaces can be intermixed on a per Synchronous Payload Envelope (SPE) basis. Thus, one design can support one unchannelized DS3, 28 T1s and 21 E1s.

2.1.1.3 HDLC Channels

	FREEDM-8	FREEDM-32	FREEDM-32A672	FREEDM-32P672	FREEDM-84A672	FREEDM-84P672
HDLC Channels	128	128	672	672	672	672

In an unchannelized application, each link is mapped to a unique logical channel. For a channelized application, a T1/J1 link carries 24 timeslots (each at 64 Kbps). Each of the timeslot can be carrying packet data independent from all other timeslots. Therefore, each channelized T1 can carry up to 24 HDLC channels (at DS0 rate). Equivalently, there are 32 timeslots in a channelized E1 and hence each channelized E1 can carry up to 32 HDLC channels (at DS0 rate).

The number of logical channels required by network equipment depends on where in the network is the equipment located. Typically, the closer to the end-users, the more

number of HDLC channels are required. For example, a remote access concentrator that provides dial-access service to remote users would require one logical channel per DS0 timeslot. That is, for a channelized DS3 service 672 HDLC channels are required. The remote access concentrator would terminate the packet data and consolidate the multiple low-speed dial-access traffics onto a faster pipe such as unchannelized T1/E1 or DS3/E3 frame relay service.

A frame relay switch typically supports unchannelized T1/E1 services. Therefore the number of HDLC channels required by a frame relay switch is much lower than that required by the remote access concentrator.

2.1.1.4 Aggregate Bandwidth

	FREEDM-8	FREEDM-32	FREEDM-32A672	FREEDM-32P672	FREEDM-84A672	FREEDM-84P672
Low-speed direct Link (Mbps full duplex)	64	64	64	64	155	155
High-speed direct link (Mbps full duplex)	104	104	104	104	155	155

The aggregate bandwidth is the sum of the bandwidth carried by all the physical links that are connected to a single FREEDM device. For example, 28 T1s connected to a single FREEDM would have an aggregate bandwidth of 28*1.544Mbps=43.232Mbps.

2.1.2 FREEDM Selection Guide

The FREEDM selection guide is the combination of individual selection tables derived from the system bus, physical link, HDLC channel, and aggregate bandwidth sections. The remainder of this chapter will use this selection guide to determine the most suitable FREEDM device for a number of representative applications.

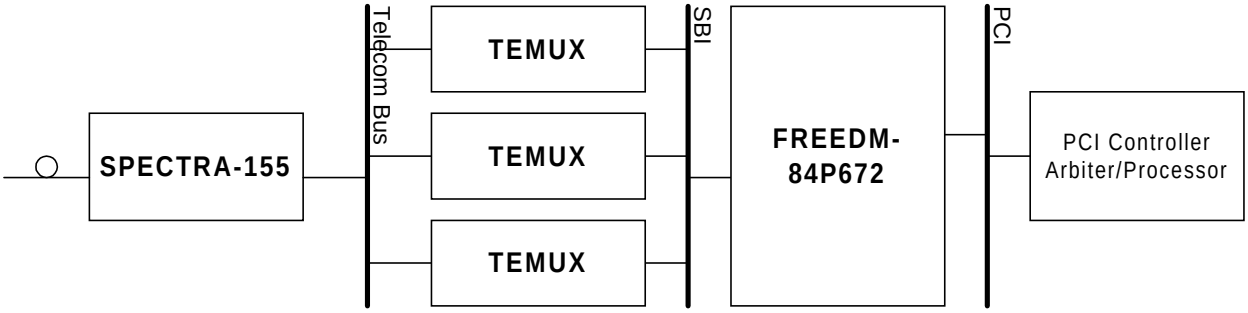
	FREEDM-8	FREEDM-32	FREEDM-32A672	FREEDM-32P672	FREEDM-84A672	FREEDM-84P672
PCI Bus	32 bit 33 MHz 5V I/O	32 bit 33 MHz 5V I/O	N/A	32 bit 33/66 MHz 3.3V I/O	N/A	32 bit 33/66 MHz 3.3V I/O
APPI Bus	N/A	N/A	16 bit 50 MHz 3.3V I/O	N/A	16 bit 50 MHz 3.3V I/O	
Low-speed direct link	8	32	32	32	84 via SBI	84 via SBI
High-speed direct link	2	2	3	3	3 direct or 3 via SBI	3 direct or 3 via SBI
H-MVIP bus	N/A	N/A	32 at 2MHz 8 at 8MHz	32 at 2MHz 8 at 8MHz	N/A	N/A
SBI bus	N/A	N/A	N/A	N/A	19.44MHz SBI	19.44 MHz SBI
HDLC Channels	128	128	672	672	672	672
Low-speed direct Link aggregate bandwidth (Mbps full duplex)	64	64	64	64	155	155
High-speed direct link aggregate bandwidth (Mbps full duplex)	104	104	104	104	155	155

2.1.2.1 Frame Relay Switch - Channelized 3*DS3

A frame relay switch needs to implement a channelized OC-3 port card for the SONET/SDH network. On average, the channelized OC-3 link needs to support 6*DS0 timeslots per HDLC channel[1]. The choice of the system bus is a 66MHz, 32 bit PCI bus. The selection criteria is summarized in the following table:

Item	Value	Note
System Bus Option	66 MHz, 32 bit PCI bus	As per specification.
Number of physical links.	84 T1s (SONET) or 63 E1s (SDH)	Each SONET STS-3 carries 84 T1s via the VT1.5 mapping. The SDH STM-0 carries 63 E1s via the VT2.0 mapping.
Number of HDLC channels	336	On average, a HDLC channel is required for every 6*DS0 timeslots. There are 24 timeslots in a T1; therefore 4 HDLC channels are required per T1. There are 84 physical links in this system and therefore 84*4=336 HDLC channels are required.
Aggregate Bandwidth	129.7 Mbps	The sum of all physical links is 84*1.544Mbps = 129.7 Mbps.

Applying the selection criteria to FREEDM Selection Guide shows that FREEDM-84P672 meets all the selection criteria and is the densest solution for this application. One FREEDM-84P672 can interface directly with 3 TEMUX across the SBI bus to support 3 channelized DS3 for the frame relay switch.



[1] Typically, the frame relay switch will support some number of T1/E1 links, some number of fractional T1/E1 links (N*DS0) and some number of DS0 channels. The total number of HDLC channels required for 84 T1 links or 63 E1 links is 336 HDLC channels or on average 4 HDLC channels per T1 link or 6*DS0 per HDLC channel.

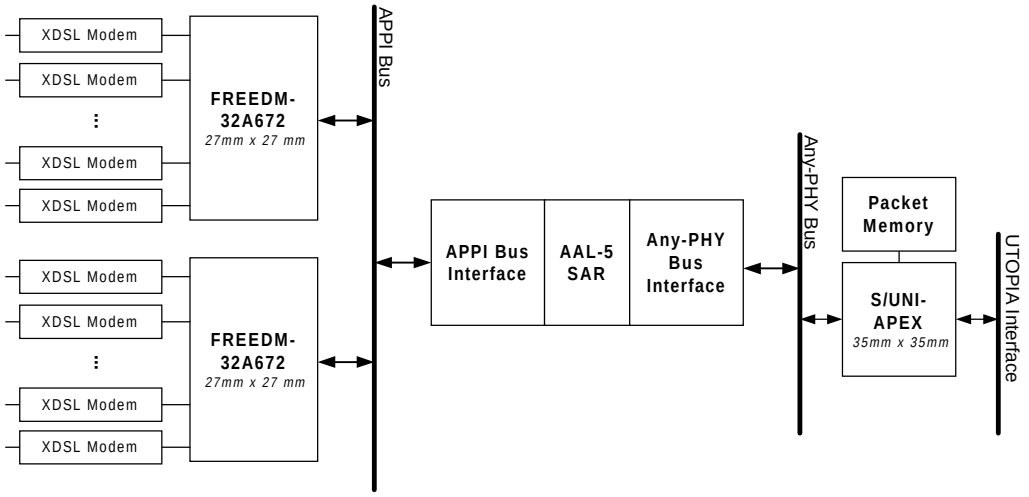
2.1.2.2 Multiservice Access Multiplexer

A multiservice access multiplexer requires a port card that can terminate 24 xDSL lines carry PPP-encapsulated IP traffic. Each xDSL line can support a maximum of 1.5 Mbps of downstream traffic and 640 Kbps of upstream traffic. The choice of the system bus is left unspecified, but a "packet aware" traffic shaper and queue manager is also required to complete this design.

Item	Value	Note
System Bus Option	Unspecified	Needs to work with a traffic shaper and queue manager.
Number of physical links.	24 xDSL	Each xDSL supports 1.5 Mbps of downstream traffic and 1 Mbps of upstream traffic.
Number of HDLC channels	24	XDSL is an unchannelized link.
Aggregate Bandwidth	Downstream: 36 Mbps Upstream: 16 Mbps	Downstream traffic: 24 links at 1.5 Mbps each = 36 Mbps. Upstream traffic: 24 links at 640 Kbps each ≅16 Mbps

Base on the above selection criteria, several FREEDM devices can be used in this application including FREEDM-32, FREEDM-32A672 and FREEDM-32P672.

One possible implementation of this multiservice access switch is to use a FREEDM-32A672 with S/UNI-APEX, which supports 2,048 line ports, 4 WAN ports, and a high-speed microprocessor port. It supports any port to any port switching for 64K independent connections. S/UNI-APEX implements a traffic queuing algorithm that is highly configurable on a per-connection, per-class and per-port basis. It can also support scheduling of four classes of service on every port.



The interface device between the FREEDM-32A672 and the S/UNI-APEX need to perform the following basic functions:

1. Allow S/UNI-APEX indirect access to FREEDM-32A672's transmit partial packet FIFO fill level on a per HDLC channel basis. This allows S/UNI-APEX to schedule packets to those channels that are ready to accept packet fragments for transmission. S/UNI-APEX can support 4 levels of QoS and can schedule a higher priority packet ahead of a lower priority packet. The S/UNI-APEX sends packet to FREEDM as ATM cells across the Any-PHY Cell Interface. The bridge device must receive the ATM cells, perform AAL5 reassembly function and forward the packet fragment to FREEDM-32A672 via the APPI interface for transmission.

2. Polls the FREEDM-32A672 to determine which device has incoming packet, receive the packet through the APPI interface, perform AAL-5 segmentation function and forward the ATM cells to the S/UNI-APEX via the Any-PHY Cell Interface. If the packet is received in error, the bridge device must set the length field of the AAL-5 trailer to zero. This will inform the S/UNI-APEX to drop the packet.

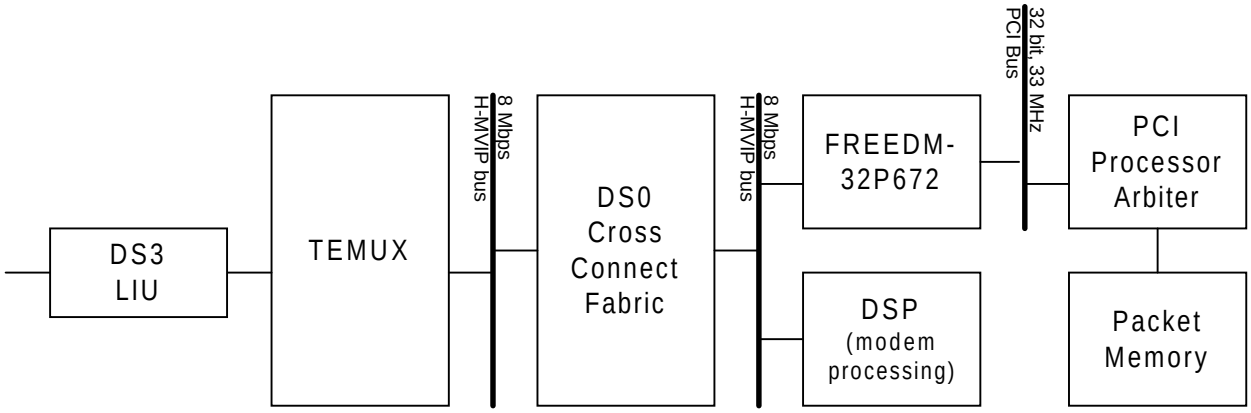
2.1.2.3 Remote Access Concentrator

A remote access concentrator needs to support a channelized DS3 carrying 28 channelized T1 or ISDN Primary Rate Interfaces (PRI). A circuit switch is used to detect whether an incoming call is from an analog or an ISDN device and direct it to the appropriate processing module. As each bearer channel can carry an independent user session, the PPP processing module needs to support up to 672 HDLC channels.

The interface from the circuit switch to the framer and to the layer 2 processing module is 8 Mbps H-MVIP. The preferred system interface is a 32 bit, 33 MHz PCI bus.

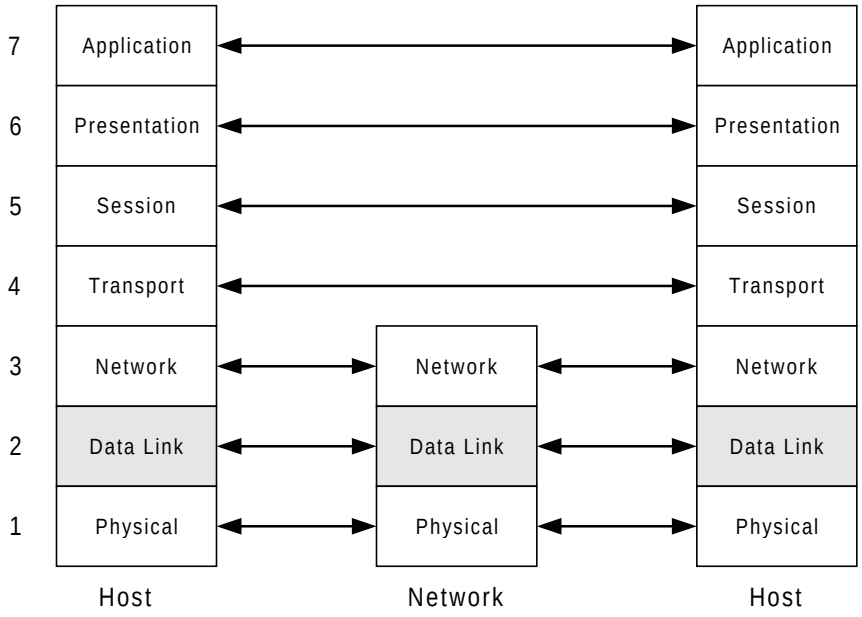
Item	Value	Note
System Bus Option	PCI	32 bit, 33 MHz
Number of physical links.	28 channelized T1	The 28 T1s are connected to the DS0 cross-connect fabric via four 8 Mb/s H-MVIP bus segments with each segment carrying 4 T1/PRIs.
Number of HDLC channels	672	There are 24 DS0 timeslots per T1 and 28 T1s per channelized DS3. Therefore there are 24*28=672 timeslots.
Aggregate Bandwidth	43 Mbps full duplex.	

The FREEDM-32P672 meets all the selection criteria and can be used in this port card design with TEMUX. Both devices support 8 Mbps H-MVIP bus interface and hence interface directly with the DS0 cross connect fabric. On the system side, the FREEDM-32P672 supports a 32 bit, 33/66 MHz PCI bus.



3 OVERVIEW

The Open Systems Interconnect (OSI) reference model, defined by the International Standards Organization (ISO), divides protocol suites into a structure consisting of seven layers. Each layer defines a set of functions common to networking environments transferring data from one place to another. A protocol at a given layer communicates with its equivalent on a remote system. Each layer passes its own data structures for use by its peer. It doesn't interpret any of the data for the layers above and below. On a given computer, data passes from users to their application software. Data then passes down the stack, layer by layer, until the physical layer sends it into the network. At the receiving end, this data passes up the stack to the receiving application. In other words, a layer in the OSI model provides service to the layer immediately above and relies on the layers below for transferring its data. The modularity enables network designers to select different protocols for each layer to accommodate varying networking situations.

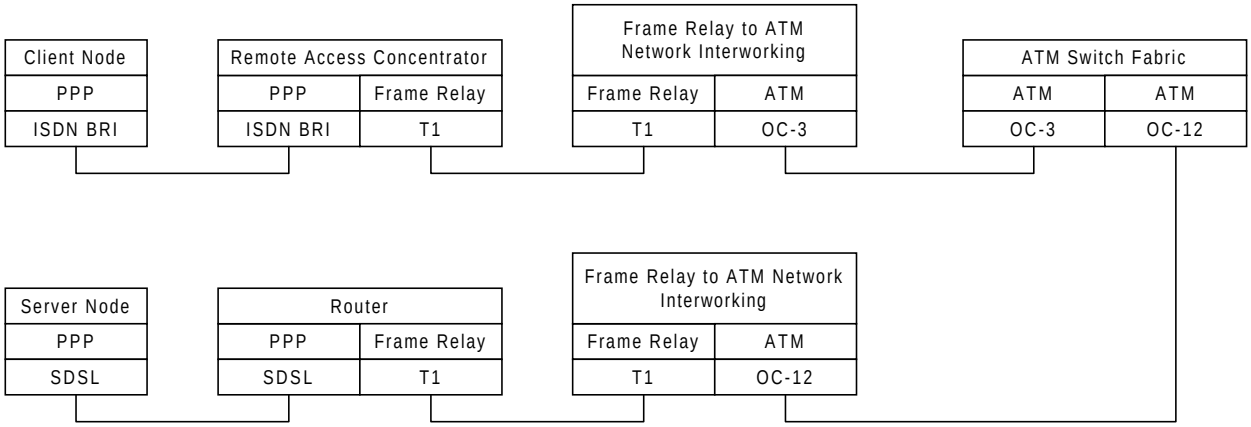


Many protocol choices are frequently available for each layer, and some overlap in functionality with several layers. On data link layer, the High Level Data Link Control (HDLC) specification is one of the most popular protocol used to encapsulate upper layer protocols, such as TCP/IP, for transmission over the wide area network.

The HDLC protocol is responsible for the error free movement of data between network nodes. That is, it enables the upper OSI layers to send and receive data error free, without loss and in the correct order. HDLC is a bit-oriented synchronous protocol that provides complete data transparency in a full-duplex point-to-point operation. It is independent of transmission bit rate and it requires a full duplex, bit transparent,

synchronous channel. HDLC is a very efficient protocol. Minimum overhead is required to ensure flow control, error detection and recovery. If data is flowing in both directions, the data frames themselves carry all the information required to ensure data integrity.

The journey taken by a user packet across the wide area network, from a client node to a server node, may be encapsulated several times using the HDLC protocol. There are many permutations for a packet to traverse the network. One possible permutation is described below as an example:



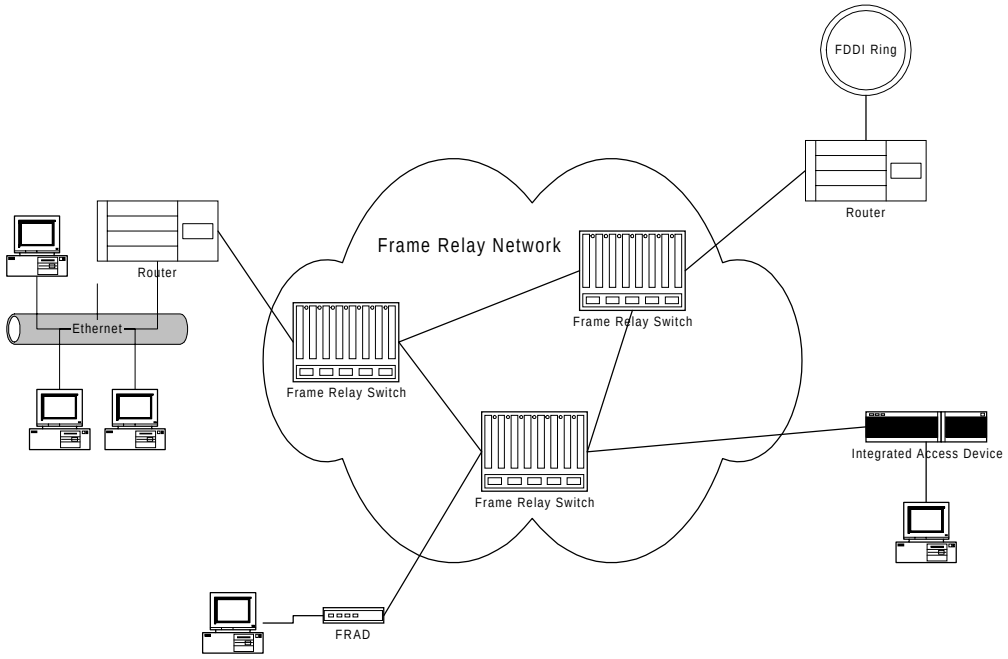
- At the client node, a user packet is encapsulated using the PPP frame structure, which is based on the HDLC protocol.
- The PPP frame is carried over an ISDN BRI channel to a remote access concentrator where PPP frame is terminated. The remote access concentrator extracts the user data from PPP frame and encapsulates it using an industry agreed scheme such as FRF.3.1 Multiprotocol Encapsulation Implementation Agreement. The frame relay frame is based on the HDLC protocol.
- The frame relay data is transmitted, via an unchannelized T1 link, to a multi-service switch that supports frame relay service. At the multiservice switch, the frame relay packet is converted to ATM cells using Frame Relay Forum's Frame Relay/ATM Network Interworking Implementation Agreement (FRF.5). The ATM cells are transmitted over an OC-3 link to an ATM core switch.
- At the ATM core switch, the ATM cells are switched to an OC-12 link destined for a downstream multi-service switch.
- At the multi-service switch, the ATM cells are reassembled back into a frame relay packet using FRF.5. The frame relay packet is forwarded to a router on a T1 link.
- The router terminates the frame relay packet and encapsulates the user data using PPP frame. The frame is transmitted to the server node using SDSL service.
- The server node extracts the user data from the PPP frame.

The following sections describe how different network equipment can use HDLC protocol to provide efficient and reliable data link layer solutions.

Frame Relay Switch

A frame relay network provides an end-user with a high-speed virtual private network capable of supporting applications with large bit-rate transmission requirements. It gives a user N*DS0, T1, E1 or higher bandwidth access rates at a lesser cost than that which can be obtained by leasing comparable physical links.

Frame Relay provides for the encapsulation of information from terminal devices connected to the network through routers, Integrated Access Devices and Frame Relay Access Devices (FRADs).



The frame relay frame is based on HDLC protocol as shown below. The general operation of a frame relay system is described below:

Flag	FCS (CRC)	Payload (I field)	Control and Address	Flag

1. A frame relay system must provide services to delimit and align frames on the channel, so flags are used at a receiver to identify the beginning and ending of a frame. Flags take the form of specific sequence of 1 and 0 bits (i.e. 01111110) to connote the start and end of a transmission. Bit stuffing is performed on any similar bit sequence between the flags to eliminate confusion. Bit are stuffed in the control, payload and FCS fields to prevent any of the bits in these fields from being interpreted incorrectly as a flag, which would render the traffic unintelligible. These extra bits must be removed at the receiver via an operation known as unstuffing.

2. The system must inspect the frame to make certain it aligns itself on integer number of octets prior to the zero bit insertion and following the unstuffing of the zero bits.

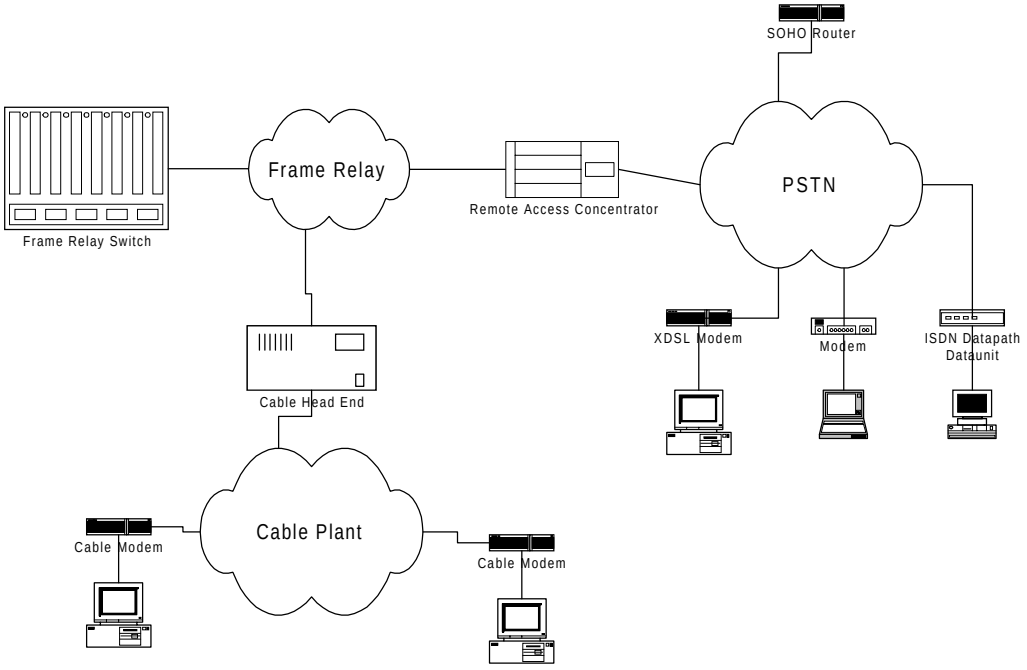
3. The system must inspect the frame to insure that it does not exceed the maximum and minimum frame sizes often referred to as the maximum data unit (MDU).

4. The system must be able to detect transmission errors through the use of the frame check sequence (FCS) field, formatting problems and other operational errors.

The HDLC controller needs to provide the above service on a per HDLC channel basis. To address higher density port cards, a single HDLC controller may be required to simultaneously support up to 672 HDLC sessions from a channelized DS3 link. In addition the frame relay system must support virtual circuit multiplexing and demultiplexing through the use of the DLCI field in the frame header. The payload fields of the frames on the channel may contain traffic from multiple users; each payload field is identified with a unique DLCI. The HDLC controller must efficiently forward the control and payload fields to a processing module where the header processing tasks can be performed.

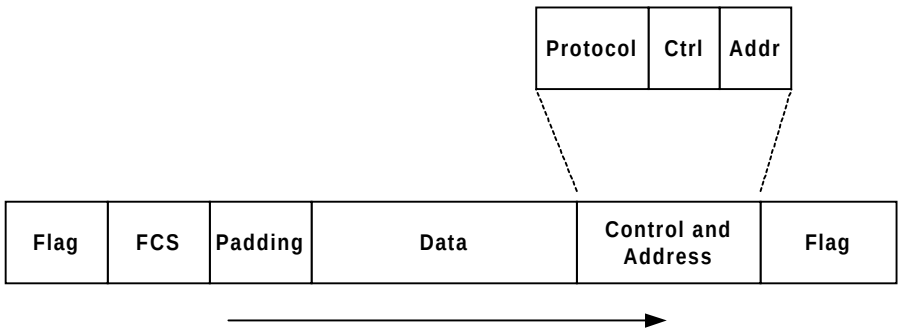
Dial Access Platform

A remote access concentrator provides dial access for remote users over services such as modem, ISDN BRI/PRI, cable modem and xDSL.



PPP was developed by Internet Engineering Task Force (IETF) to address the need for a standard method for encapsulating and sending datagrams over point-to-point serial connections.

The PPP frame structure is similar to the frames defined by the HDLC standards. The PPP frame consists of a header and a data block. All information in a frame is composed of multiple 8-bit octets. The default lengths for both the Protocol and the Frame Check Sequence (FCS) field are 16 bits.



4 GLOSSARY

APPI	Any-PHY Packet Interface: A 16 bit, 50 MHz master/slave bus that allows packet fragments to be sent to and from FREEDM 2nd generation devices.
CRC	Cyclic Redundancy Check: A check performed on data to see if an error has occurred in the transmitting, reading or writing of the data. The Frame Relay's FCS field uses a sixteen bit CRC check sum.
DLCI	Data Link Connection Identifier: A Frame Relay term defining a 10-bit field of the Address Field. The DLCI identifies the data link and its service parameters, including frame size, committed information rate, committed burst size, burst excess size and committed rate measurement interval.
DS0	Digital Service, level 0: There are 24 DS0 channels in a DS1. Each DS0 channel has a bandwidth of 64 Kbps full duplex.
E1	E1 carries information at the rate of 2 Mbps. This is the rate used by European CEPT carriers to transmit 30, 64 Kbps digital channels for voice or data calls, plus a 64 Kbps channel for signaling and a 64 Kbps channel for framing.
FCS	Frame Check Sequence: Bits added to the end of a frame for error detection. In bit-oriented protocols, a frame check sequence is a 16-bit field added to the end of a frame that contains transmission error-checking information.
FRAD	Frame Relay Access Device. A device allows a LAN or computer to interface to a frame relay network. A FRAD may be stand-alone device, although the function generally is embedded in a router.
Frame Relay	Equipment and services pertaining to the switching of variable length packets.
FRF.3.1	Frame Relay Forum's Multiprotocol Encapsulation Implementation Agreement.
FRF.5	Frame Relay Forum's Frame Relay/ATM Network Interworking Implementation Agreement.
HDLC	High Level Data Link Control: A communications protocol that is bit oriented and is used at the data link layer to encapsulate upper

	layer protocols such as TCP/IP for transmission over a wide area network.
H-MVIP	High Speed Multi-Vendor Integration Protocol: A synchronous time division multiplexed bus of Nx64 Kbps constant bit rate data stream. The H-MVIP standards are defined by the GO-MVIP organization.
HSSI	High Speed Serial Interface: High Speed Serial Interface: A serial data communication interface optimized for high speeds up to 52 Mbps.
ISDN	Integrated Services Digital Network: ISDN has several options and two of which are described below: • Basic Rate ISDN (2B+D), which has 144 Kbit/s of data/bearer channel and 16 Kbit/s of signaling channel. • Primary Rate ISDN (PRI) which support 1.544 Mbps in North America and 2 Mbps in Europe.
ISO	International Standards Organization: An international standards-setting organization.
MAN	Metropolitan Area Network: A term used to describe a data network covering an area larger than a local area network, but less than a wide area network. A MAN may carry voice, video and multimedia data.
OC-12	Optical Carrier 12. SONET channel of 622.08 Mbps.
OC-3	Optical Carrier 3. A SONET channel that has a bandwidth of 155.52 Mbps
OSI	Open Systems Interconnect: A standard that defines seven independent layers of communication protocols. Each layer enhances the communication services of the layer just below it and shields the layer above it from the implementation details of the lower layer.
PCI	Peripheral Component Interconnect (PCI) an open standard bus architecture that defines the specifications needed to interconnect devices over a high-speed parallel bus.
PPP	Point-to-Point Protocol: The most popular way to carry IP frames over a leased line or switched circuit. A protocol that allows a

	computer to connect to the Internet. PPP features error detection, data compression and link layer negotiation protocol.
SBI	Scaleable Bandwidth Interconnect: A synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links.
SDH	Synchronous Digital Hierarchy: A set of standard fiber-optic transmission standards used outside North America.
SDSL	Symmetrical Digital Subscriber Line. An access technology that support up to 1 Mbps full duplex.
SONET	Synchronous Optical NETwork: A family of fiber optic transmission standards used in North America.
T1	Trunk Level 1: A digital transmission link with a total signaling speed of 1.544 Mbps.
TCP/IP	Transmission Control Protocol/Internet Protocol: A networking protocol that provides communication across interconnected networks, between computers with diverse hardware architecture and various operating systems.
UTOPIA	Universal Test and Operations Interface: Refers to an electrical interface between the TC and PMD sublayers of the physical layer. UTOPIA is the interface for devices connecting to an ATM network.
VT	Virtual Tributary: A structure designed for transport and switching of sub-DS3 payloads. A unit of sub-SONET bandwidth that can be combined or concatenated, for transmission through the network. VT1.5 is equivalent to 1.544 Mbps and VT2 equals 2.048 Mbps
WAN	Wide Area Network: A data network that is used to interconnect remote LANs or users over leased lines, packet or cell switch services

NOTES

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