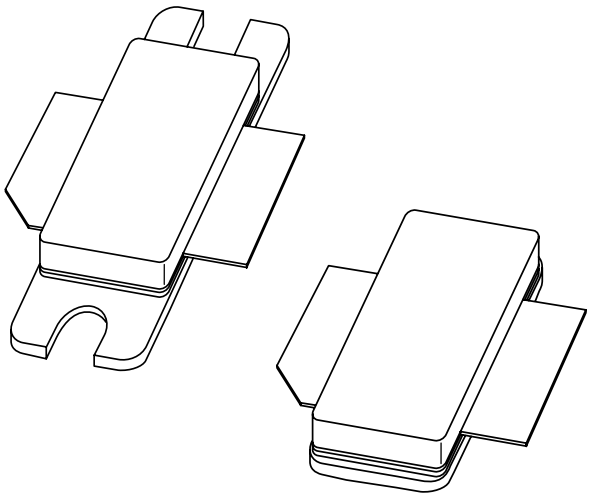
DATA SHEET



BLF0810-180; BLF0810S-180
Base station LDMOS transistors

Preliminary specification

2002 Aug 02

Philips
Semiconductors

PHILIPS

Base station LDMOS transistors BLF0810-180; BLF0810S-180

FEATURES

- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1 GHz)
- Internally matched for ease of use.

APPLICATIONS

- Common source class-AB operation applicable in the 860 to 960 MHz frequency range
- CDMA and multi carrier applications.

DESCRIPTION

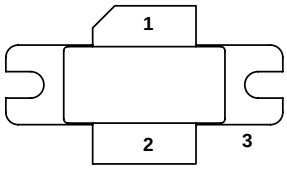
180 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

Typical CDMA IS95 performance at standard settings at a supply voltage of 28 V and I_{DQ} = 1125 mA, channel bandwidth is 30 kHz, adjacent channels at ± 750 kHz and at ± 1.98 MHz:

Output power = 35 W
Gain = 15.6 dB
Efficiency = 26 %
ACPR <–45 dBc at 750 kHz and BW = 30 kHz
ACPR <–63 dBc at 1.98 MHz and BW = 30 kHz

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange

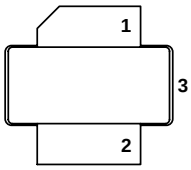


Top view MBK394

Fig.1 Simplified outline SOT502A (BLF0810-180)

PINNING - SOT502B

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



Top view MBL105

Fig.2 Simplified outline SOT502B (BLF0810S-180)

QUICK REFERENCE DATA

Typical RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dBc)	ACPR (dB)
Class-AB (2-tone)	f_1 = 890.0 f_2 = 890.1	28	140 (PEP)	15.2	35	–30	–
CDMA(1)	881.5	28	32	15.6	26	–	<–45 (2) <–63 (3)
CDMA multi carrier signal(4)	881.5	28	14	15.6	16	–	<–52 (2) <–56 (3)

Note

1. IS95 CDMA (Pilot, Paging, Sync, and Trafic Codes 8 trough 13)
2. ACPR 750 kHz at BW = 30 kHz
3. ACPR 1.98 MHz at BW = 30 kHz
4. 3 adjacent carriers with 32 channels walsh codes each.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	T_h = 25 °C, P_L = 35 W avg, note 1	<0.42	K/W
$R_{th\ hs\text{-}j}$	thermal resistance from heatsink to junction	T_h = 25 °C, P_L = 32 W avg, note 2	<0.62	K/W

Note

1. Thermal resistance is determined under RF operating conditions.
2. Depends of installation.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 36 V	–	–	1	μA
I_{DSX}	on-state drain current	V_{GS} = $V_{GS(th)}$ + 9 V; V_{DS} = 10 V	45	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	–	9	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	–	60	–	mΩ

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C;.

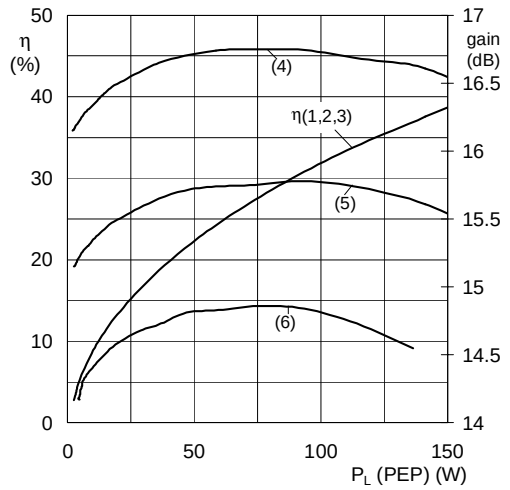
MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	I_{DQ} (mA)	G_p (dB)	η_D (%)	d_3 (dBc)	ACPR (dB)
Class-AB (2-tone)	f_1 = 890.0 f_2 = 890.1	28	140 (PEP)	1125	15.2	35	–30	–
CDMA(1)	881.5	28	32	1250	15.6	26	–	<–45 (2) <–63 (3)
CDMA multi carrier signal(4)	881.5	28	14	1250	15.6	16	–	<–52 (2) <–56 (3)

Note

1. IS95 CDMA (Pilot, Paging, Sync, and Trafic Codes 8 trough 13)
2. ACPR 750 kHz at BW = 30 kHz
3. ACPR 1.98 MHz at BW = 30 kHz
4. 3 adjacent carriers with 32 channels walsh codes each.

Ruggedness in class-AB operation

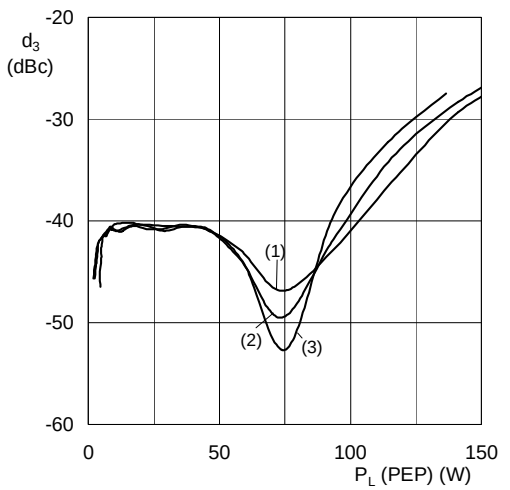
The BLF0810-180 and BLF0810S-180 are capable of withstanding a load mismatch corresponding to VSWR = 15 : 1 through all phases at V_{DS} = 27 V; P_L = 126 W (PEP).



V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

Efficiency at $T_{heatsink}$: (1) = –40 °C (2) = 20 °C (3) = 80 °C
Gain at $T_{heatsink}$: (4) = –40 °C (5) = 20 °C (6) = 80 °C

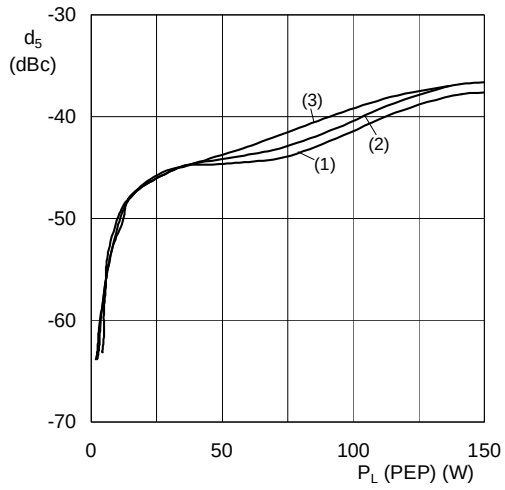
Fig.3 Two tone power gain and efficiency as functions of the load power at different temperatures.



V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 890.0 MHz; f_2 = 890.1 MHz

$T_{heatsink}$: (1) = –40 °C (2) = 20 °C (3) = 80 °C

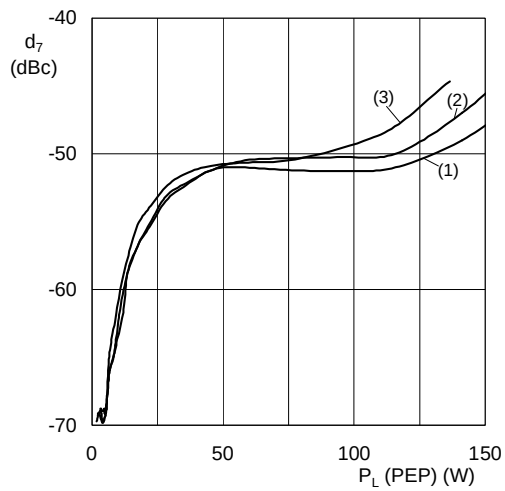
Fig.4 Third order intermodulation distortion as a function of the load power at different temperatures.



V_{DS} = 27 V;I_{DQ} = 1.1 A; f_1 = 890.0 MHz; f_2 = 890.1 MHz

$T_{heatsink}$: (1) = –40 °C (2) = 20 °C (3) = 80 °C

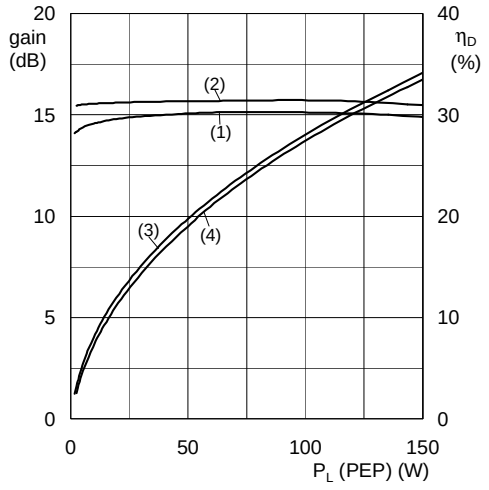
Fig.5 Fifth order intermodulation distortion as a function of the load power at different temperatures.



V_{DS} = 27 V;I_{DQ} = 1.1 A; f_1 = 890.0 MHz; f_2 = 890.1 MHz

$T_{heatsink}$: (1) = –40 °C (2) = 20 °C (3) = 80 °C

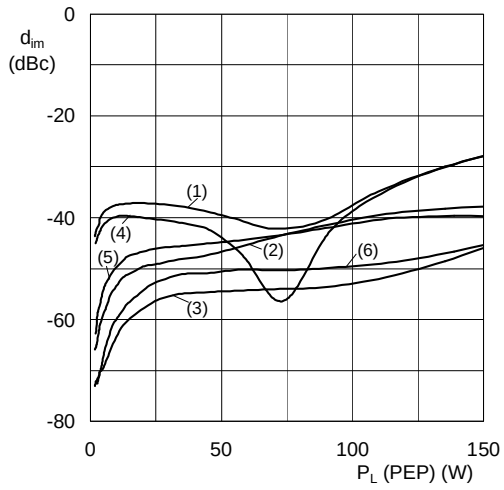
Fig.6 Seventh order intermodulation distortion as a function of the load power at different temperatures.



V_{DS} = 27 V; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

Gain: (1) : I_{DQ} = 1.0 A; (2) : I_{DQ} = 1.45 A
Efficiency: (3) : I_{DQ} = 1.0 A; (4) : I_{DQ} = 1.45 A

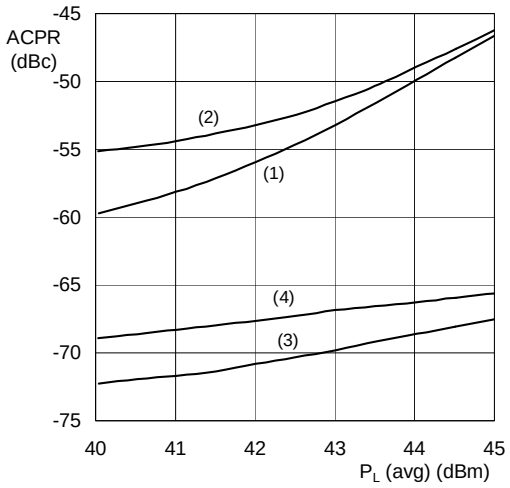
Fig.7 Two tone power gain and efficiency as functions of the load power and I_{DQ}.



V_{DS} = 27 V; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

I_{DQ} = 1.0 A: (1) = d_3 (2) = d_5 (3) = d_7;
I_{DQ} = 1.3 A: (4) = d_3 (5) = d_5 (6) = d_7;

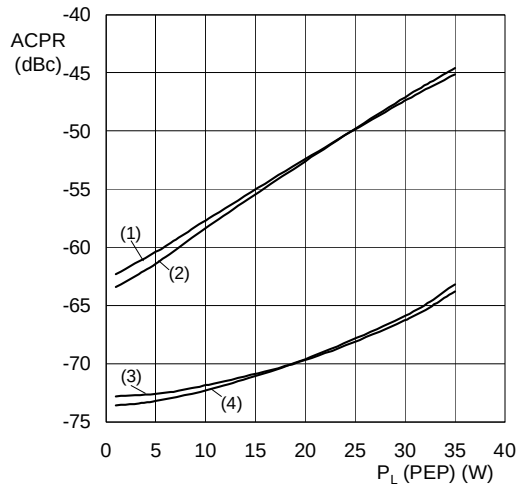
Fig.8 Intermodulation distortion as a function of the load power



V_{DS} = 27 V; f = 894 MHz;

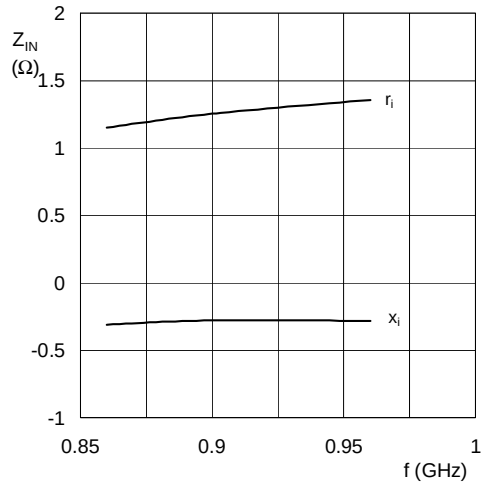
ACPR @750 kHz:
(1): I_{DQ} = 1.1 A (2):I_{DQ} = 1.4 A;
ACPR @1.98 MHz:
(3):I_{DQ} = 1.1 A (4):I_{DQ} = 1.4 A

Fig.9 CDMA IS95 ACPR distortion as a function of the average load power and I_{DQ}.



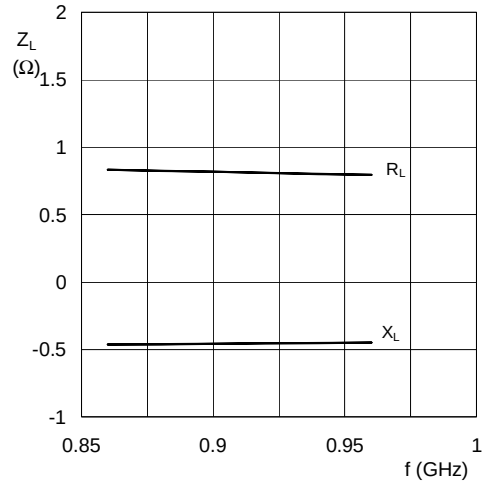
V_{DS} = 27 V; f = 890 MHz; I_{DQ} = 1.1 A;
ACPR @750 kHz:
(1): $T_{heatsink}$ = 20 °C (2): $T_{heatsink}$ = 80 °C;
ACPR @1.98 MHz:
(3): $T_{heatsink}$ = 20 °C (4): $T_{heatsink}$ = 80 °C.

Fig.10 CDMA IS95 ACPR distortion as a function of the load power at different temperatures.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 1125 mA; P_L = 35 W.

Fig.11 Input impedance as a function of frequency (series components):typical values; values compromised for different parameters



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 1125 mA; P_L = 35 W.

Fig.12 Load impedance as a function of frequency (series components); typical values; values compromised for different parameters.

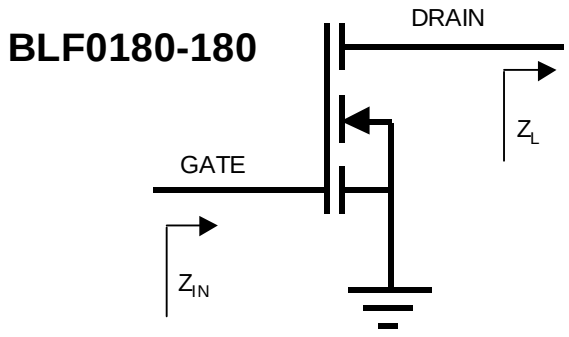


Fig.13 Definition of transistor impedance.

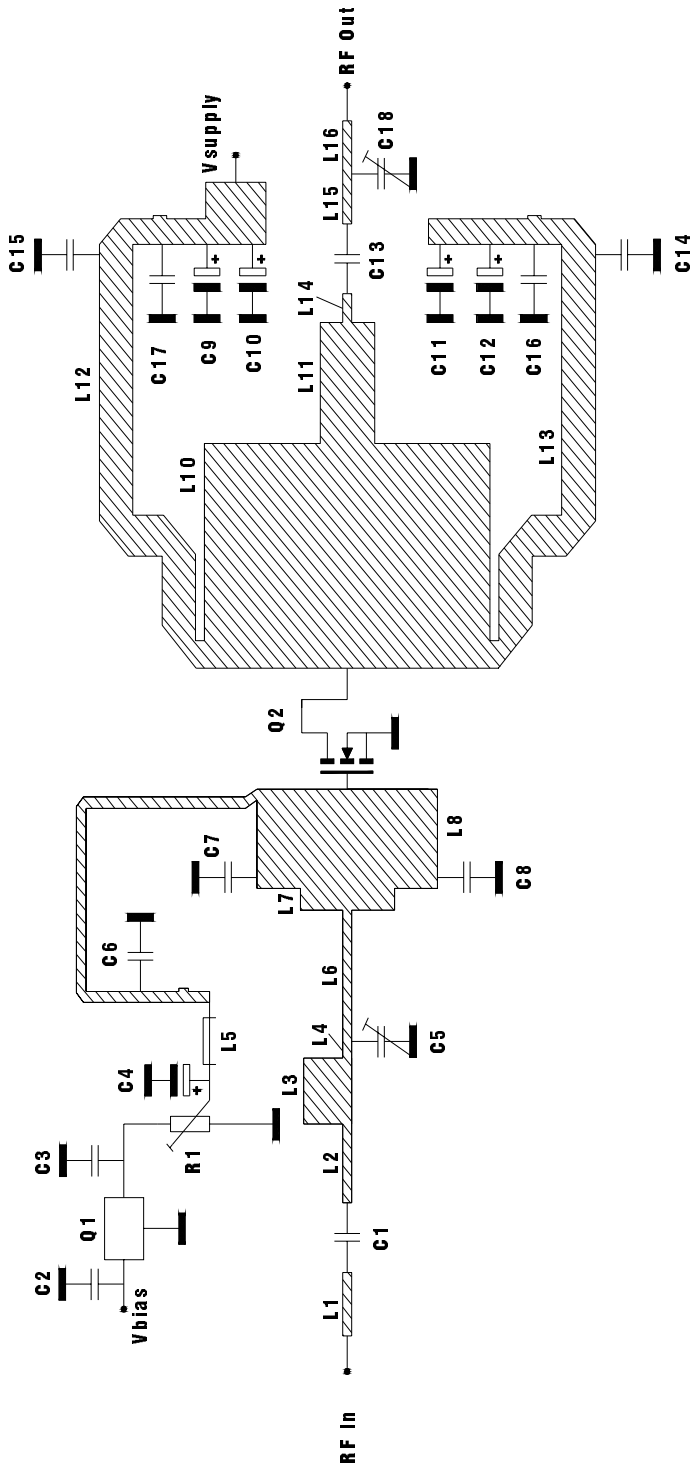
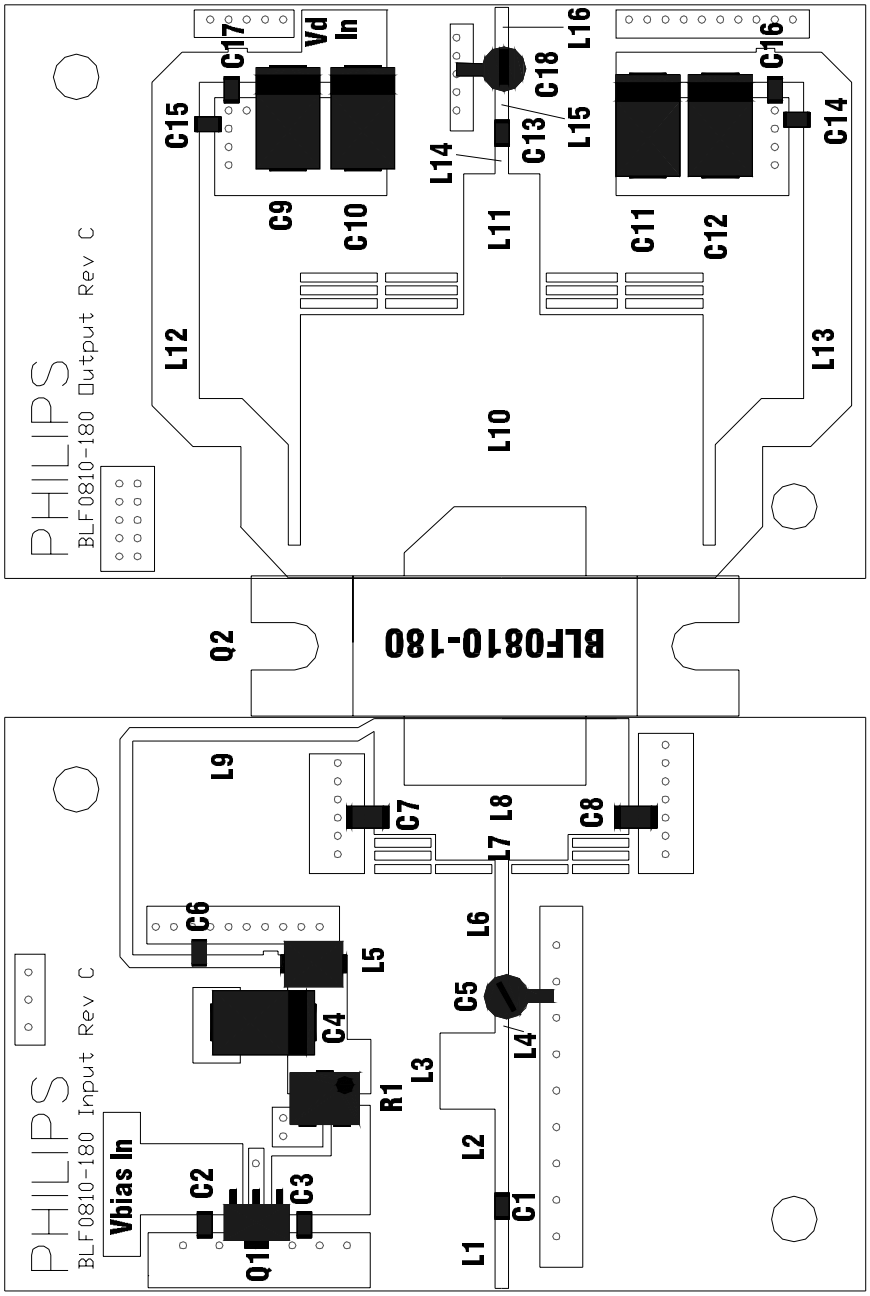


Fig.14 Circuit for 860 to 900 MHz test circuit.



Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 25 mils.

The other side is unetched and serves as a ground plane.

Fig.15 Circuit for 860 to 900 MHz test circuit.

List of components

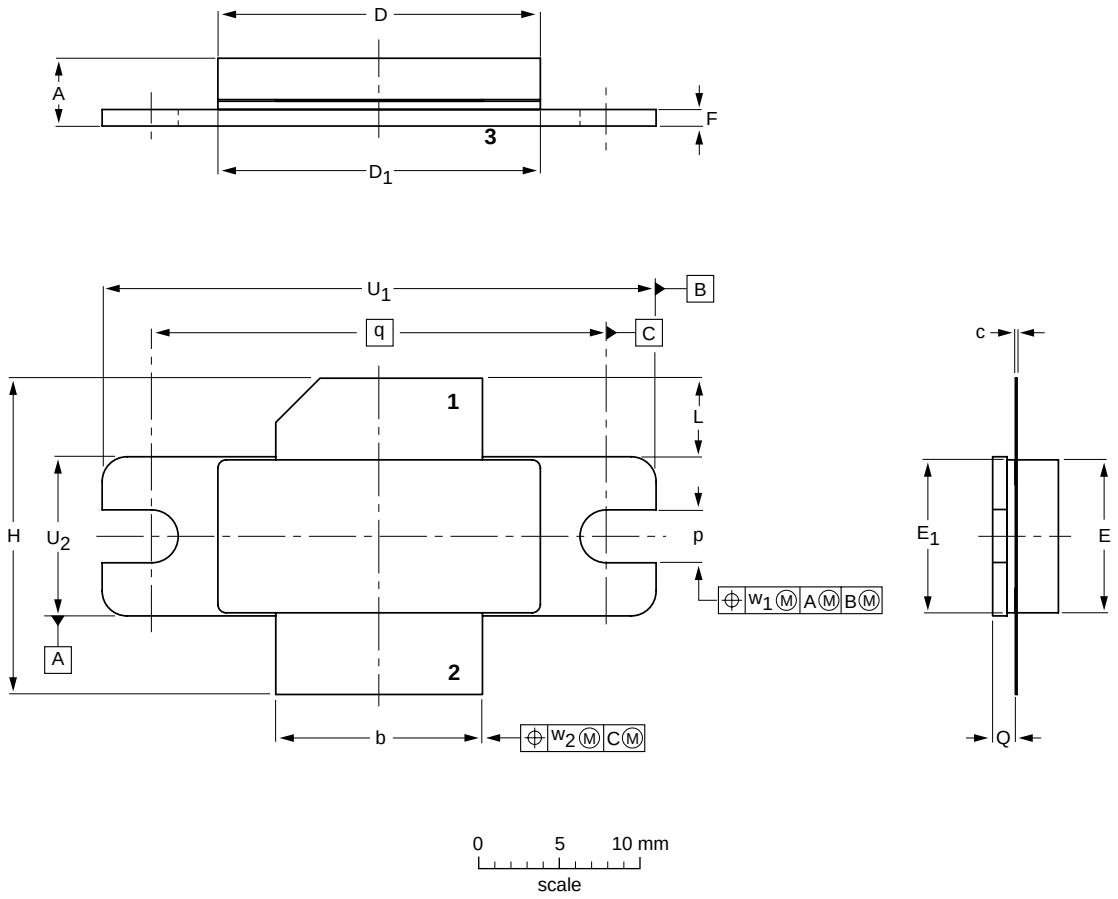
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μF	
C5, C18	air trimmer capacitor	5 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 kΩ	
Q1	7808 voltage regulator		
Q2	BLF0910-140 LDMOS transistor		
L1	stripline; note 2		5.22 × 0.92 mm
L2	stripline; note 2		6.47 × 0.92 mm
L3	stripline; note 2		5.38 × 4.8 mm
L4	stripline; note 2		2.4 × 0.92 mm
L5	Ferroxcube		
L6	stripline; note 2		9.73 × 0.92 mm
L7	stripline; note 2		1.82 × 9.3 mm
L8	stripline; note 2		8.15 × 17.9 mm
L9	stripline; note 2		44 × 0.92 mm
L10	stripline; note 2		18.45 × 28.3 mm
L11	stripline; note 2		9.95 × 5.38 mm
L12, L13	stripline; note 2		37.6 × 3.35 mm
L14	stripline; note 2		2.36 × 0.92 mm
L15, L16	stripline; note 2		4.22 × 0.92 mm

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 0.64 mm

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

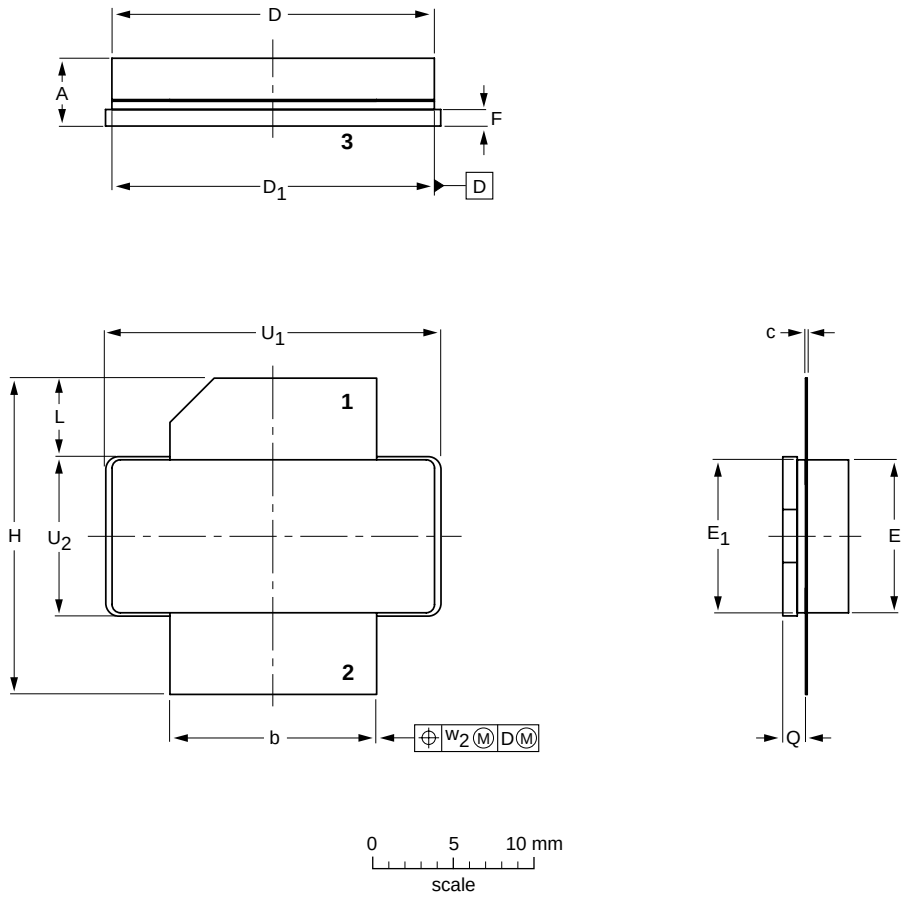
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						~~99-10-13~~ 99-12-28

PACKAGE OUTLINE

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502B						~~99-12-16~~ 99-12-28

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

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1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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Contact information

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