HMC461LP3

InGaP HBT 1 Watt High IP3 AMPLIFIER, 1.7 - 2.2 GHz

Typical Applications

A high linearity 1 watt amplifier for:

- Multi-Carrier Systems
- GSM, GPRS & EDGE
- CDMA & W-CDMA
- PHS
- Balanced or Push-Pull Configurable

Features

+45 dBm Output IP3 (Balanced Configuration)

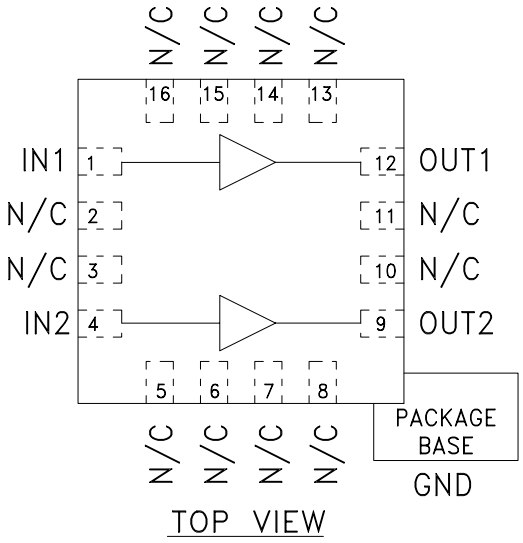
12 dB Gain

48% PAE @ +30.5 dBm Pout

+20 dBm W-CDMA Channel Power @ -45 dBc ACP

3 x 3 x 1 mm QFN SMT Package

Functional Diagram



General Description

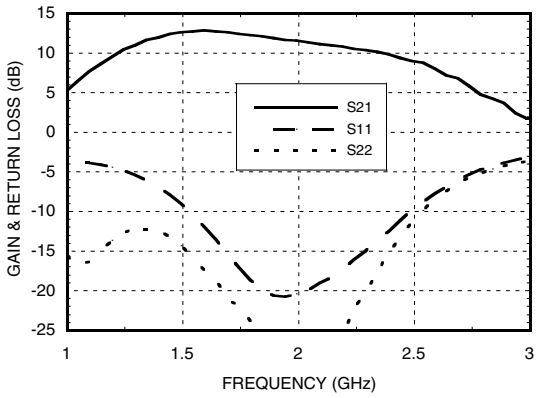
The HMC461LP3 is a 1.7 - 2.2 GHz high output IP3 GaAs InGaP Heterojunction Bipolar Transistor (HBT) dual-channel MMIC amplifier. The linear performance of two HMC455LP3 high IP3 drivers is offered in this single IC which can be configured in a balanced or push-pull amplifier circuit. The amplifier provides 12 dB of gain and +30.5 dBm of saturated power at 48% PAE from a single +5 Vdc supply while utilizing external baluns in a balanced configuration. The high output IP3 of +45 dBm coupled with the low VSWR of 1.2:1 makes the HMC461LP3 an ideal driver amplifier for PCS/3G wireless infrastructure. A low cost, leadless 3x3 mm QFN surface mount package (LP3) houses the dual MMIC amplifier IC. The LP3 provides an exposed base for excellent RF and thermal performance.

Electrical Specifications*, T_A = +25° C, Vs= +5V

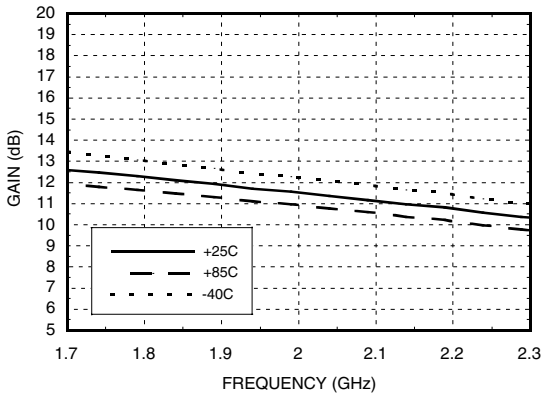
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		1.7 - 1.9			1.9 - 2.2		GHz
Gain	10	12.5		9	12		dB
Gain Variation Over Temperature		0.012	0.02		0.012	0.02	dB / °C
Input Return Loss		17			18		dB
Output Return Loss		20			25		dB
Output Power for 1dB Compression (P1dB)	26	29		26.5	29.5		dBm
Saturated Output Power (Psat)		29.5			30.5		dBm
Output Third Order Intercept (IP3)	41	44		42	45		dBm
Noise Figure		6.5			6		dB
Supply Current (Icq)		300			300		mA

** Specifications and data reflect HMC461LP3 measured with external baluns in a balanced amplifier configuration optimized for 1.85 - 2.2 GHz per application circuit herein. Contact HMC Applications for 1.7 - 1.85 GHz performance optimization.*

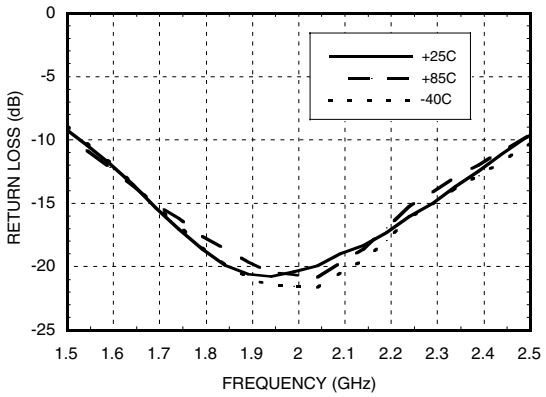
Broadband Gain & Return Loss



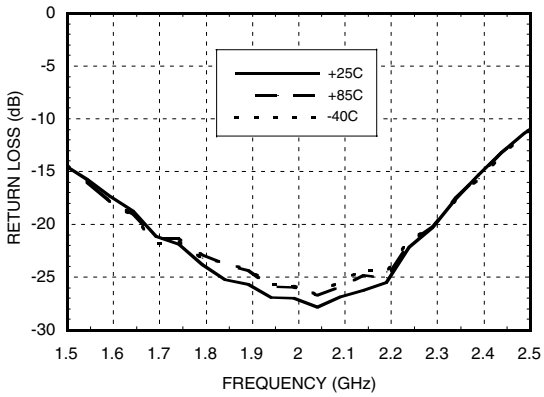
Gain vs. Temperature



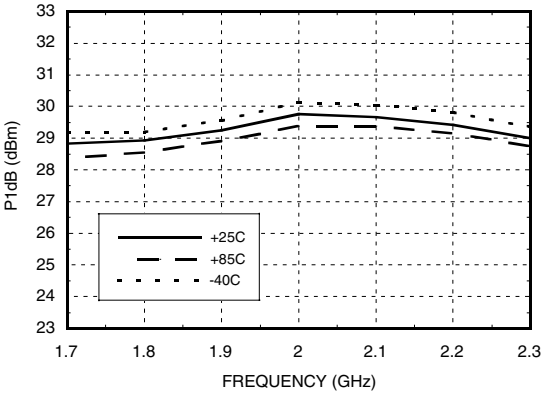
Input Return Loss vs. Temperature



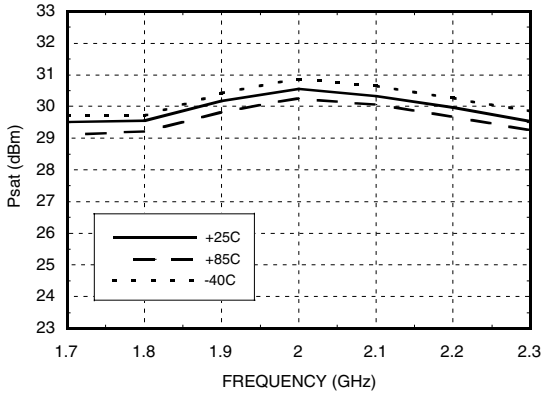
Output Return Loss vs. Temperature



P1dB vs. Temperature



Psat vs. Temperature



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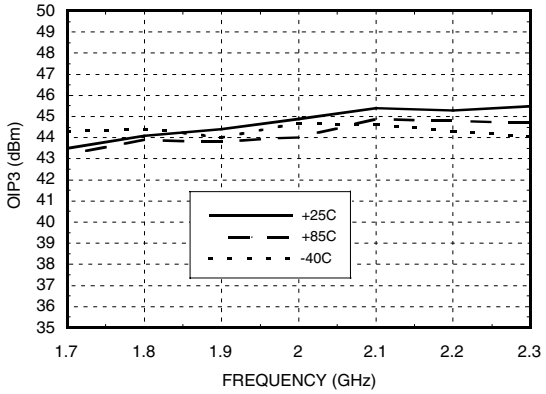
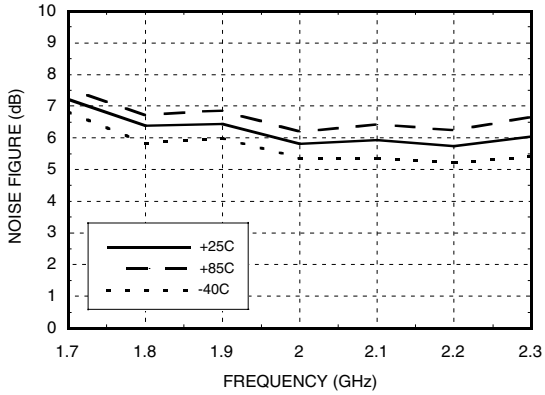
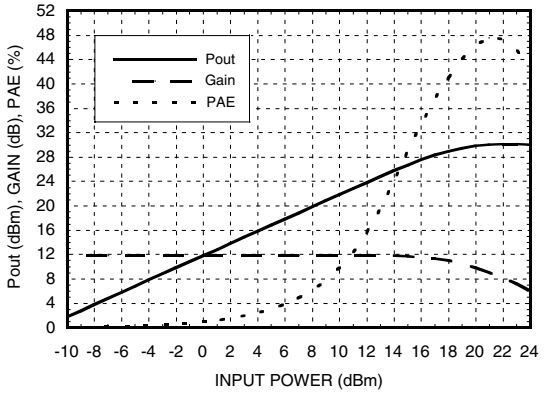
Output IP3 vs. Temperature



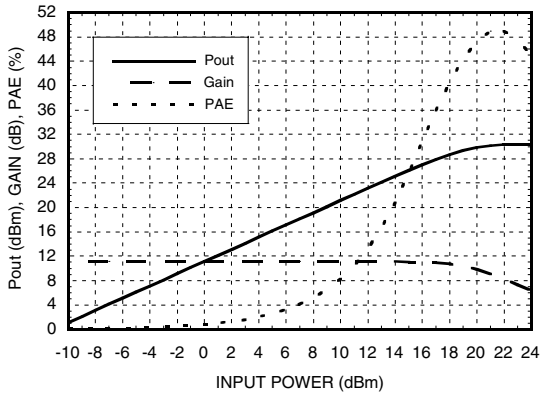
Noise Figure vs. Temperature



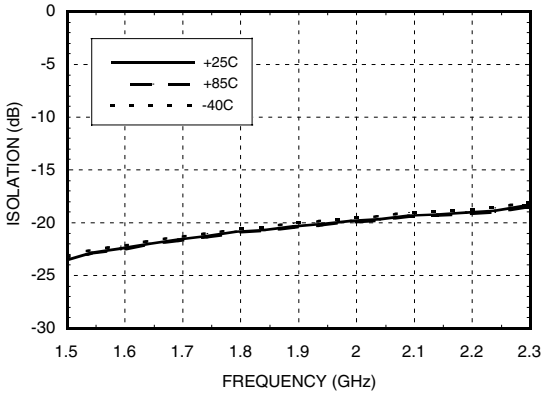
Power Compression @ 1.95 GHz



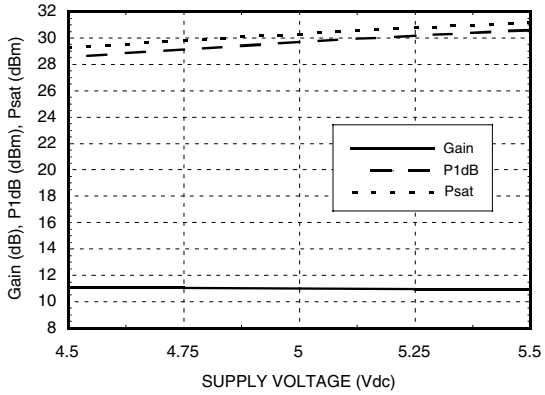
Power Compression @ 2.15 GHz



Reverse Isolation vs. Temperature

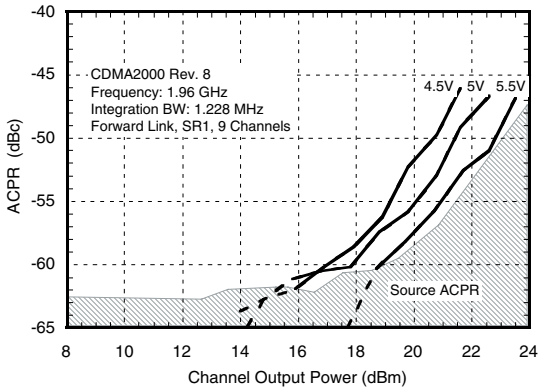


Gain & Power vs. Supply Voltage @ 2.15 GHz

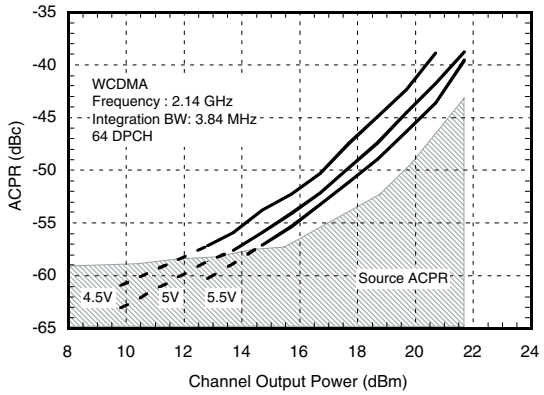


Specifications and data reflect HMC461LP3 measured with external baluns in a balanced amplifier configuration optimized for 1.85 - 2.2 GHz per application circuit herein. Contact HMC Applications for 1.7 - 1.85 GHz performance optimization.

ACPR vs. Supply Voltage @ 1.96 GHz CDMA2000, 9 Channels Forward

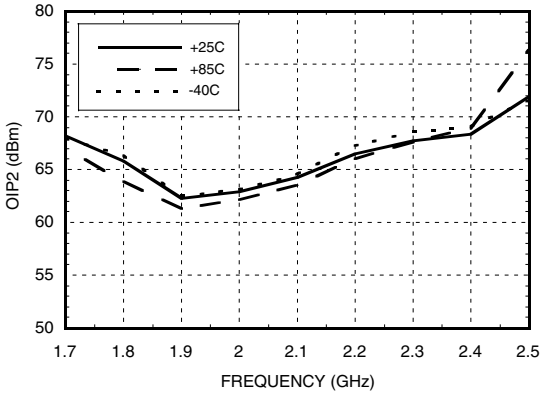


ACPR vs. Supply Voltage @ 2.14 GHz W-CDMA, 64 DCPH



** Source ACPR: All data is RSS corrected for source ACPR. Dashed lines are shown where corrected data is below source ACPR.*

Output IP2 vs. Temperature



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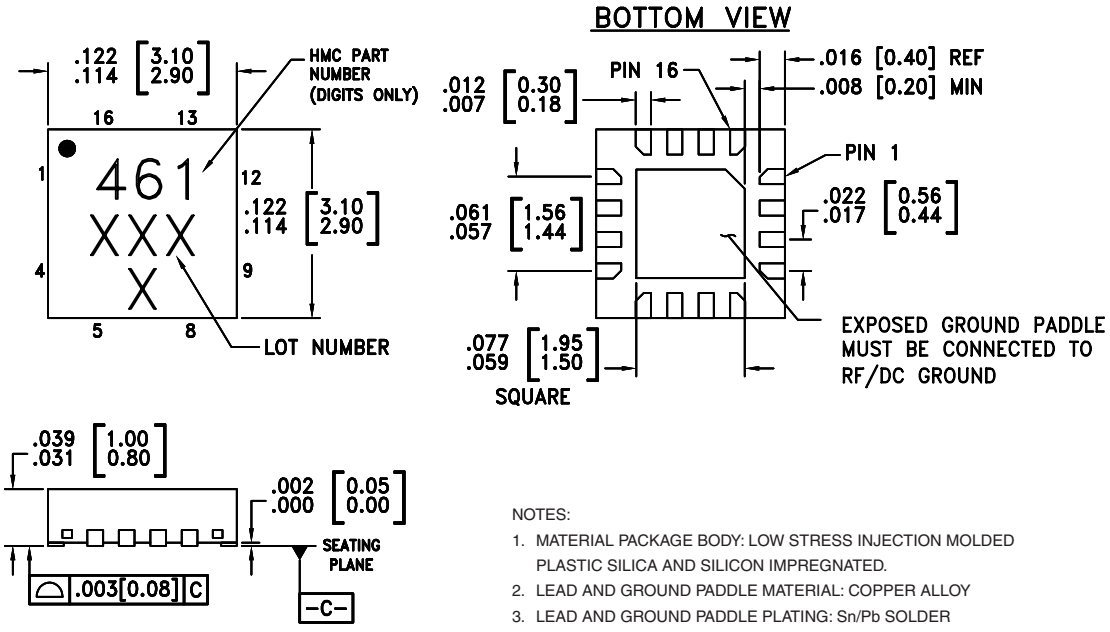
Absolute Maximum Ratings

Collector Bias Voltage (Vcc1, Vcc2)	+6.0 Vdc
RF Input Power (RFin)(Vs = +5.0 Vdc)	+30 dBm
Junction Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 32 mW/°C above 85 °C)	2.08 W
Thermal Resistance (junction to ground paddle)	31 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Outline Drawing



NOTES:

1. MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

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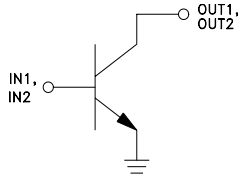
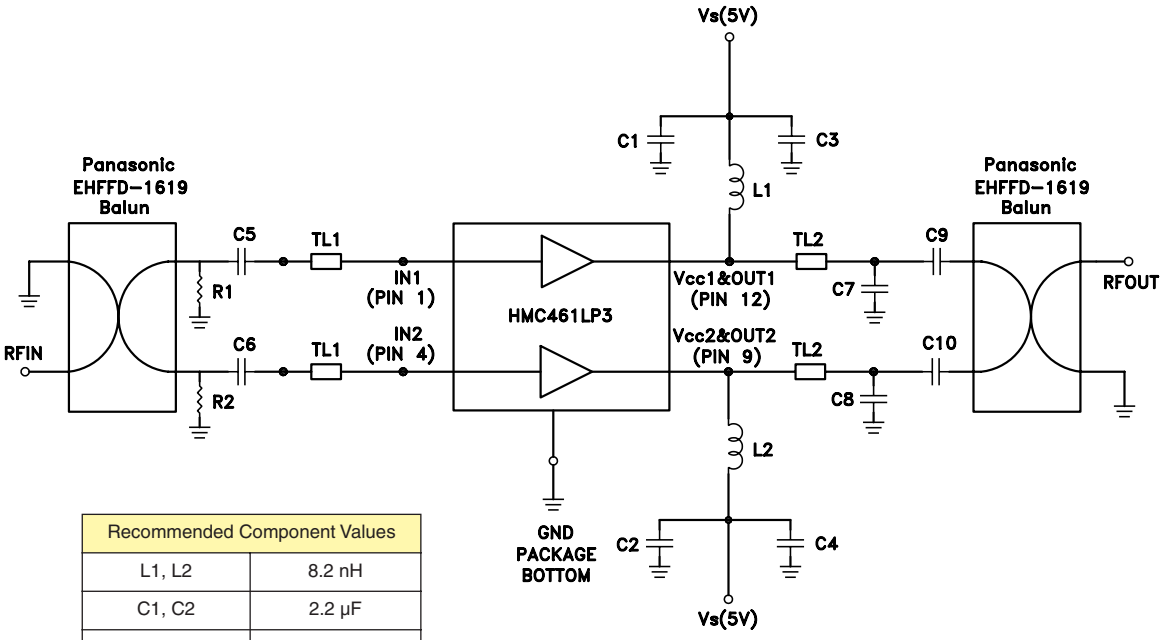
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
2, 3, 5 - 8, 10, 11, 13 - 16	N/C	This pin may be connected to RF ground.	
1, 4	IN1, IN2	RF Input. This pin is AC coupled. An off chip series matching capacitor is required.	
9, 12	OUT1, OUT2	RF output and DC Bias for the output stage.	
	GND	Package bottom must be connected to RF/DC ground.	

Recommended Application Circuit for Balanced Amplifier Configuration



Recommended Component Values	
L1, L2	8.2 nH
C1, C2	2.2 µF
C5, C6	5.0 pF
C7, C8	0.9 pF
C3, C4	100 pF
C7, C8	0.8 pF
C9, C10	4.0 pF
R1, R2	130 Ohm

	TL1	TL2
Impedance	50 Ohm	50 Ohm
Physical Length	0.09"	0.18"
Electrical Length	9.5°	19°
PCB Material: 10 mil Rogers 4350, Er = 3.48		

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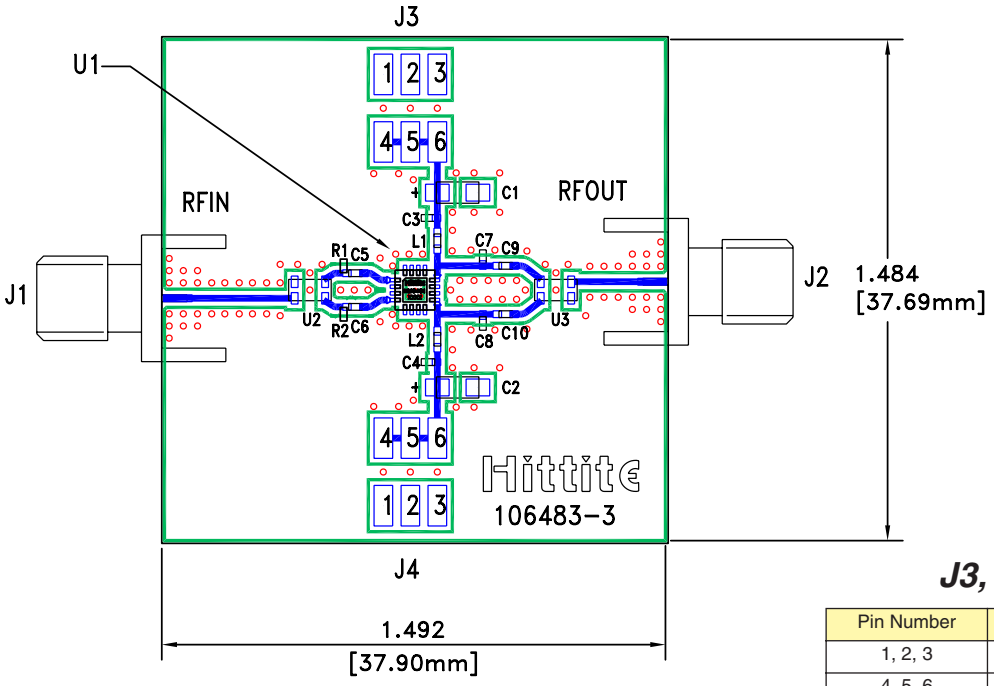
Evaluation PCB



J3, J4

Pin Number	Description
1, 2, 3	GND
4, 5, 6	Vs

List of Materials

Item	Description
J1, J2	PC Mount SMA Connector
J3, J4	2 mm DC Header
C1, C2	2.2 µF Capacitor, Tantalum
C3, C4	100 pF Capacitor, 0402 Pkg.
C5, C6	5 pF Capacitor, 0402 Pkg.
C7, C8	0.8 pF Capacitor, 0402 Pkg.
C9, C10	4 pF Capacitor, 0402 Pkg.
L1, L2	8.2 nH Inductor, 0402 Pkg.
U1	HMC461LP3 Power Amplifier
U2, U3	Panasonic Balun, P/N EHFFD - 1619
PCB*	106483 Evaluation PCB, 10 mils
* Circuit Board Material: Rogers 4350, Er = 3.48	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

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Notes: