



**128K X 36, 256K X 18
3.3V Synchronous SRAMs
3.3V I/O, Flow-Through Outputs
Burst Counter, Single Cycle Deselect**

**IDT71V3577
IDT71V3579**

Features

- ◆ 128K x 36, 256K x 18 memory configurations
- ◆ Supports fast access times:
 - Commercial:*
 - 7.5ns up to 117MHz clock frequency
 - Commercial and Industrial:*
 - 8.0ns up to 100MHz clock frequency
 - 8.5ns up to 87MHz clock frequency
- ◆ **LBO** input selects interleaved or linear burst mode
- ◆ Self-timed write cycle with global write control (**GW**), byte write enable (**BWE**), and byte writes (**BWx**)
- ◆ 3.3V core power supply
- ◆ Power down controlled by **ZZ** input
- ◆ 3.3V I/O
- ◆ Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array

Description

The IDT71V3577/79 are high-speed SRAMs organized as 128K x 36/256K x 18. The IDT71V3577/79 SRAMs contain write, data, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V3577/79 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected (**ADV**=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the **LBO** input pin.

The IDT71V3577/79 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Description Summary

| | | | |
|---|-----------------------------------|--------|--------------|
| A0-A17 | Address Inputs | Input | Synchronous |
| \overline{CE} | Chip Enable | Input | Synchronous |
| CS ₀ , \overline{CS}_1 | Chip Selects | Input | Synchronous |
| \overline{OE} | Output Enable | Input | Asynchronous |
| \overline{GW} | Global Write Enable | Input | Synchronous |
| \overline{BWE} | Byte Write Enable | Input | Synchronous |
| \overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 , $\overline{BW}_4^{(1)}$ | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| \overline{ADV} | Burst Address Advance | Input | Synchronous |
| \overline{ADSC} | Address Status (Cache Controller) | Input | Synchronous |
| \overline{ADSP} | Address Status (Processor) | Input | Synchronous |
| LBO | Linear / Interleaved Burst Order | Input | DC |
| ZZ | Sleep Mode | Input | Asynchronous |
| I/O ₀ -I/O ₃₁ , I/OP ₁ -I/OP ₄ | Data Input / Output | I/O | Synchronous |
| V _{DD} , V _{DDQ} | Core Power, I/O Power | Supply | N/A |
| V _{SS} | Ground | Supply | N/A |

NOTE:

1. \overline{BW}_3 and \overline{BW}_4 are not applicable for the IDT71V3579.

5280 tbi 01

APRIL 2003

Pin Definitions⁽¹⁾

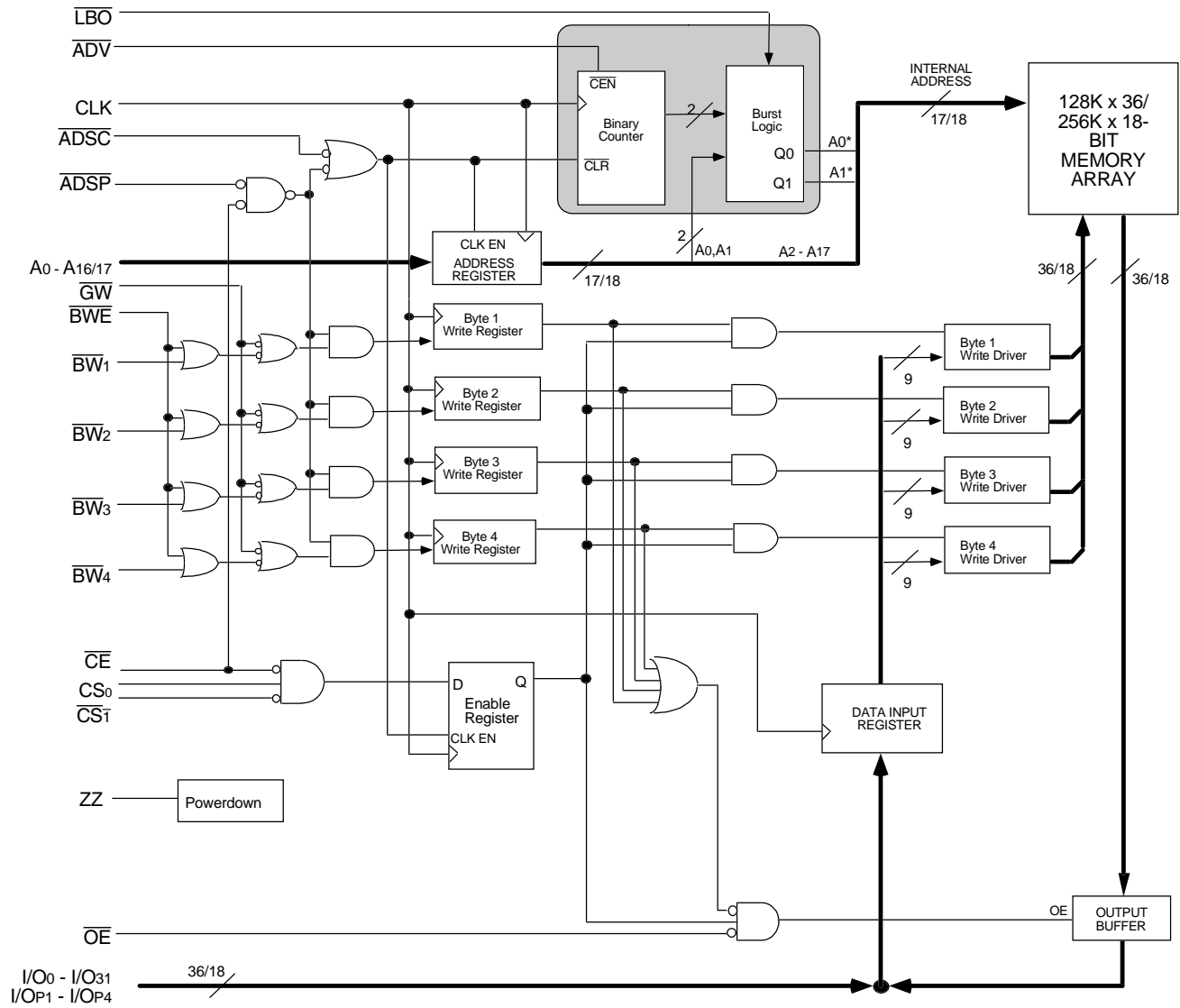
| Symbol | Pin Function | I/O | Active | Description |
|-------------------------------------|-----------------------------------|-----|--------|--|
| A0-A17 | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and \overline{ADSC} Low or \overline{ADSP} Low and \overline{CE} Low. |
| \overline{ADSC} | Address Status (Cache Controller) | I | LOW | Synchronous Address Status from Cache Controller. \overline{ADSC} is an active LOW input that is used to load the address registers with new addresses. |
| \overline{ADSP} | Address Status (Processor) | I | LOW | Synchronous Address Status from Processor. \overline{ADSP} is an active LOW input that is used to load the address registers with new addresses. \overline{ADSP} is gated by \overline{CE} . |
| \overline{ADV} | Burst Address Advance | I | LOW | Synchronous Address Advance. \overline{ADV} is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance. |
| \overline{BWE} | Byte Write Enable | I | LOW | Synchronous byte write enable gates the byte write inputs $\overline{BW1}$ - $\overline{BW4}$. If \overline{BWE} is LOW at the rising edge of CLK then \overline{BWx} inputs are passed to the next stage in the circuit. If \overline{BWE} is HIGH then the byte write inputs are blocked and only \overline{GW} can initiate a write cycle. |
| $\overline{BW1}$ - $\overline{BW4}$ | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. $\overline{BW1}$ controls I/O0-7, I/OP1, $\overline{BW2}$ controls I/O8-15, I/OP2, etc. Any active byte write causes all outputs to be disabled. |
| \overline{CE} | Chip Enable | I | LOW | Synchronous chip enable. \overline{CE} is used with CS_0 and \overline{CS}_1 to enable the IDT71V3577/79. \overline{CE} also gates \overline{ADSP} . |
| CLK | Clock | I | N/A | This is the clock input. All timing references for the device are made with respect to this input. |
| CS_0 | Chip Select 0 | I | HIGH | Synchronous active HIGH chip select. CS_0 is used with \overline{CE} and \overline{CS}_1 to enable the chip. |
| \overline{CS}_1 | Chip Select 1 | I | LOW | Synchronous active LOW chip select. \overline{CS}_1 is used with \overline{CE} and CS_0 to enable the chip. |
| \overline{GW} | Global Write Enable | I | LOW | Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. \overline{GW} supersedes individual byte write enables. |
| I/O0-I/O31 I/OP1-I/OP4 | Data Input/Output | I/O | N/A | Synchronous data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register). |
| \overline{LBO} | Linear Burst Order | I | LOW | Asynchronous burst order selection input. When \overline{LBO} is HIGH, the inter-leaved burst sequence is selected. When \overline{LBO} is LOW the Linear burst sequence is selected. \overline{LBO} is a static input and must not change state while the device is operating. |
| \overline{OE} | Output Enable | I | LOW | Asynchronous output enable. When \overline{OE} is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When \overline{OE} is HIGH the I/O pins are in a high-impedance state. |
| V _{DD} | Power Supply | N/A | N/A | 3.3V core power supply. |
| V _{DDQ} | Power Supply | N/A | N/A | 3.3V I/O Supply. |
| V _{SS} | Ground | N/A | N/A | Ground. |
| NC | No Connect | N/A | N/A | NC pins are not electrically connected to the device. |
| ZZ | Sleep Mode | 1 | HIGH | Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V3577/79 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. |

5280 tbl 02

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



5280 drw 01

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial Values | Unit |
|------------------------------------|--------------------------------------|--------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| V _{TERM} ^(3,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DD} | V |
| V _{TERM} ^(4,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DD} +0.5 | V |
| V _{TERM} ^(5,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DDQ} +0.5 | V |
| T _A ⁽⁷⁾ | Commercial Operating Temperature | -0 to +70 | °C |
| | Industrial Operating Temperature | -40 to +85 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | °C |
| P _T | Power Dissipation | 2.0 | W |
| I _{OUT} | DC Output Current | 50 | mA |

5280 tbl 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD} terminals only.
- V_{DDQ} terminals only.
- Input terminals only.
- I/O terminals only.
- This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
- T_A is the "instant on" case temperature.

Recommended Operating Temperature Supply Voltage

| Grade | Temperature ⁽¹⁾ | V _{SS} | V _{DD} | V _{DDQ} |
|------------|----------------------------|-----------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 0V | 3.3V±5% | 3.3V±5% |
| Industrial | -40°C to +85°C | 0V | 3.3V±5% | 3.3V±5% |

5280 tbl 04

NOTES:

- T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------|---------------------|------|--------------------------------------|------|
| V _{DD} | Core Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| V _{DDQ} | I/O Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| V _{SS} | Supply Voltage | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage - Inputs | 2.0 | — | V _{DD} +0.3 | V |
| V _{IH} | Input High Voltage - I/O | 2.0 | — | V _{DDQ} +0.3 ⁽¹⁾ | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽²⁾ | — | 0.8 | V |

5280 tbl 06

NOTES:

- V_{IH} (max) = V_{DDQ} + 1.0V for pulse width less than t_{CYC/2}, once per cycle.
- V_{IL} (min) = -1.0V for pulse width less than t_{CYC/2}, once per cycle.

100 Pin TQFP Capacitance

(T_A = +25° C, f = 1.0mhz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|-----------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 5 | pF |
| C _{VO} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

5280 tbl 07

119 BGA Capacitance

(T_A = +25° C, f = 1.0mhz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|-----------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 7 | pF |
| C _{VO} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

5280 tbl 07a

165 fBGA Capacitance

(T_A = +25° C, f = 1.0mhz)

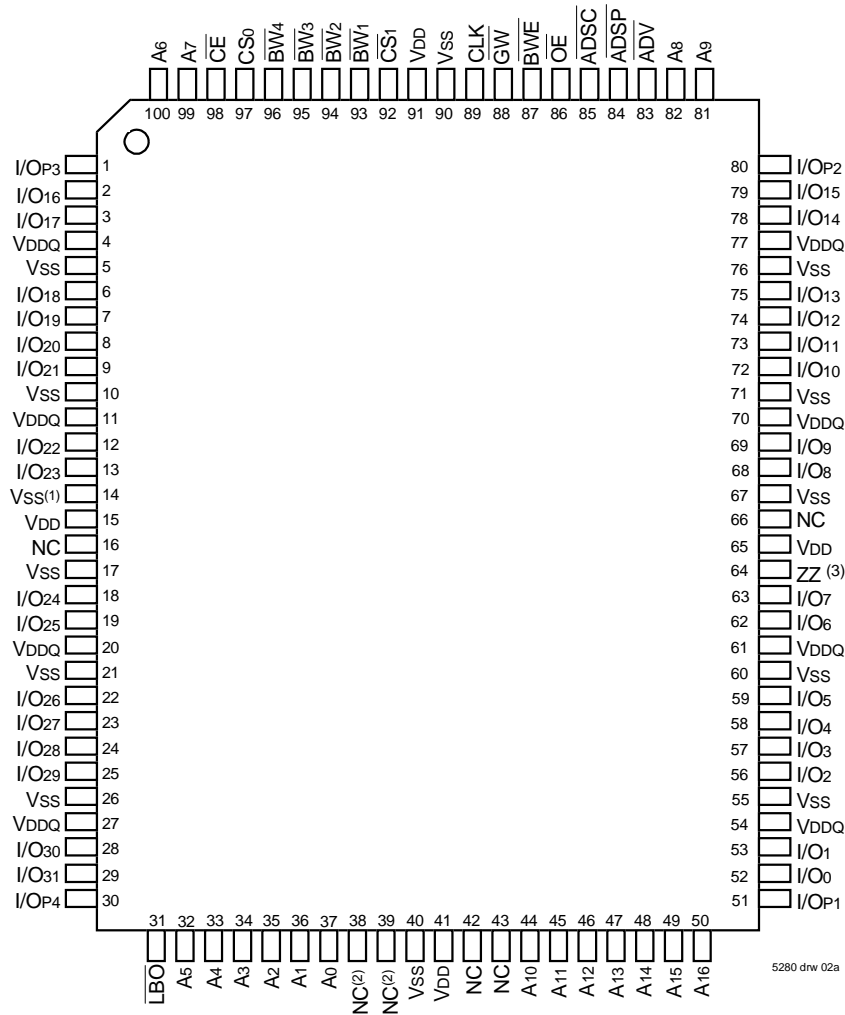
| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|-----------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 7 | pF |
| C _{VO} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

5280 tbl 07b

NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration – 128K x 36

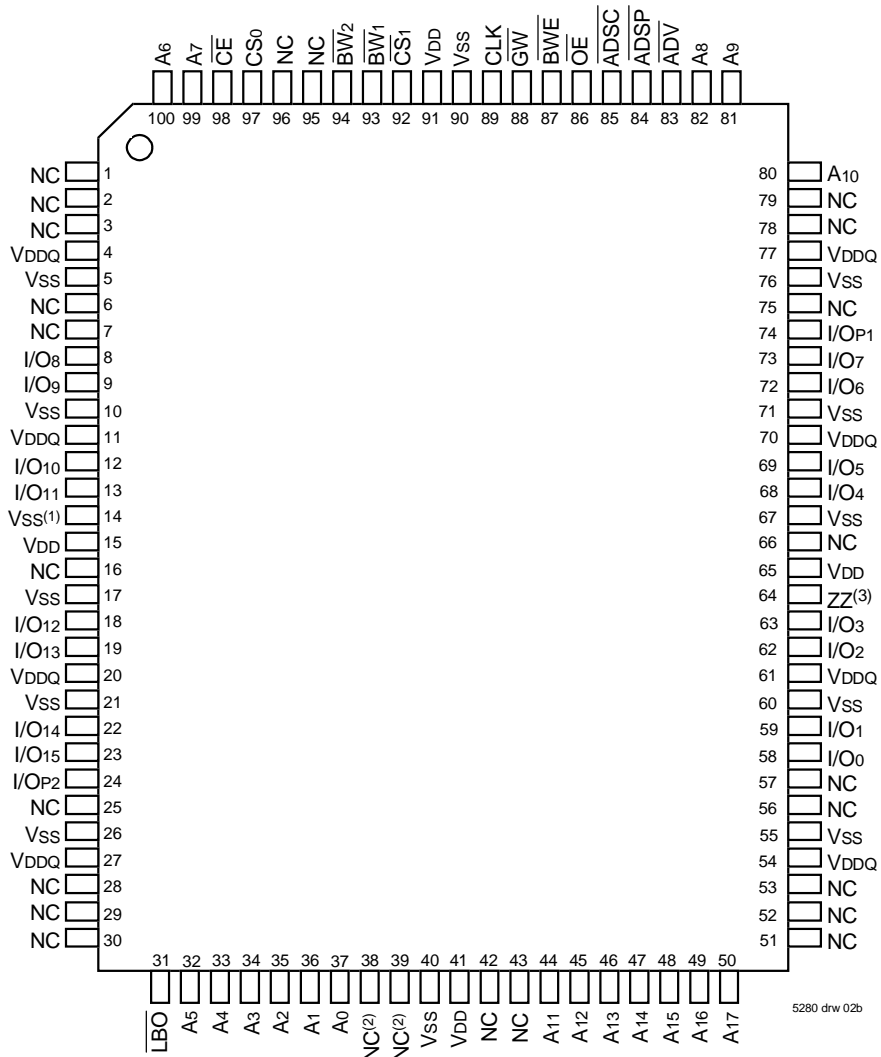


100 TQFP Top View

NOTES:

1. Pin 14 does not have to be directly connected to Vss as long as the input voltage is $\leq V_{IL}$.
2. Pins 38 and 39 can be either NC or connected to Vss.
3. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 256K x 18



100 TQFP Top View

NOTES:

1. Pin 14 does not have to be directly connected to Vss as long as the input voltage is $\leq V_{IL}$.
2. Pins 38 and 39 can be either NC or connected to Vss.
3. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 128K x 36, 119 BGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|-------------------|--------------------|--------------------|----------------------|--------------------|--------------------|-------------------|
| A | VDDQ | A6 | A4 | ADSP | A8 | A16 | VDDQ |
| B | NC | CS ₀ | A3 | ADSC | A9 | CS ₁ | NC |
| C | NC | A7 | A2 | VDD | A12 | A15 | NC |
| D | I/O ₁₆ | I/OP ₃ | VSS | NC | VSS | I/OP ₂ | I/O ₁₅ |
| E | I/O ₁₇ | I/O ₁₈ | VSS | CE | VSS | I/O ₁₃ | I/O ₁₄ |
| F | VDDQ | I/O ₁₉ | VSS | OE | VSS | I/O ₁₂ | VDDQ |
| G | I/O ₂₀ | I/O ₂₁ | BW ₃ | ADV | BW ₂ | I/O ₁₁ | I/O ₁₀ |
| H | I/O ₂₂ | I/O ₂₃ | VSS | GW | VSS | I/O ₉ | I/O ₈ |
| J | VDDQ | VDD | NC | VDD | NC | VDD | VDDQ |
| K | I/O ₂₄ | I/O ₂₆ | VSS | CLK | VSS | I/O ₆ | I/O ₇ |
| L | I/O ₂₅ | I/O ₂₇ | BW ₄ | NC ⁽²⁾ | BW ₁ | I/O ₄ | I/O ₅ |
| M | VDDQ | I/O ₂₈ | VSS | BWE | VSS | I/O ₃ | VDDQ |
| N | I/O ₂₉ | I/O ₃₀ | VSS | A1 | VSS | I/O ₂ | I/O ₁ |
| P | I/O ₃₁ | I/OP ₄ | VSS | A0 | VSS | I/O ₀ | I/OP ₁ |
| R | NC | A5 | LBO | VDD | VSS | A13 | NC |
| T | NC | NC | A10 | A11 | A14 | NC | ZZ ⁽³⁾ |
| U | VDDQ | DNU ⁽⁴⁾ | DNU ⁽⁴⁾ | DNU ^(2,4) | DNU ⁽⁴⁾ | DNU ⁽⁴⁾ | VDDQ |

5280 drw 02c

Top View

Pin Configuration – 256K x 18, 119 BGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|-------------------|--------------------|--------------------|----------------------|--------------------|--------------------|-------------------|
| A | VDDQ | A6 | A4 | ADSP | A8 | A16 | VDDQ |
| B | NC | CS ₀ | A3 | ADSC | A9 | CS ₁ | NC |
| C | NC | A7 | A2 | VDD | A13 | A17 | NC |
| D | I/O ₈ | NC | VSS | NC | VSS | I/O ₇ | NC |
| E | NC | I/O ₉ | VSS | CE | VSS | NC | I/O ₆ |
| F | VDDQ | NC | VSS | OE | VSS | I/O ₅ | VDDQ |
| G | NC | I/O ₁₀ | BW ₂ | ADV | VSS | NC | I/O ₄ |
| H | I/O ₁₁ | NC | VSS | GW | VSS | I/O ₃ | NC |
| J | VDDQ | VDD | NC | VDD | NC | VDD | VDDQ |
| K | NC | I/O ₁₂ | VSS | CLK | VSS | NC | I/O ₂ |
| L | I/O ₁₃ | NC | VSS | NC ⁽²⁾ | BW ₁ | I/O ₁ | NC |
| M | VDDQ | I/O ₁₄ | VSS | BWE | VSS | NC | VDDQ |
| N | I/O ₁₅ | NC | VSS | A1 | VSS | I/O ₀ | NC |
| P | NC | I/OP ₂ | VSS | A0 | VSS | NC | I/OP ₁ |
| R | NC | A5 | LBO | VDD | VSS | A12 | NC |
| T | NC | A10 | A15 | NC | A14 | A11 | ZZ ⁽³⁾ |
| U | VDDQ | DNU ⁽⁴⁾ | DNU ⁽⁴⁾ | DNU ^(2,4) | DNU ⁽⁴⁾ | DNU ⁽⁴⁾ | VDDQ |

5280 drw 02d

Top View

NOTES:

1. R5 does not have to be directly connected to Vss as long as the input voltage is $\leq V_{IL}$.
2. L4 and U4 can be either NC or connected to Vss.
3. T7 can be left unconnected and the device will always remain in active mode.
4. DNU = Do not use: Pins U2, U3, U4, U5 and U6 are reserved for respective JTAG pins: TDI, TDO, TMS, TCK and $\overline{\text{TRST}}$ on future revisions. Within the current version these pins are not connected.

Pin Configuration – 128K x 36, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|-------------------|-------------------|-------------------|--------------------|-------------------|--------------------|-------------------|-------------------|-------|-------------------|
| A | NC ⁽⁴⁾ | A7 | \overline{CE}_1 | \overline{BW}_3 | \overline{BW}_2 | \overline{CS}_1 | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A8 | NC |
| B | NC | A6 | CS0 | \overline{BW}_4 | \overline{BW}_1 | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A9 | NC ⁽⁴⁾ |
| C | I/OP3 | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/OP2 |
| D | I/O17 | I/O16 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O15 | I/O14 |
| E | I/O19 | I/O18 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O13 | I/O12 |
| F | I/O21 | I/O20 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O11 | I/O10 |
| G | I/O23 | I/O22 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O9 | I/O8 |
| H | VSS ⁽¹⁾ | NC ⁽²⁾ | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ ⁽³⁾ |
| J | I/O25 | I/O24 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O7 | I/O6 |
| K | I/O27 | I/O26 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O5 | I/O4 |
| L | I/O29 | I/O28 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O3 | I/O2 |
| M | I/O31 | I/O30 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O1 | I/O0 |
| N | I/OP4 | NC | VDDQ | VSS | DNU ⁽⁵⁾ | NC ⁽⁴⁾ | NC ⁽²⁾ | VSS | VDDQ | NC | I/OP1 |
| P | NC | NC ⁽⁴⁾ | A5 | A2 | DNU ⁽⁵⁾ | A1 | DNU ⁽⁵⁾ | A10 | A13 | A14 | NC ⁽⁴⁾ |
| R | \overline{LBO} | NC ⁽⁴⁾ | A4 | A3 | DNU ⁽⁵⁾ | A0 | DNU ⁽⁵⁾ | A11 | A12 | A15 | A16 |

5280 tbl 17

Pin Configuration – 256K x 18, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|-------------------|-------------------|-------------------|--------------------|-------------------|--------------------|-------------------|-------------------|------|-------------------|
| A | NC ⁽⁴⁾ | A7 | \overline{CE}_1 | \overline{BW}_2 | NC | \overline{CS}_1 | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A8 | A10 |
| B | NC | A6 | CS0 | NC | \overline{BW}_1 | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A9 | NC ⁽⁴⁾ |
| C | NC | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/OP1 |
| D | NC | I/O8 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O7 |
| E | NC | I/O9 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O6 |
| F | NC | I/O10 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O5 |
| G | NC | I/O11 | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O4 |
| H | VSS ⁽¹⁾ | NC ⁽²⁾ | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ ⁽³⁾ |
| J | I/O12 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O3 | NC |
| K | I/O13 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O2 | NC |
| L | I/O14 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O1 | NC |
| M | I/O15 | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O0 | NC |
| N | I/OP2 | NC | VDDQ | VSS | DNU ⁽⁵⁾ | NC ⁽⁴⁾ | NC ⁽²⁾ | VSS | VDDQ | NC | NC |
| P | NC | NC ⁽⁴⁾ | A5 | A2 | DNU ⁽⁵⁾ | A1 | DNU ⁽⁵⁾ | A11 | A14 | A15 | NC ⁽⁴⁾ |
| R | \overline{LBO} | NC ⁽⁴⁾ | A4 | A3 | DNU ⁽⁵⁾ | A0 | DNU ⁽⁵⁾ | A12 | A13 | A16 | A17 |

5280 tbl 17a

NOTES:

- H1 does not have to be directly Vss as long as input voltage is $\leq V_{IL}$
- H2 and N7 can be either NC or connected to Vss.
- H11 can be left unconnected and the device will always remain in active mode.
- Pins P11, N6, B11, A1, R2 and P2 are reserved for 9M, 18M, 36M, 72M, 144M and 288M respectively.
- DNU = Do not use; Pins P5, P7, R5, R7 and N5 are reserved for respective JTAG pins: TDI, TDO, TMS, TCK and \overline{TRST} on future revisions. Within the current version these pins are not connected.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 5\%$)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|------------|--|---|------|------|---------|
| $ I_{L} $ | Input Leakage Current | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 5 | μA |
| $ I_{L} $ | ZZ and $\overline{LB0}$ Input Leakage Current ⁽¹⁾ | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 30 | μA |
| $ I_{LO} $ | Output Leakage Current | $V_{OUT} = 0V \text{ to } V_{DDQ}, \text{ Device Deselected}$ | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = +8mA, V_{DD} = \text{Min.}$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -8mA, V_{DD} = \text{Min.}$ | 2.4 | — | V |

5280 tbl 08

NOTE:

- The $\overline{LB0}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ in will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ⁽¹⁾

| Symbol | Parameter | Test Conditions | 7.5ns | 8ns | | 8.5ns | | Unit |
|-----------|------------------------------------|---|------------|-------|-----|-------|-----|------|
| | | | Com'l Only | Com'l | Ind | Com'l | Ind | |
| I_{DD} | Operating Power Supply Current | Device Selected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$ | 255 | 200 | 210 | 180 | 190 | mA |
| I_{SB1} | CMOS Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2,3)}$ | 30 | 30 | 35 | 30 | 35 | mA |
| I_{SB2} | Clock Running Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$ | 90 | 85 | 95 | 80 | 90 | mA |
| I_{ZZ} | Full Sleep Mode Supply Current | $ZZ \geq V_{HD}, V_{DD} = \text{Max.}$ | 30 | 30 | 35 | 30 | 35 | mA |

5280 tbl 09

NOTES:

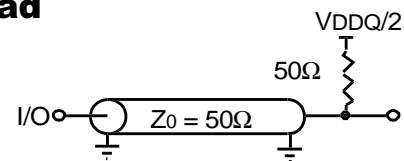
- All values are maximum guaranteed values.
- At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$ while $\overline{ADSC} = \text{LOW}$; $f=0$ means no input lines are changing.
- For I/Os $V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V$. For other inputs $V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V$.

AC Test Conditions ($V_{DDQ} = 3.3V$)

| | |
|--------------------------------|--------------|
| Input Pulse Levels | 0 to 3V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| AC Test Load | See Figure 1 |

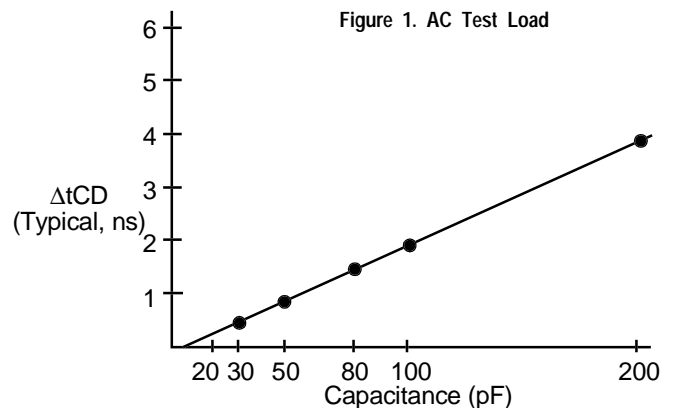
5280 tbl 10

AC Test Load



5280 drw 03

Figure 1. AC Test Load



5280 drw 05

Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table (1,3)

| Operation | Address Used | \overline{CE} | CS_0 | \overline{CS}_1 | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | \overline{GW} | \overline{BWE} | \overline{BW}_x | $\overline{OE}^{(2)}$ | CLK | I/O |
|------------------------------|--------------|-----------------|--------|-------------------|-------------------|-------------------|------------------|-----------------|------------------|-------------------|-----------------------|-----|------|
| Deselected Cycle, Power Down | None | H | X | X | X | L | X | X | X | X | X | ↑ | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | L | X | X | X | X | X | X | ↑ | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | L | X | X | X | X | X | X | ↑ | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | X | L | X | X | X | X | X | ↑ | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | X | L | X | X | X | X | X | ↑ | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | L | ↑ | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | H | ↑ | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | H | X | L | ↑ | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | L | ↑ | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | H | ↑ | HI-Z |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | L | X | ↑ | DIN |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | L | X | X | X | ↑ | DIN |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | H | ↑ | HI-Z |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | H | ↑ | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | H | ↑ | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | H | ↑ | HI-Z |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | L | X | ↑ | DIN |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | X | X | ↑ | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | L | X | ↑ | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | X | X | ↑ | DIN |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | H | ↑ | HI-Z |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | H | ↑ | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | H | ↑ | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | H | ↑ | HI-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | L | X | ↑ | DIN |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | X | X | ↑ | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | L | X | ↑ | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | X | X | ↑ | DIN |

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. \overline{OE} is an asynchronous input.
3. ZZ - low for the table.

5280 bl 11

Synchronous Write Function Truth Table (1, 2)

| Operation | \overline{GW} | BWE | BW ₁ | \overline{BW}_2 | \overline{BW}_3 | \overline{BW}_4 |
|-----------------------------|-----------------|-----|-----------------|-------------------|-------------------|-------------------|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write all Bytes | L | X | X | X | X | X |
| Write all Bytes | H | L | L | L | L | L |
| Write Byte 1 ⁽⁶⁾ | H | L | L | H | H | H |
| Write Byte 2 ⁽⁶⁾ | H | L | H | L | H | H |
| Write Byte 3 ⁽⁶⁾ | H | L | H | H | L | H |
| Write Byte 4 ⁽⁶⁾ | H | L | H | H | H | L |

5280 tbl 12

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. \overline{BW}_3 and \overline{BW}_4 are not applicable for the IDT71V3579.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table (1)

| Operation ⁽²⁾ | \overline{OE} | ZZ | I/O Status | Power |
|--------------------------|-----------------|----|------------------|---------|
| Read | L | L | Data Out | Active |
| Read | H | L | High-Z | Active |
| Write | X | L | High-Z - Data In | Active |
| Deselected | X | L | High-Z | Standby |
| Sleep Mode | X | H | High-Z | Sleep |

5280 tbl 13

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}=V_{DD}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

5280 tbl 14

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}=V_{SS}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

5280 tbl 15

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC Electrical Characteristics

(VDD = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

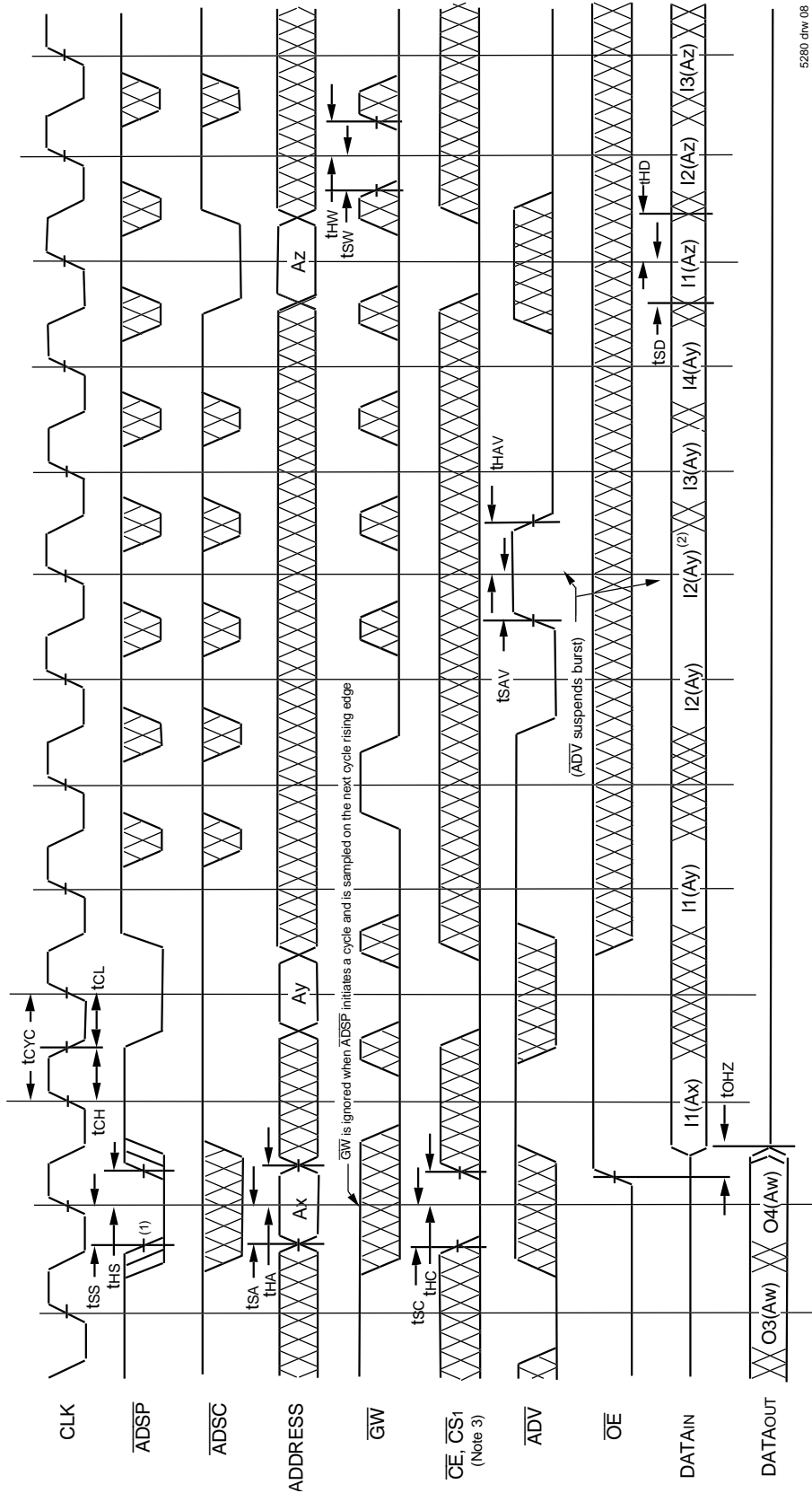
| Symbol | Parameter | 7.5ns ⁽⁵⁾ | | 8ns | | 8.5ns | | Unit |
|--|-------------------------------------|----------------------|------|------|------|-------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock Parameter | | | | | | | | |
| t _{CYC} | Clock Cycle Time | 8.5 | — | 10 | — | 11.5 | — | ns |
| t _{CH} ⁽¹⁾ | Clock High Pulse Width | 3 | — | 4 | — | 4.5 | — | ns |
| t _{CL} ⁽¹⁾ | Clock Low Pulse Width | 3 | — | 4 | — | 4.5 | — | ns |
| Output Parameters | | | | | | | | |
| t _{CD} | Clock High to Valid Data | — | 7.5 | — | 8 | — | 8.5 | ns |
| t _{CD} | Clock High to Data Change | 2 | — | 2 | — | 2 | — | ns |
| t _{CLZ} ⁽²⁾ | Clock High to Output Active | 0 | — | 0 | — | 0 | — | ns |
| t _{CHZ} ⁽²⁾ | Clock High to Data High-Z | 2 | 3.5 | 2 | 3.5 | 2 | 3.5 | ns |
| t _{OE} | Output Enable Access Time | — | 3.5 | — | 3.5 | — | 3.5 | ns |
| t _{OLZ} ⁽²⁾ | Output Enable Low to Output Active | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽²⁾ | Output Enable High to Output High-Z | — | 3.5 | — | 3.5 | — | 3.5 | ns |
| Set Up Times | | | | | | | | |
| t _{SA} | Address Setup Time | 1.5 | — | 2 | — | 2 | — | ns |
| t _{SS} | Address Status Setup Time | 1.5 | — | 2 | — | 2 | — | ns |
| t _{SD} | Data In Setup Time | 1.5 | — | 2 | — | 2 | — | ns |
| t _{SW} | Write Setup Time | 1.5 | — | 2 | — | 2 | — | ns |
| t _{SAV} | Address Advance Setup Time | 1.5 | — | 2 | — | 2 | — | ns |
| t _{SC} | Chip Enable/Select Setup Time | 1.5 | — | 2 | — | 2 | — | ns |
| Hold Times | | | | | | | | |
| t _{HA} | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HS} | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HD} | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HW} | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HAV} | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HC} | Chip Enable/Select Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| Sleep Mode and Configuration Parameters | | | | | | | | |
| t _{ZZPW} | ZZ Pulse Width | 100 | — | 100 | — | 100 | — | ns |
| t _{ZZR} ⁽³⁾ | ZZ Recovery Time | 100 | — | 100 | — | 100 | — | ns |
| t _{CFG} ⁽⁴⁾ | Configuration Set-up Time | 34 | — | 40 | — | 50 | — | ns |

NOTES:

5280 tbl 16

1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{\text{LBO}}$ input. $\overline{\text{LBO}}$ is a static input and must not change during normal operation.
5. Commercial temperature range only.

Timing Waveform of Write Cycle No. 1 - \overline{GW} Controlled (1,2,3)

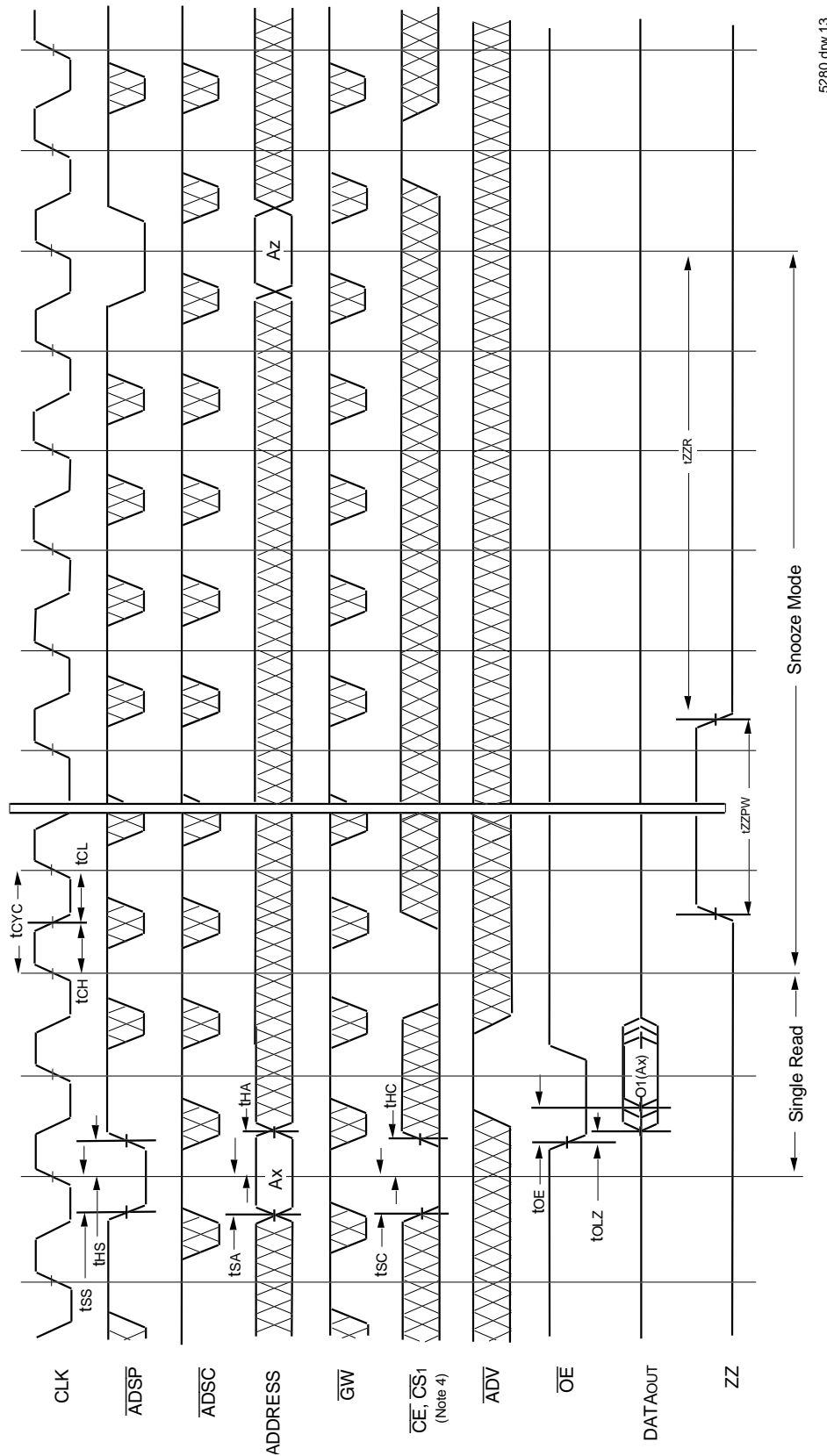


5280 dhw 08

NOTES:

1. ZZ input is LOW, \overline{BWE} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. 04(Aw) represents the final output data in the burst sequence of the base address A_w . 11(Ax) represents the first input from the external address A_y ; 12(Ay) represents the next input data in the burst sequence of the base address A_y , etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input. In the case of input 12(Ay) this data is valid for two cycles because ADV is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes (1,2,3)

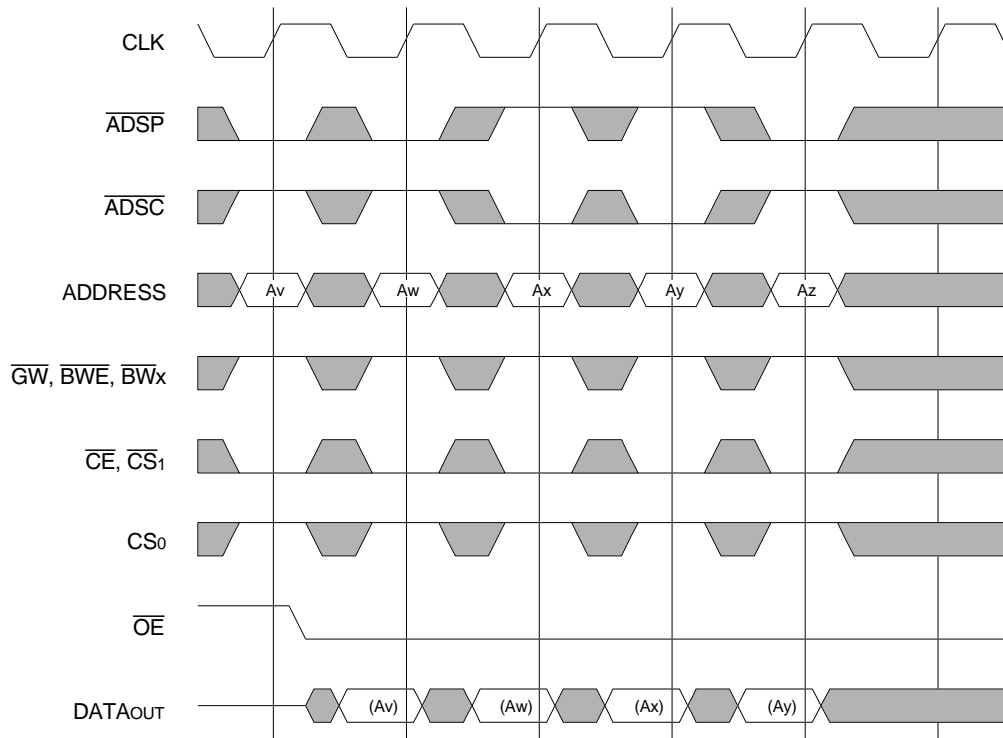


5280 drw 13

NOTES:

1. Device must power up in deselected Mode.
2. LBO is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform

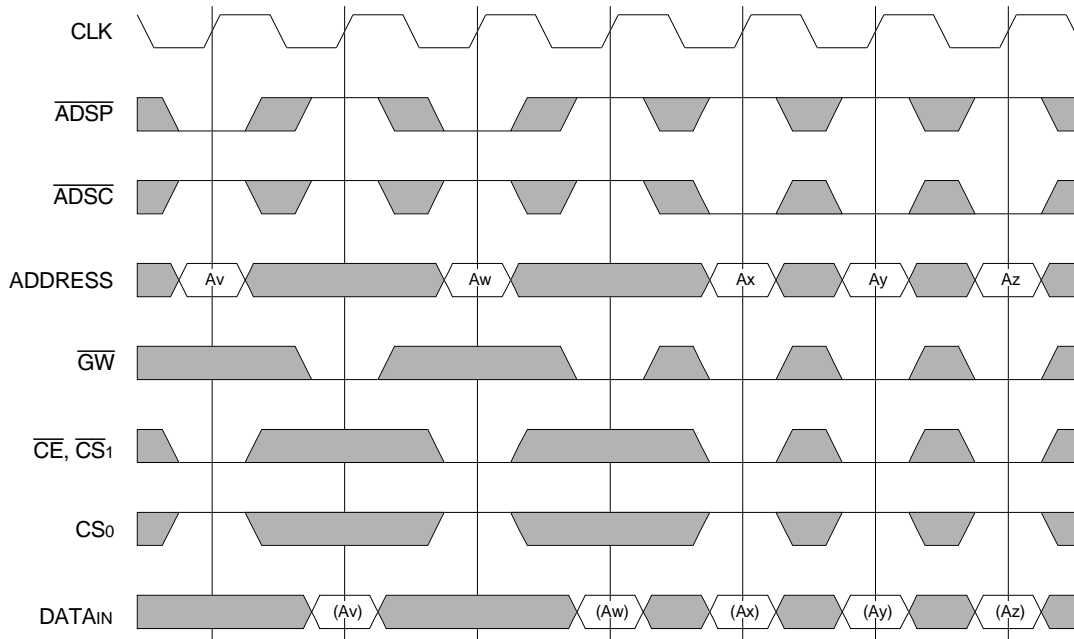


NOTES:

1. ZZ input is LOW, \overline{ADV} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, \overline{ADSP} and \overline{ADSC} function identically and are therefore interchangeable.

5280 drw 10

Non-Burst Write Cycle Timing Waveform

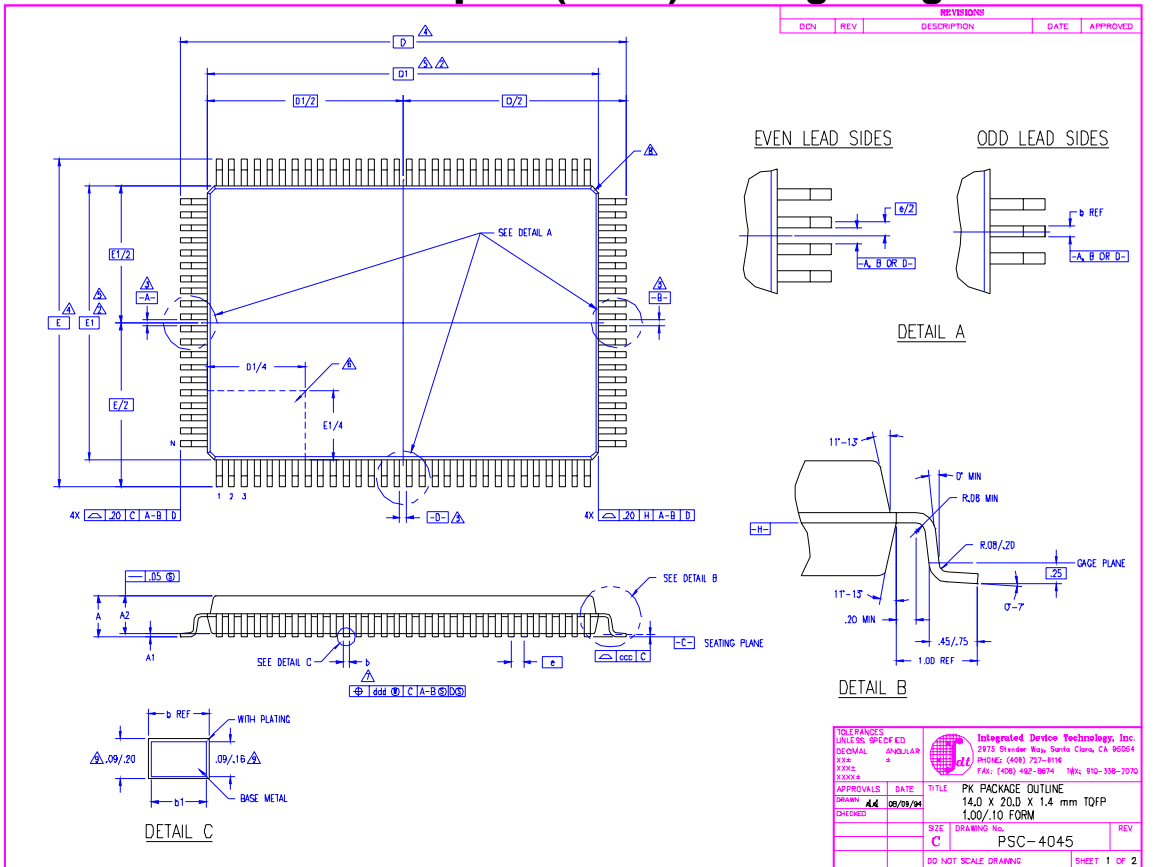


NOTES:

1. ZZ input is LOW, \overline{ADV} and \overline{OE} are HIGH, and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only \overline{GW} writes are shown, the functionality of \overline{BWE} and \overline{BWx} together is the same as \overline{GW} .
4. For write cycles, \overline{ADSP} and \overline{ADSC} have different limitations.

5280 drw 11

100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline

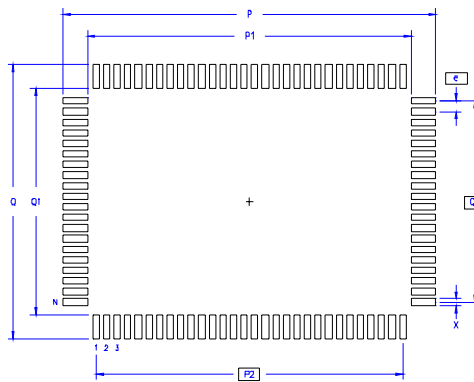


| SYMBOL | JEDEC VARIATION | | | UNIT |
|--------|-----------------|------|------|------|
| | MIN | NOM | MAX | |
| A | - | - | 1.60 | |
| A1 | .05 | .10 | .15 | |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | 22.00 BSC | | | 4 |
| D1 | 20.00 BSC | | | 5,2 |
| E | 16.00 BSC | | | 4 |
| E1 | 14.00 BSC | | | 5,2 |
| N | 100 | | | |
| ND | 30 | | | |
| NE | 20 | | | |
| e | .65 BSC | | | |
| b | .22 | .32 | .38 | 7 |
| b1 | .22 | .30 | .33 | |
| ccc | - | - | .10 | |
| ddd | - | - | .13 | |

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
- DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION, ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE, D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MD-136, VARIATION DJ AND BX

LAND PATTERN DIMENSIONS



| | MIN | MAX |
|----|-----------|-------|
| P | 22.80 | 23.00 |
| P1 | 19.80 | 20.00 |
| P2 | 18.85 BSC | |
| Q | 16.80 | 17.00 |
| Q1 | 13.80 | 14.00 |
| Q2 | 12.35 BSC | |
| X | .30 | .50 |
| e | .65 BSC | |
| N | 100 | |

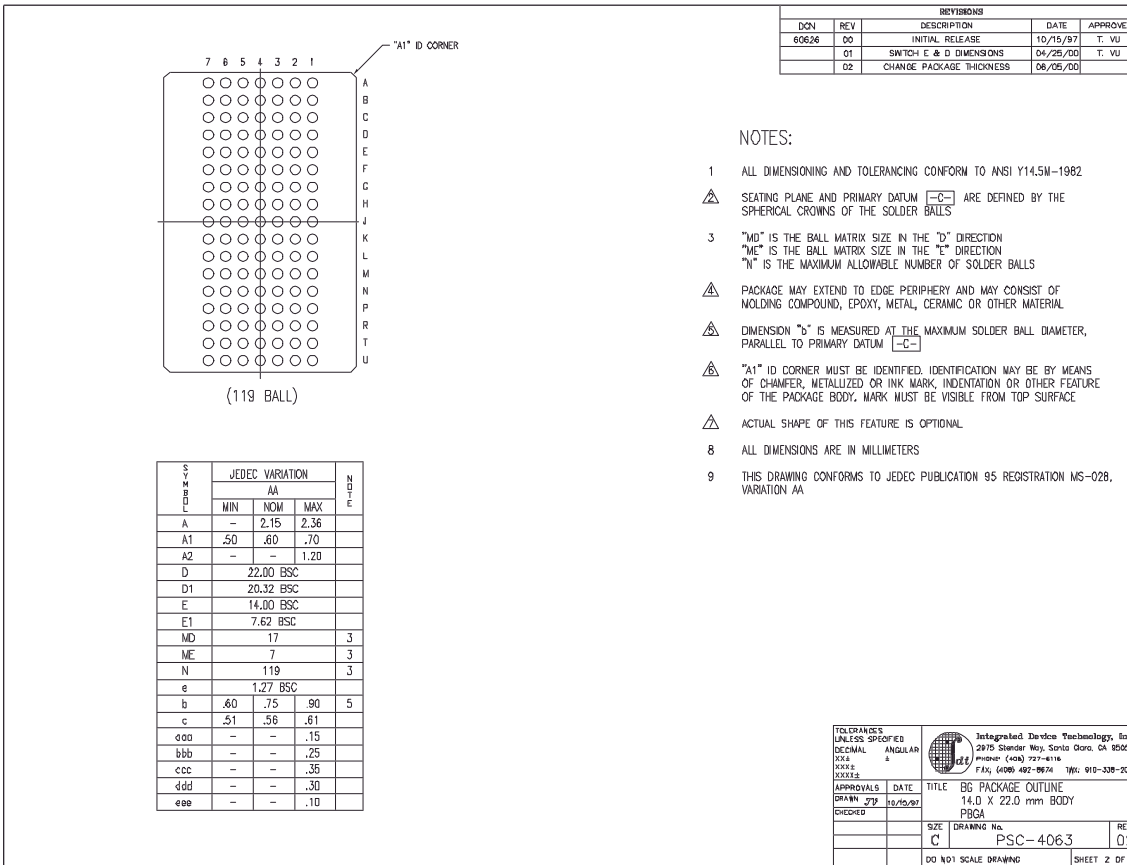
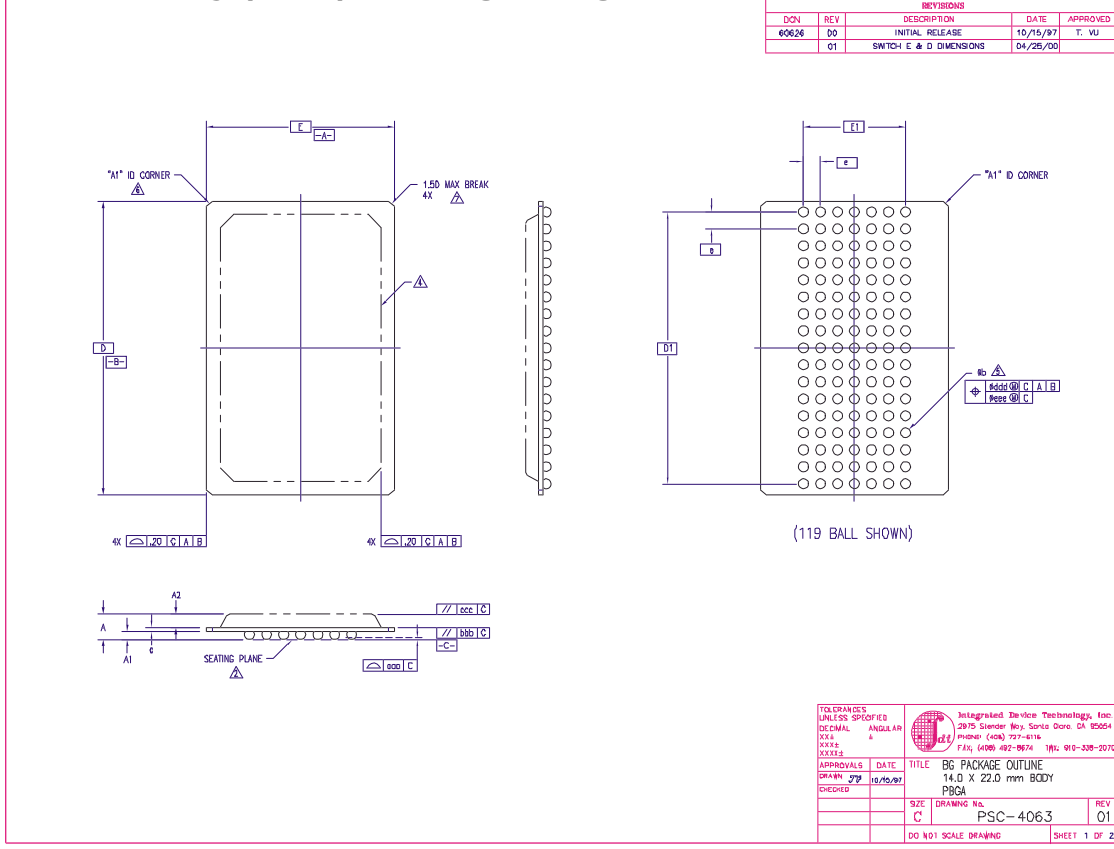
TOLERANCES UNLESS SPECIFIED:
 DECIMAL ±
 ANGULAR °
 HOLE Ø
 SURFACE S

Integrated Device Technology, Inc.
 2975 Stoner Way, Santa Clara, CA 95054
 PHONE: (408) 727-8110 FAX: (408) 492-8074 TEL: 910-330-2070

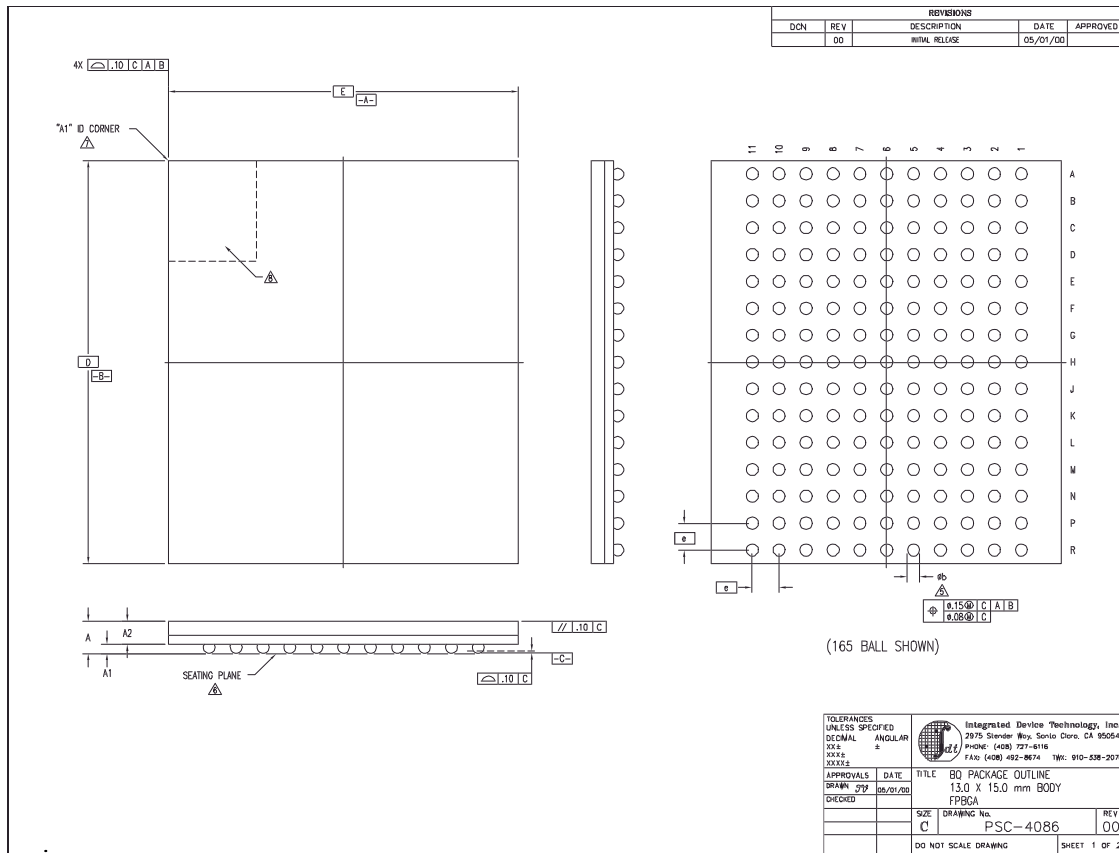
APPROVALS


| APPROVALS | DATE | TITLE | PK PACKAGE OUTLINE | REV |
|-----------|----------|---------------------------|----------------------|--------------|
| ADL | 08/09/94 | 14.0 X 20.0 X 1.4 mm TQFP | 1.00/10 FORM | |
| | | SIZE C | DRAWING No. PSC-4045 | |
| | | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

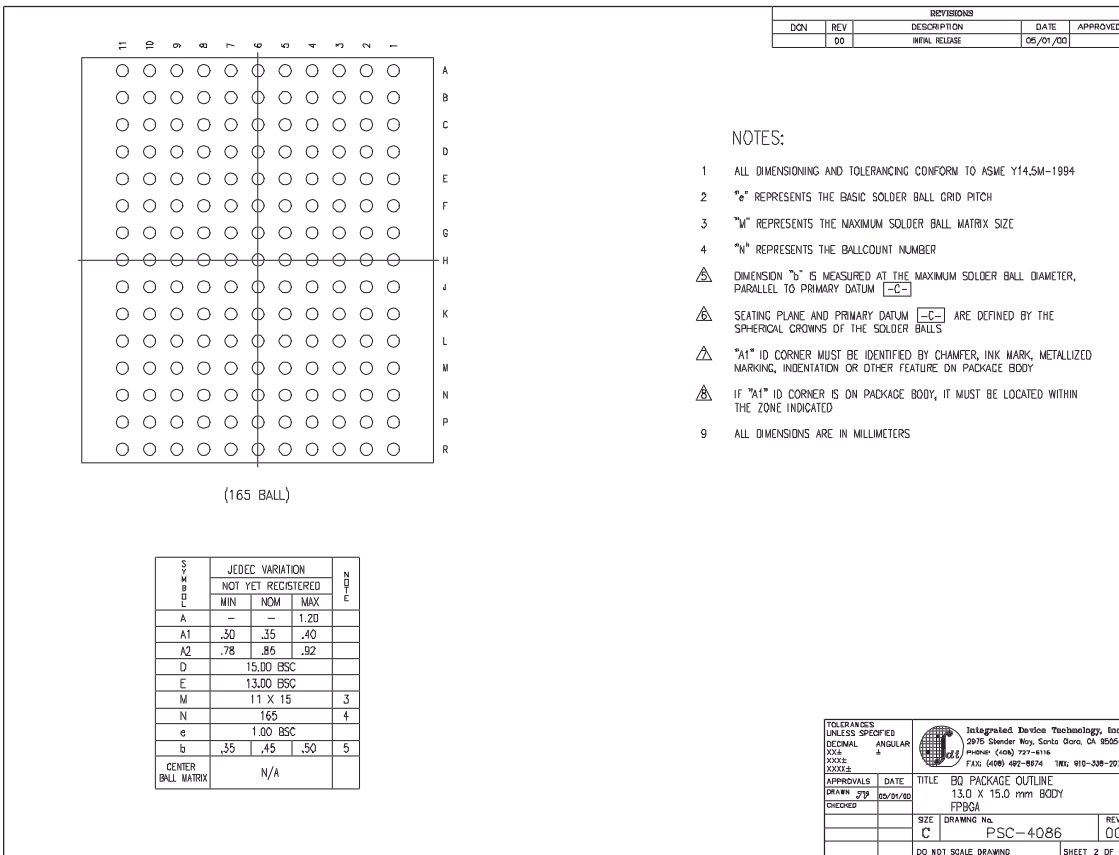
119 Ball Grid Array (BGA) Package Diagram Outline



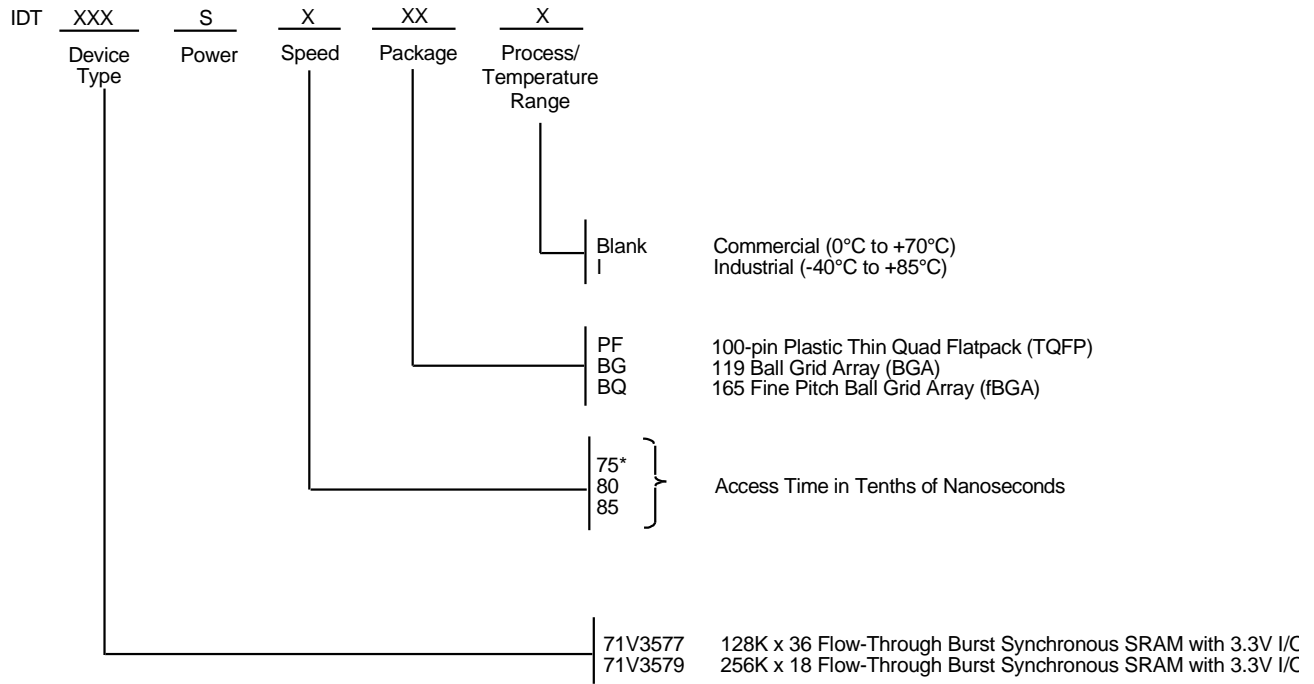
165 Fine Pitch Ball Grid Array (fBGA) Package Diagram Outline



| | | |
|-----------------------------|----------|---|
| TOLERANCES UNLESS SPECIFIED | |  Integrated Device Technology, Inc. 2975 Stander Way, Santa Clara, CA 95054 Phone: (408) 737-6116 Fax: (408) 492-8674 TEL: 910-538-2070 |
| DECIMAL | ANGULAR | |
| XXX | A | |
| APPROVALS | DATE | TITLE |
| DRAWN: STP | 05/01/00 | B0 PACKAGE OUTLINE |
| CHECKED: | | 13.0 X 15.0 mm BODY |
| | | FPBGA |
| | SIZE | DRAWING No. |
| | C | PSC-4086 |
| | | REV |
| | | 00 |
| DO NOT SCALE DRAWING | | SHEET 1 OF 2 |



Ordering Information



*Commercial temperature range only.

Datasheet Document History

| | | |
|----------|---------------------|--|
| 7/23/99 | | Updated to new format |
| 9/17/99 | Pg. 2 | Revised I/O pin description |
| | Pg. 3 | Revised block diagram for flow-through functionality |
| | Pg. 8 | Revised t _{SB1} and t _{ZZ} for speeds 7.5 to 8.5ns |
| | Pg. 18 | Added 119-lead BGA package diagram |
| | Pg. 20 | Added Datasheet Document History |
| 12/31/99 | Pp. 1, 4, 8, 11, 19 | Added Industrial Temperature range offerings |
| 04/03/00 | Pg. 18 | Added 100pinTQFP Package Diagram Outline |
| | Pg. 4 | Add capacitance table for BGA package; add Industrial temperature to table; Insert note to Absolute Max Ratings and Recommended Operating Temperature tables |
| 06/01/00 | | Add new package offering, 13 x 15mm 165 fBGA |
| | Pg. 20 | Correct 119BGA Package Diagram Outline |
| 07/15/00 | Pg. 7 | Add note reference to BG119 pinout |
| | Pg. 8 | Add DNU reference note to BQ165 pinout |
| | Pg. 20 | Update BG119 Package Diagram Outline Dimensions |
| 10/25/00 | | Remove Preliminary status |
| | Pg.8 | Add reference note to pin N5 on BQ165 pinout, reserved for JTAG $\overline{\text{TRST}}$ |
| 04/22/03 | Pg.4 | Updated 165 BGA table information from TBD to 7 |



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