# 3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

**IDT74LVCHR16543A**

## FEATURES:

- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Vcc = 3.3V ± 0.3V, Normal Range**
- **Vcc = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **All inputs, outputs, and I/O are 5V tolerant**
- **Supports hot insertion**
- **Available in SSOP, TSSOP, and TVSOP packages**

## DRIVE FEATURES:

- **Balanced Output Drivers: ±12mA**
- **Low switching noise**

## APPLICATIONS:

- **5V and 3.3V mixed voltage systems**
- **Data communication and telecommunication systems**

## DESCRIPTION:

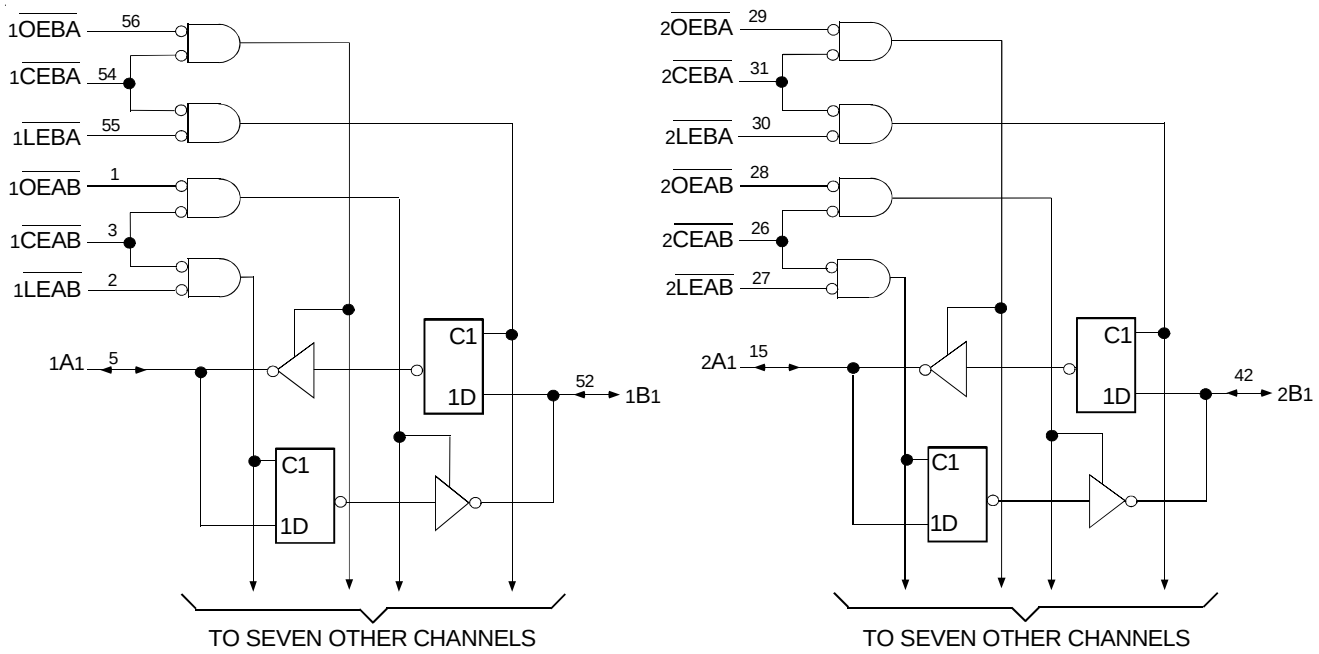
The LVCHR16543A 16-bit registered transceiver is built using advanced dual metal CMOS technology. The LVCHR16543A device can be used as two independent 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow. The A-to-B enable ($\overline{CEAB}$) must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to Vcc through a pullup resistor; the minmum value of the resistor is determined by the current sinking capability of the driver.

The LVCHR16543A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. The driver has been designed to drive ±12mA at the designated threshold levels.

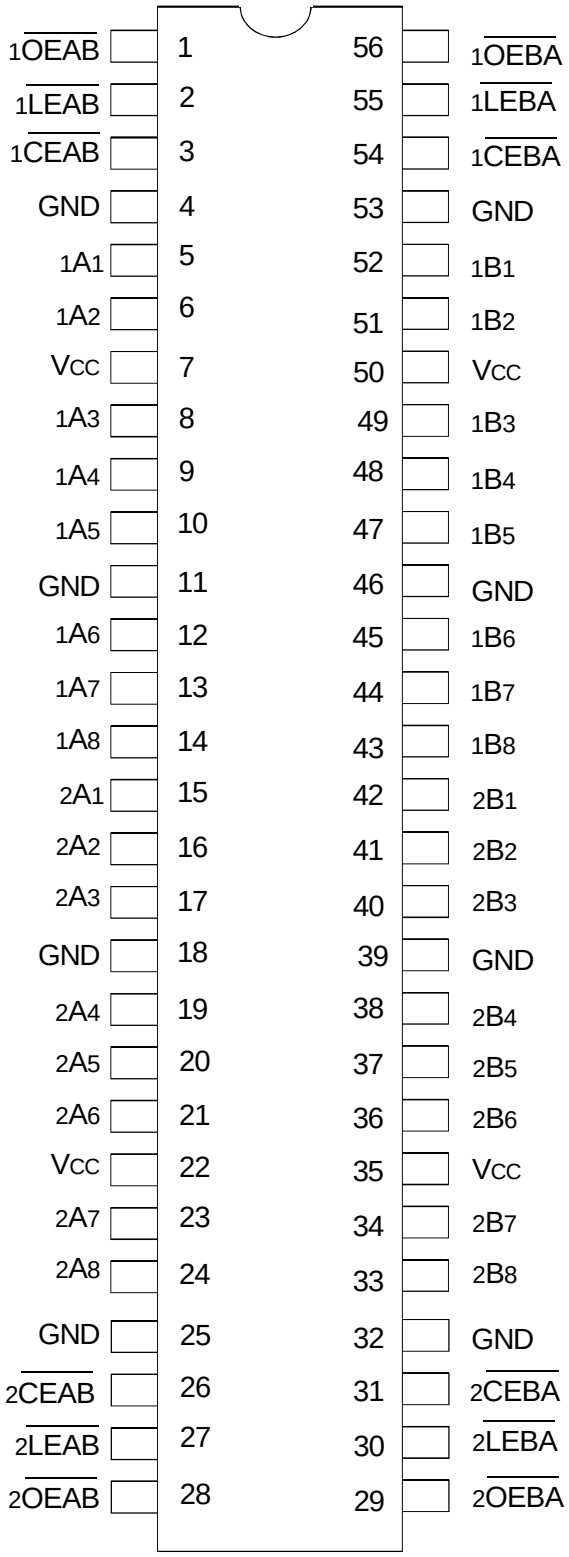
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCHR16543A has "bus-hold" which retains the input's last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SSOP/ TSSOP/ TVSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +6.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –50 to +50 | mA |
| $I_{IK}$<br>$I_{OK}$ | Continuous Clamp Current,<br>$V_I < 0$ or $V_O < 0$ | –50 | mA |
| $I_{CC}$<br>$I_{SS}$ | Continuous Current through each<br>$V_{CC}$ or GND | ±100 | mA |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 6.5 | 8 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 6.5 | 8 | pF |

**NOTE:**
1. As applicable to the device type.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| x$\overline{OE}$AB | A-to-B Output Enable Input (Active LOW) |
| x$\overline{OE}$BA | B-to-A Output Enable Input (Active LOW) |
| x$\overline{CE}$AB | A-to-B Enable Input (Active LOW) |
| x$\overline{CE}$BA | B-to-A Enable Input (Active LOW) |
| x$\overline{LE}$AB | A-to-B Latch Enable Input (Active LOW) |
| x$\overline{LE}$BA | B-to-A Latch Enable Input (Active LOW) |
| xAx | A-to-B Data Inputs or B-to-A 3-State Outputs(1) |
| xBx | B-to-A Data Inputs or A-to-B 3-State Outputs(1) |

**NOTE:**
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH 8-BIT SECTION)(1,2)

| Inputs | | | | Output Buffers |
|---|---|---|---|---|
| x$\overline{CE}$AB | x$\overline{LE}$AB | x$\overline{OE}$AB | xAx | xBx |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | B(3) |
| L | L | L | L | L |
| L | L | L | H | H |

**NOTES:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
3. Before $\overline{LEAB}$ LOW-to-HIGH transition.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A$ = –40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$<br>$I_{IL}$ | Input Leakage Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 5.5V | — | — | ±5 | µA |
| $I_{OZH}$<br>$I_{OZL}$ | High Impedance Output Current (3-State Output pins) | $V_{CC}$ = 3.6V | $V_O$ = 0 to 5.5V | — | — | ±10 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$ 5.5V | | — | — | ±50 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $V_{IN}$ = GND or $V_{CC}$ | — | — | 10 | µA |
| | | | 3.6 ≤ $V_{IN}$ ≤ 5.5V(2) | — | — | 10 | |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | | — | — | 500 | µA |

**NOTES:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

| Symbol | Parameter(1) | Test Conditions | | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3V | $V_I$ = 2V | –75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | — | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | — | — | — | |
| $I_{BHHO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ±500 | µA |
| $I_{BHLO}$ | | | | | | | |

**NOTES:**
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 4mA | 1.9 | — | |
| | | | $I_{OH}$ = – 6mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | $I_{OH}$ = – 4mA | 2.2 | — | |
| | | | $I_{OH}$ = – 8mA | 2 | — | |
| | | $V_{CC}$ = 3V | $I_{OH}$ = – 6mA | 2.4 | — | |
| | | | $I_{OH}$ = – 12mA | 2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 4mA | — | 0.4 | |
| | | | $I_{OL}$ = 6mA | — | 0.55 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 4mA | — | 0.4 | |
| | | | $I_{OL}$ = 8mA | — | 0.6 | |
| | | $V_{CC}$ = 3V | $I_{OL}$ = 6mA | — | 0.55 | |
| | | | $I_{OL}$ = 12mA | — | 0.8 | |

**NOTE:**
1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to + 85°C.

## OPERATING CHARACTERISTICS, $V_{CC}$ = 3.3V ± 0.3V, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance per Transceiver Outputs enabled | $C_L$ = 0pF, f = 10Mhz | | pF |
| $C_{PD}$ | Power Dissipation Capacitance per Transceiver Outputs disabled | | | |

## SWITCHING CHARACTERISTICS(1)

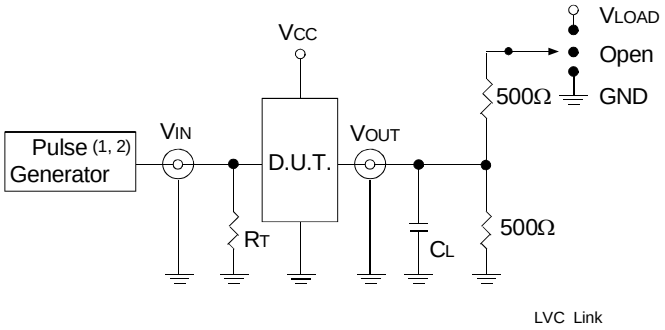
| Symbol | Parameter | Vcc = 2.7V | | Vcc = 3.3V ± 0.3V | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>xAx to xBx or xBx to xAx | 1.5 | 7 | 1.5 | 6 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>x$\overline{LEBA}$ to xAx, x$\overline{LEAB}$ to xBx | 1.5 | 8 | 1.5 | 7 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx | 1.5 | 9 | 1.5 | 8 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx | 1.5 | 9 | 1.5 | 8 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx | 1.5 | 7.5 | 1.5 | 6.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx | 1.5 | 7.5 | 1.5 | 6.5 | ns |
| $t_{SU}$ | Set-up Time, data before $\overline{CE}\uparrow$ | 2 | — | 2 | — | ns |
| $t_{SU}$ | Set-up Time, data before $\overline{LE}\uparrow$, $\overline{CE}$ LOW | 2 | — | 2 | — | ns |
| $t_H$ | Hold Time, data after $\overline{CE}\uparrow$ | 2 | — | 2 | — | ns |
| $t_H$ | Hold Time, data after $\overline{LE}\uparrow$, $\overline{CE}$ LOW | 2 | — | 2 | — | ns |
| $t_W$ | Pulse Duration, x$\overline{LEBA}$ or x$\overline{LEAB}$, x$\overline{CEBA}$ or x$\overline{CEAB}$ LOW | 5 | — | 5 | — | ns |
| $t_{SK(o)}$ | Output Skew(2) | — | — | — | 500 | ps |

**NOTES:**
1. See TEST CIRCUITS AND WAVEFORMS. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$=3.3V±0.3V | $V_{CC}^{(1)}$=2.7V | $V_{CC}^{(2)}$=2.5V±0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |




***Test Circuit for All Outputs***

**DEFINITIONS:**

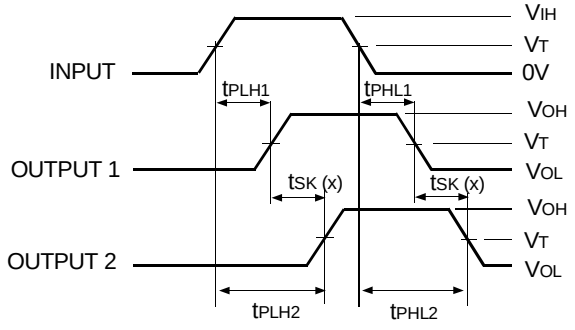
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

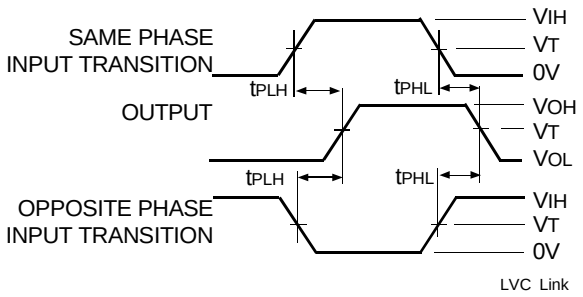
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other Tests | Open |



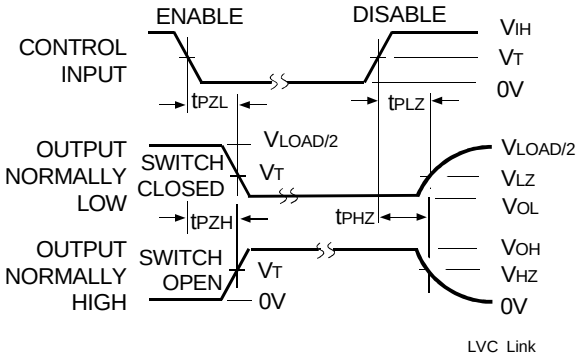

***Output Skew - $t_{SK}(x)$***

**NOTES:**

1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.



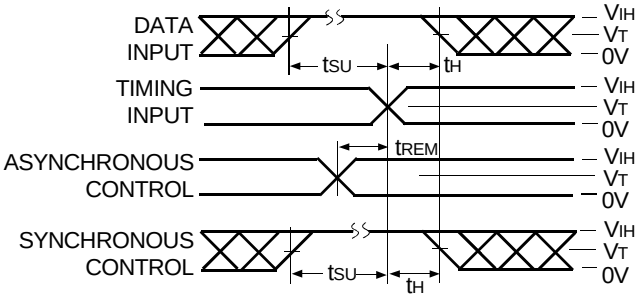

***Propagation Delay***



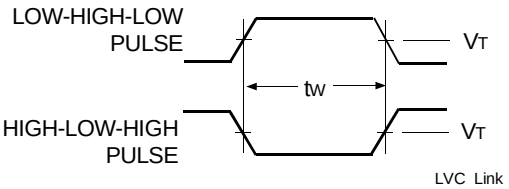

***Enable and Disable Times***

**NOTE:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

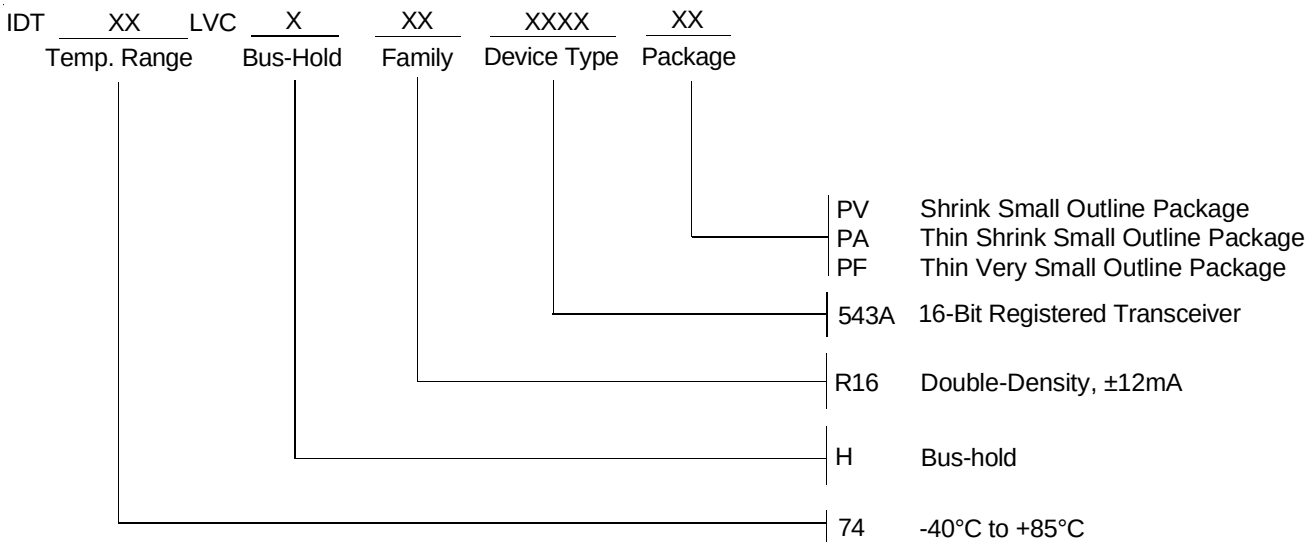



***Set-up, Hold, and Release Times***




***Pulse Width***

## ORDERING INFORMATION

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