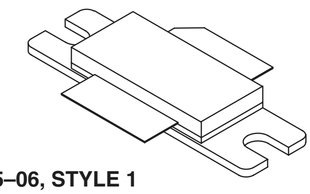
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18060B
MRF18060BR3
MRF18060BLSR3
MRF18060BSR3

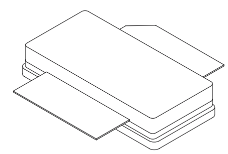
Designed for PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications. Specified for GSM1930 – 1990 MHz.

- GSM Performance, Full Frequency Band (1930 – 1990 MHz)
  Power Gain — 13 dB (Typ) @ 60 Watts CW
  Efficiency — 45% (Typ) @ 60 Watts CW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts CW Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40µ″ Nominal.

1.90 – 1.99 GHz, 60 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465–06, STYLE 1
NI–780
MRF18060B



CASE 465A–06, STYLE 1
NI–780S
MRF18060BLSR3, MRF18060BSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

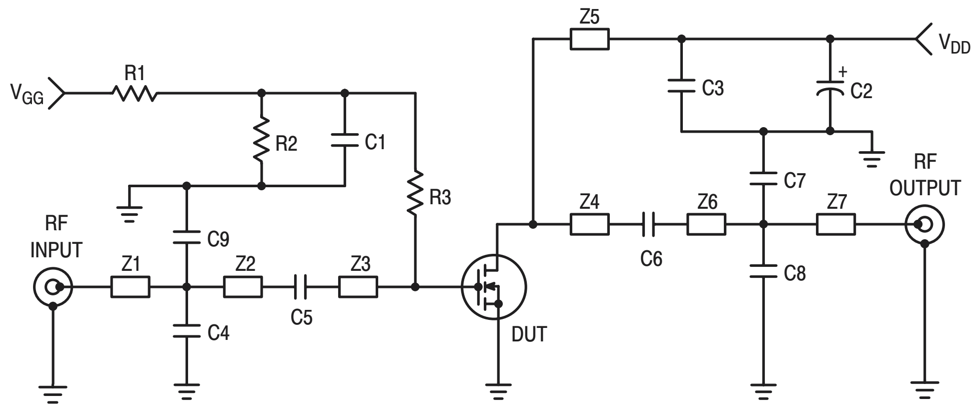
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	160	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	740	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Common–Source Amplifier Power Gain @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	G_{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (2) (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.



C1, C3	10 pF, 100B Chip Capacitors	Z1	0.60″ x 0.09″ Microstrip
C2	10 μF, 35 V Electrolytic Tantalum Capacitor	Z2	1.00″ x 0.09″ Microstrip
C4, C8	1.2 pF, 100B Chip Capacitors	Z3	0.51″ x 0.94″ Microstrip
C5	1.0 pF, 100B Chip Capacitor	Z4	0.59″ x 0.98″ Microstrip
C6	2.2 pF, 100B Chip Capacitor	Z5	0.79″ x 0.09″ Microstrip
C7, C9	0.3 pF, 100B Chip Capacitors	Z6	1.38″ x 0.09″ Microstrip
R1, R2	10 kΩ Chip Resistors (0805)	Z7	0.79″ x 0.09″ Microstrip
R3	1.0 kΩ Chip Resistor (0805)	PCB	Teflon® Glass

Figure 1. 1930 – 1990 MHz Test Fixture Schematic

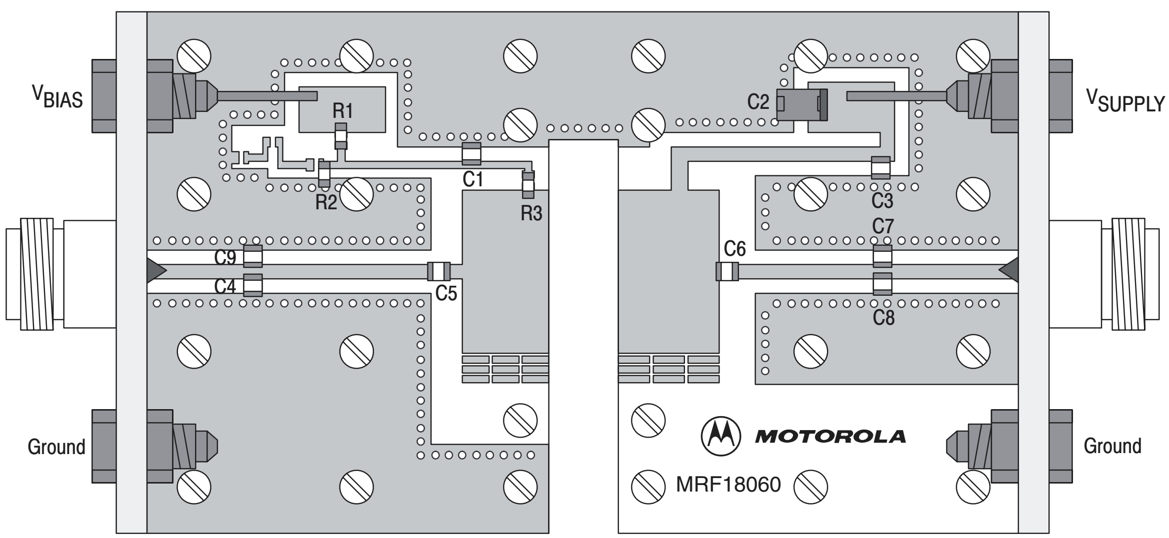
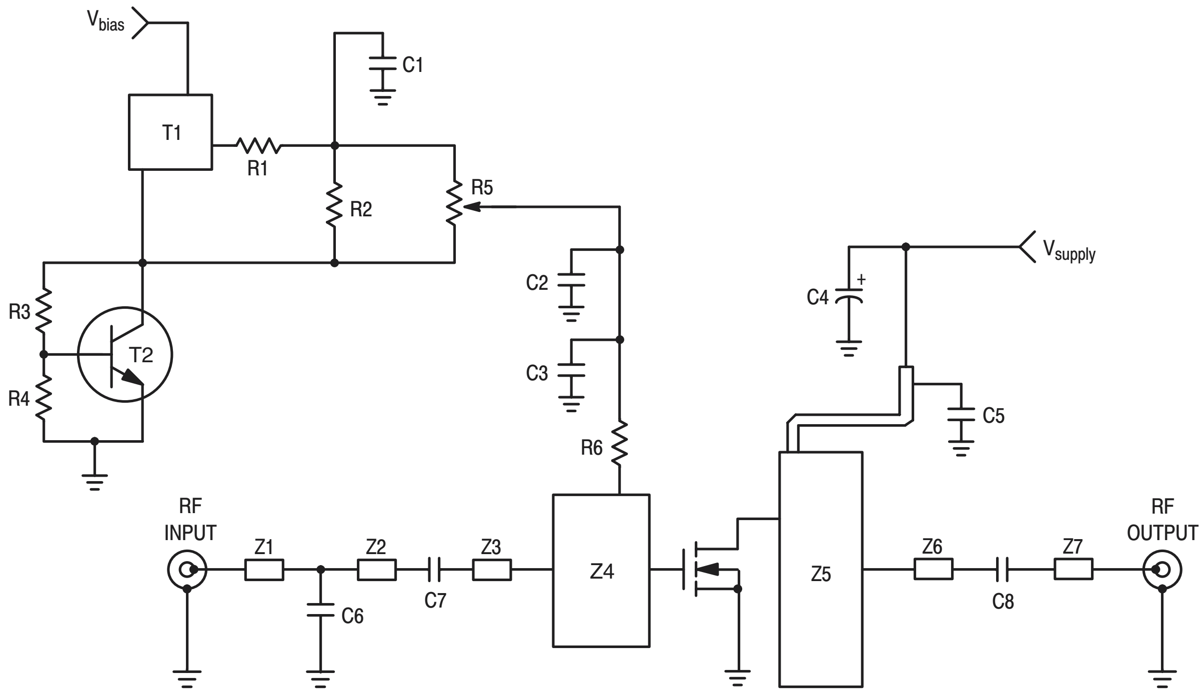


Figure 2. 1930 – 1990 MHz Test Fixture Component Layout



C1	1 μF Chip Capacitor (0805)	T1	LP2951 Micro–8 Voltage Regulator
C2	100 nF Chip Capacitor (0805)	T2	BC847 SOT–23 NPN Transistor
C3, C5, C8	10 pF Chip Capacitors, ACCU–P (0805)	Z1	0.159″ x 0.055″ Microstrip
C4	10 μF, 35 V Tantalum Electrolytic Capacitor	Z2	0.982″ x 0.055″ Microstrip
C6	1.8 pF Chip Capacitor, ACCU–P (0805)	Z3	0.087″ x 0.055″ Microstrip
C7	1 pF Chip Capacitor, ACCU–P (0805)	Z4	0.512″ x 0.787″ Microstrip
R1	10 Ω Chip Resistor (0805)	Z5	0.433″ x 1.220″ Microstrip
R2, R6	1 kΩ Chip Resistors (0805)	Z6	1.039″ x 0.118″ Microstrip
R3	1.2 kΩ Chip Resistor (0805)	Z7	0.268″ x 0.055″ Microstrip
R4	2.2 kΩ Chip Resistor (0805)	Substrate = 0.5 mm Teflon® Glass, ε_r = 2.55	
R5	5 kΩ, SMD Potentiometer		

Figure 3. 1800 – 2000 MHz Demo Board Schematic

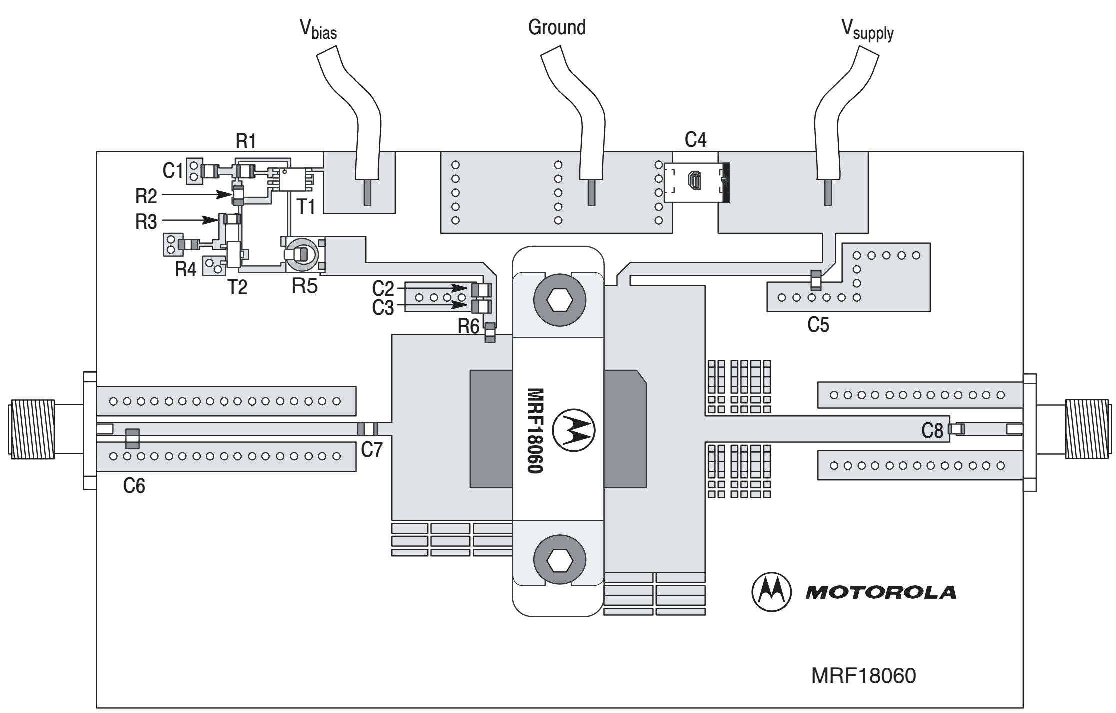


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

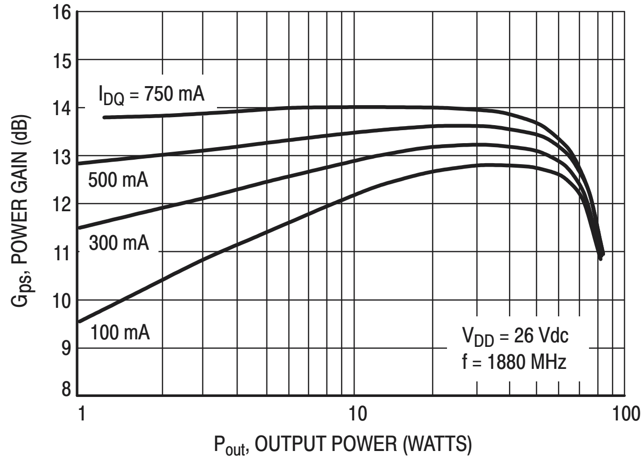


Figure 5. Power Gain versus Output Power

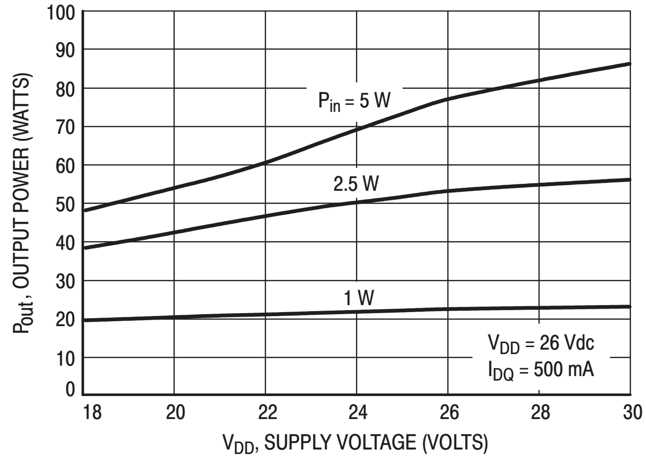


Figure 6. Output Power versus Supply Voltage

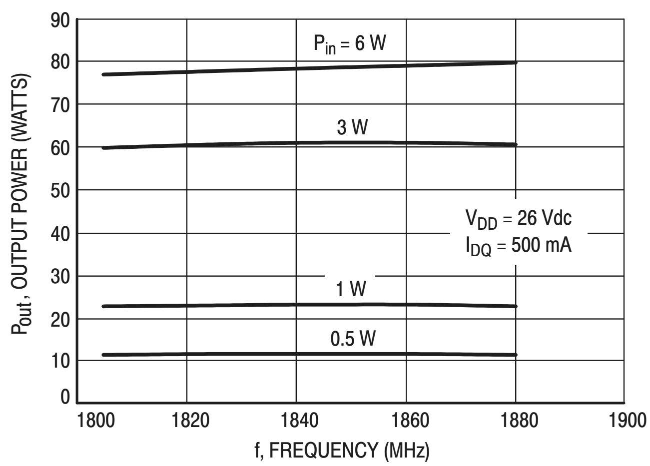


Figure 7. Output Power versus Frequency

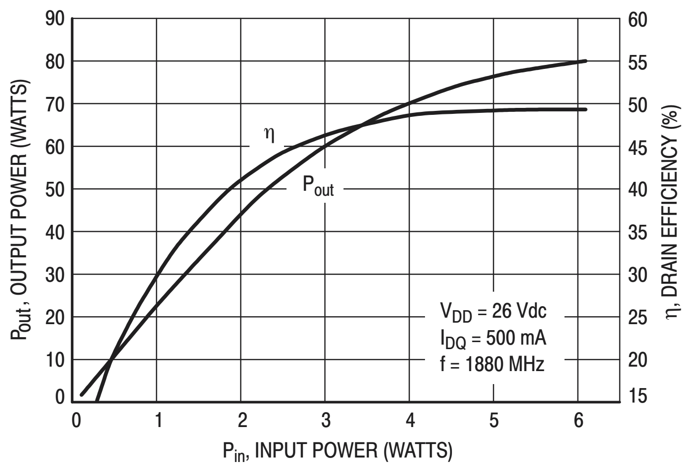


Figure 8. Output Power and Efficiency versus Input Power

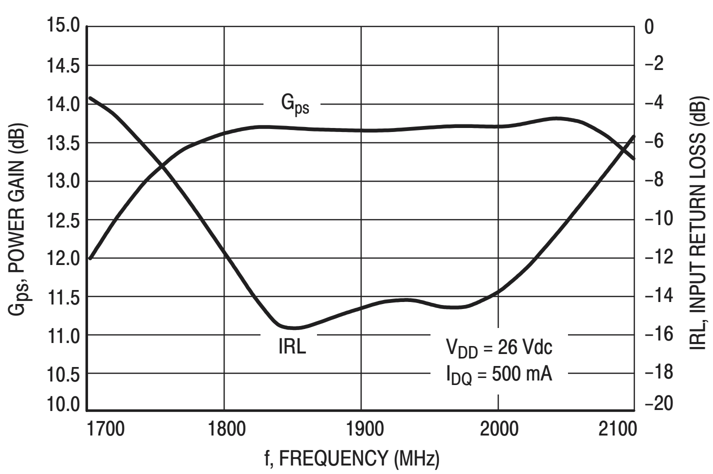
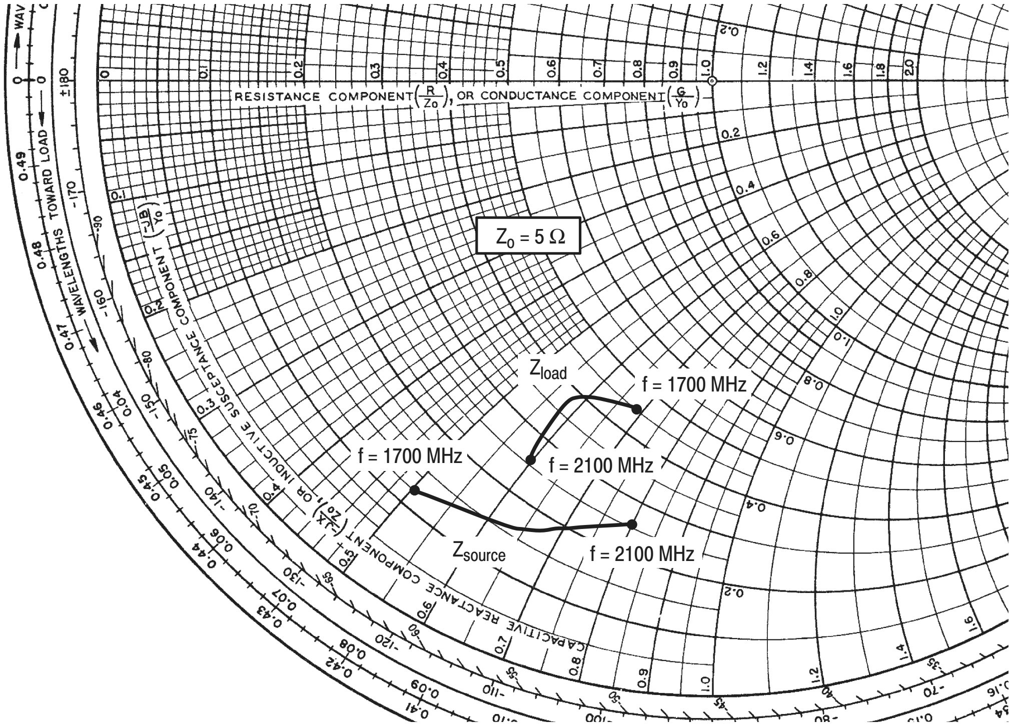


Figure 9. Wideband Gain and IRL (at Small Signal)



V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
1700	0.60 – j2.53	2.27 – j3.44
1800	0.80 – j3.20	2.05 – j3.05
1900	0.92 – j3.42	1.90 – j2.90
2000	1.07 – j3.59	1.64 – j2.88
2100	1.31 – j4.00	1.29 – j2.99

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

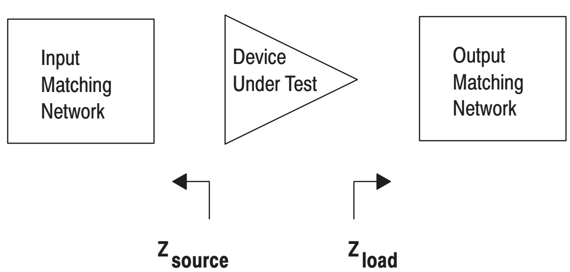
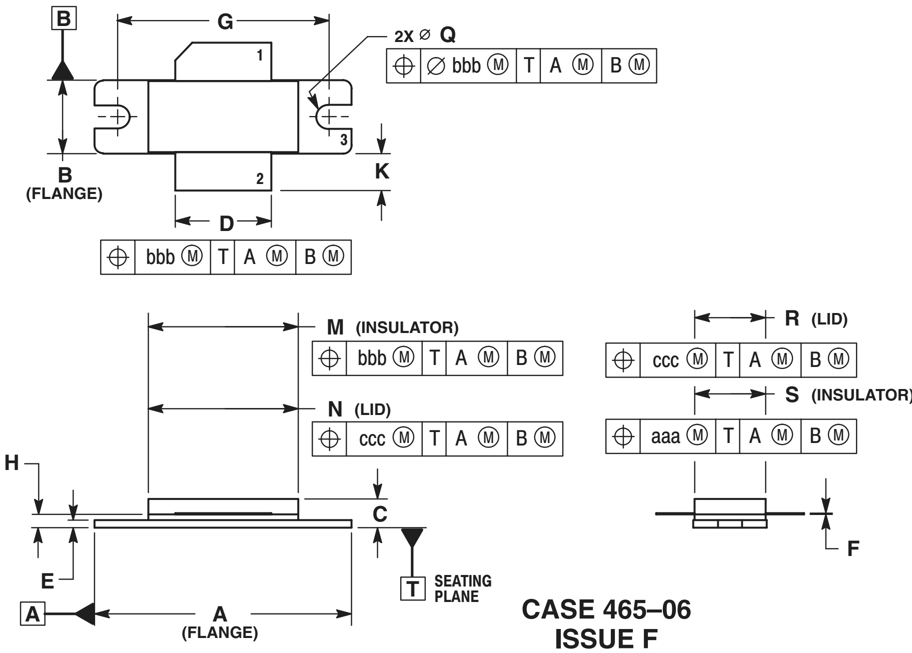


Figure 10. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS

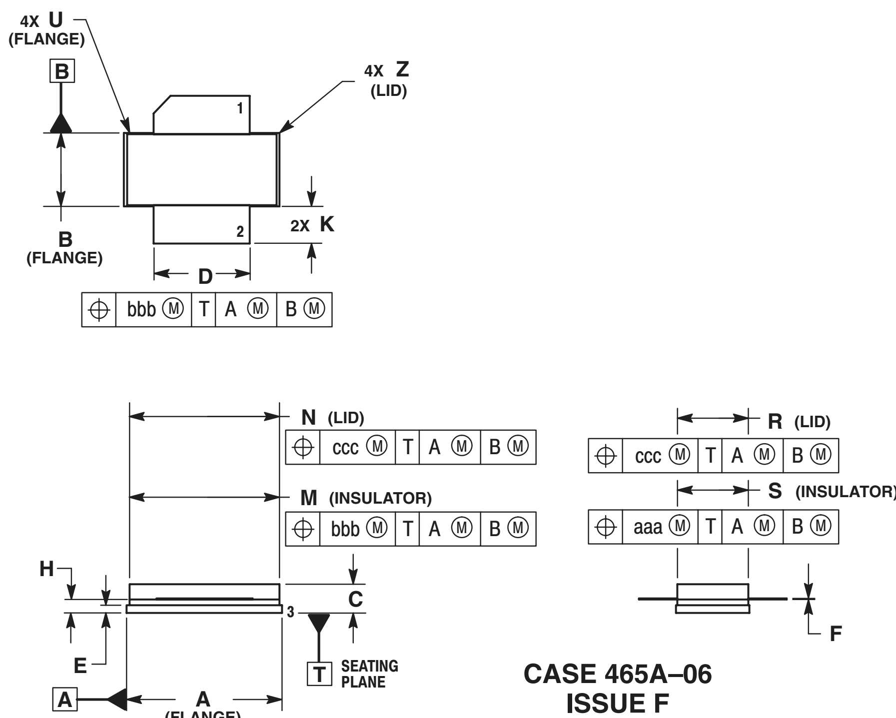


CASE 465–06
ISSUE F
NI–780
MRF18060B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	Ø.118	Ø.138	Ø3.00	Ø3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE



CASE 465A–06
ISSUE F
NI–780S
MRF18060BLSR3, MRF18060BSR3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

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