OKI Semiconductor

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MSM63182

4-Bit Microcontroller with Built-in 512-Dot Matrix LCD Drivers, Operating at 0.9 V (Min.)

GENERAL DESCRIPTION

The MSM63182 is a CMOS 4-bit microcontroller with built-in 512-dot matrix LCD drivers and operates at 0.9 V (min.). The MSM63182 is suitable for applications such as games, toys, watches, etc. which are provided with an LCD display.
The MSM63182 is an M6318x series mask ROM-version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.
The MSM63P180 is the one-time-programmable ROM version of MSM63188, having one-time PROM (OTP) as internal program memory.
The MSM63P180 is used to evaluate the software development.

FEATURES

- Rich instruction set
  439 instructions
  Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, branch, conditional branch, call/return, control.

- Rich selection of addressing modes
  Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
  Data memory bank internal direct addressing mode.

- Processing speed
  Two clocks per machine cycle, with most instructions executed in one machine cycle.
  Minimum instruction execution time : 61 µs (@ 32.768 kHz system clock)
  1 µs (@ 2 MHz system clock)

- Clock generation circuit
  Low-speed clock : 32.768 kHz crystal oscillator
  High-speed clock : 2 MHz (Max.) RC or ceramic oscillator select

- Program memory space
  4K words
  Basic instruction length is 16 bits/1 word

- Data memory space
  384 nibbles

- External data memory space
  64 Kbytes (expandable by using an I/O port)

- Stack level
  - Call stack level : 8 levels
  - Register stack level : 16 levels

- I/O ports
  - Input ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
  - Output ports: Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
  - Input-output ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
    Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
  - Can be interfaced with external peripherals that use a different power supply than this device uses.
  - Number of ports:
    - Input port : 2 ports × 4 bits
    - Output port : 4 ports × 4 bits
    - Input-output port : 3 ports × 4 bits

- Buzzer function
  - Buzzer output : 0.946 to 5.461 kHz (adjustable in 15 steps)
  - Buzzer output modes : Intermittent sound 1, 2; simple sound; continuous sound

- LCD driver
  - Number of segments : 512 Max. (32 SEG × 16 COM)
  - 1/1 to 1/16 duty
  - 1/4 or 1/5 bias (regulator built-in)
  - Selectable as all-on mode/all-off mode/power down mode/normal display mode
  - Adjustable contrast

- Reset function
  - Reset through RESET pin
  - Power-on reset
  - Reset by low-speed oscillation halt

- Battery check
  - Low-voltage supply check
  - Criterion voltage : Can be selected as 1.05 ±0.10 V, 1.30 ±0.15 V, 2.20 ±0.20 V or 2.80 ±0.30 V

- Power supply backup
  - Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

- Timers and counter
  Watchdog timer × 1
  Overflows in 2 sec.
  100 Hz timer × 1
  Measurable in steps of 1/100 sec.
  15-bit time base counter × 1
  1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read

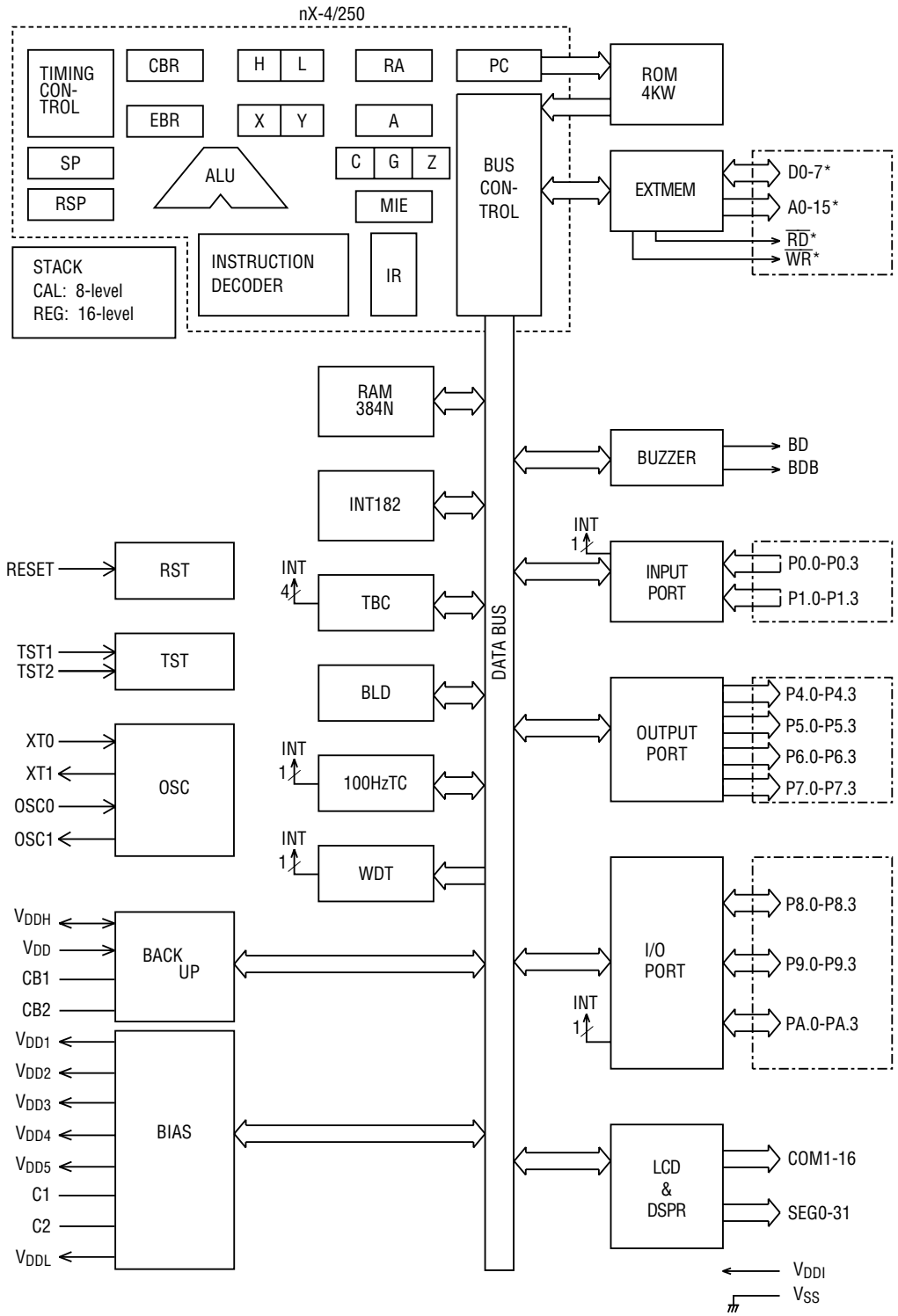
- Interrupt sources
  External interrupt : 2
  Internal interrupt : 6 (watchdog timer interrupt is a nonmaskable interrupt)

- Operating voltage
  When backup used : 0.9 to 2.7 V
  (Low-speed clock operating)
  1.2 to 2.7 V
  (Operating frequency: 300 to 500 kHz)
  1.5 to 2.7 V
  (Operating frequency: 200 kHz to 1 MHz)
  When backup not used : 1.8 to 5.5 V
  (Operating frequency: 300 to 500 kHz)
  2.2 to 5.5 V
  (Operating frequency: 300 kHz to 1 MHz)
  2.7 to 5.5 V
  (Operating frequency: 200 kHz to 2 MHz)

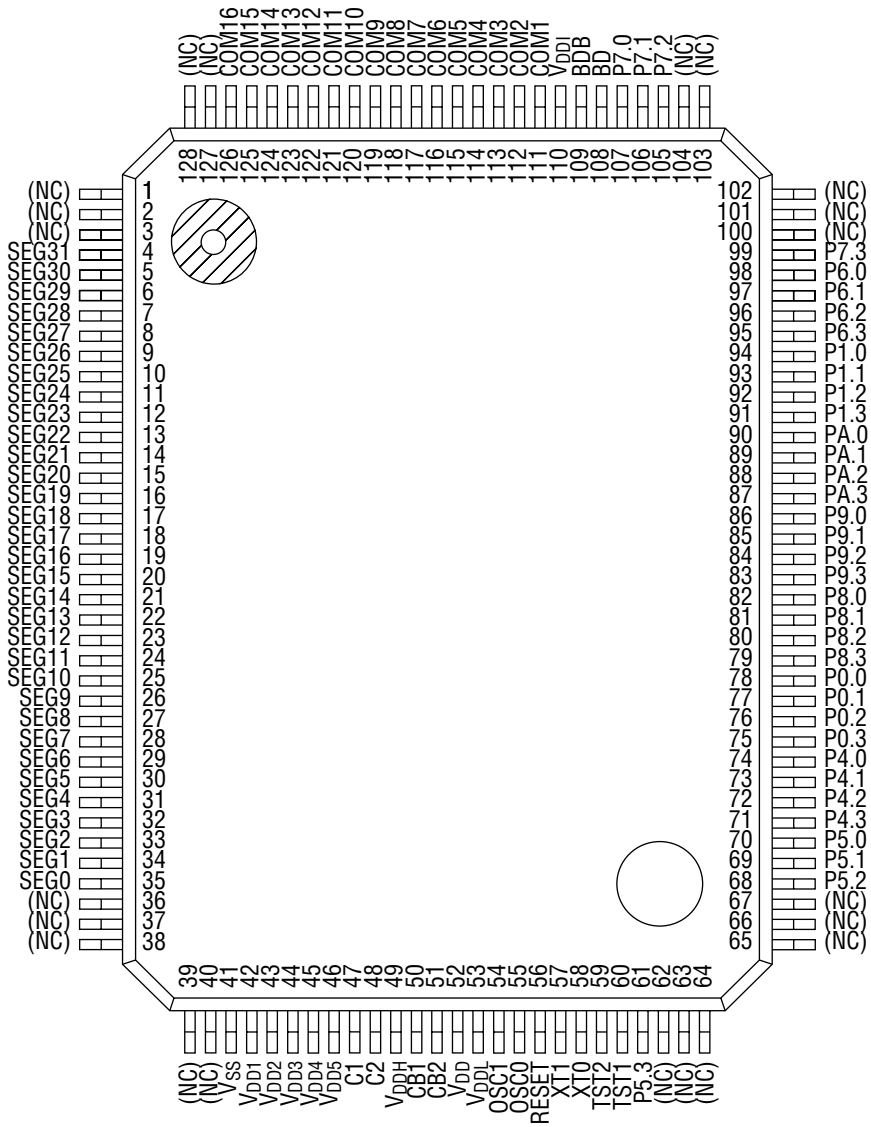
- Package:
  128-pin plastic QFP (QFP128-P-1420-0.50-K) : (Product name: MSM63182-xxxGS-K)
  Chip : (Product name: MSM63182-xxx)
  xxx indicates a code number.

BLOCK DIAGRAM

An asterisk (*) indicates the port secondary function. ⬚ indicates that the power is supplied to the circuits corresponding to the signal names inside ⬚ from V_{DDI} (power supply for interface).



PIN CONFIGURATION (TOP VIEW)

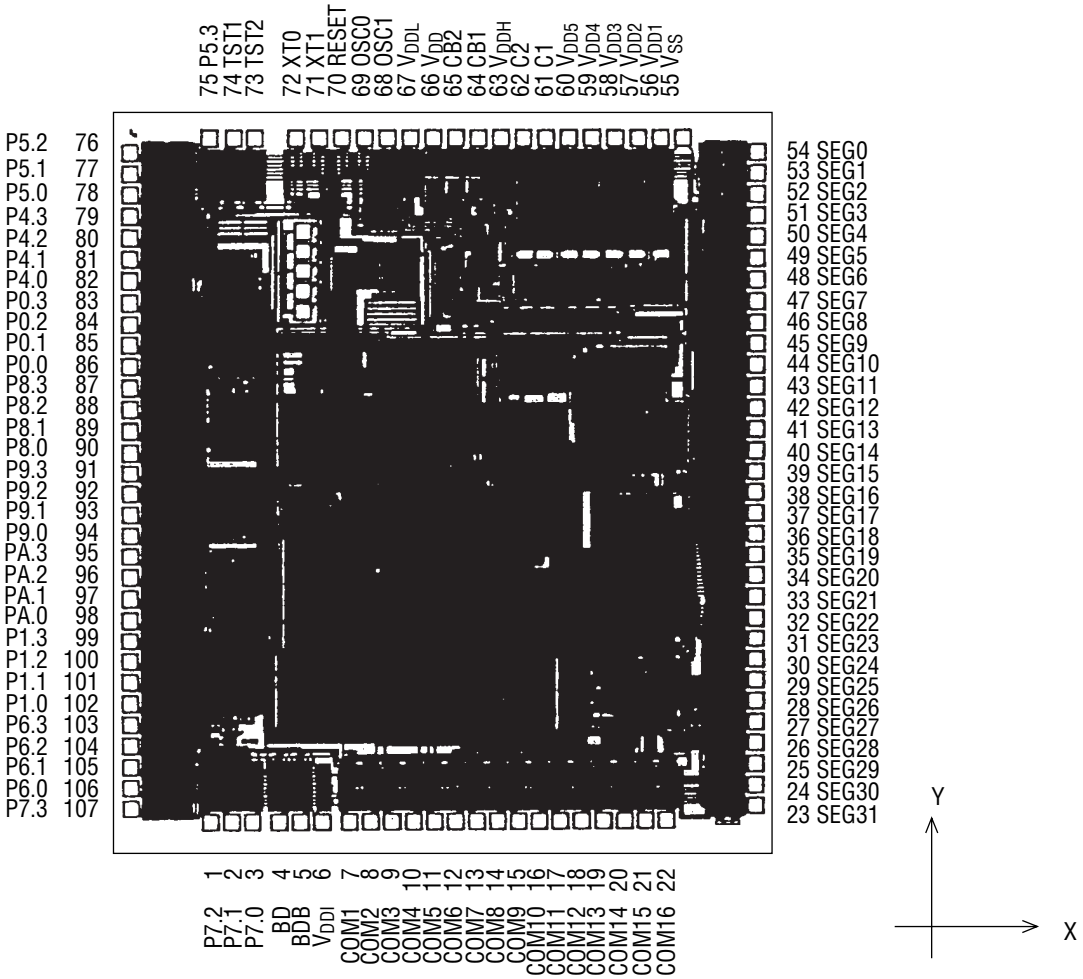


128-Pin Plastic QFP

Note: Pins marked as (NC) are no-connection pins which are left open.

PAD CONFIGURATION

Pad Layout



Chip Size	: 4.44 mm × 4.92 mm
Chip Thickness	: 350 µm (typ.)
Coordinate Origin	: Chip center
Pad Hole Size	: 100 µm × 100 µm
Pad Size	: 110 µm × 110 µm
Minimum Pad Pitch	: 140 µm

Note: The chip substrate voltage is V_{SS}.

Pad Coordinates

Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)
1	P7.2	–1547	–2265	37	SEG17	2075	–210	73	TST2	–1247	2265
2	P7.1	–1407	–2265	38	SEG16	2075	–70	74	TST1	–1387	2265
3	P7.0	–1267	–2265	39	SEG15	2075	70	75	P5.3	–1548	2265
4	BD	–1090	–2265	40	SEG14	2075	210	76	P5.2	–2075	2170
5	BDB	–950	–2265	41	SEG13	2075	350	77	P5.1	–2075	2030
6	V_{DDI}	–810	–2265	42	SEG12	2075	490	78	P5.0	–2075	1890
7	COM1	–630	–2265	43	SEG11	2075	630	79	P4.3	–2075	1750
8	COM2	–490	–2265	44	SEG10	2075	770	80	P4.2	–2075	1610
9	COM3	–350	–2265	45	SEG9	2075	910	81	P4.1	–2075	1470
10	COM4	–210	–2265	46	SEG8	2075	1050	82	P4.0	–2075	1330
11	COM5	–70	–2265	47	SEG7	2075	1190	83	P0.3	–2075	1190
12	COM6	70	–2265	48	SEG6	2075	1330	84	P0.2	–2075	1050
13	COM7	210	–2265	49	SEG5	2075	1470	85	P0.1	–2075	910
14	COM8	350	–2265	50	SEG4	2075	1610	86	P0.0	–2075	770
15	COM9	490	–2265	51	SEG3	2075	1750	87	P8.3	–2075	630
16	COM10	630	–2265	52	SEG2	2075	1890	88	P8.2	–2075	490
17	COM11	770	–2265	53	SEG1	2075	2030	89	P8.1	–2075	350
18	COM12	910	–2265	54	SEG0	2075	2170	90	P8.0	–2075	210
19	COM13	1050	–2265	55	V_{SS}	1575	2265	91	P9.3	–2075	70
20	COM14	1190	–2265	56	V_{DD1}	1425	2265	92	P9.2	–2075	–70
21	COM15	1330	–2265	57	V_{DD2}	1275	2265	93	P9.1	–2075	–210
22	COM16	1470	–2265	58	V_{DD3}	1125	2265	94	P9.0	–2075	–350
23	SEG31	2075	–2170	59	V_{DD4}	975	2265	95	PA.3	–2075	–490
24	SEG30	2075	–2030	60	V_{DD5}	825	2265	96	PA.2	–2075	–630
25	SEG29	2075	–1890	61	C1	675	2265	97	PA.1	–2075	–770
26	SEG28	2075	–1750	62	C2	525	2265	98	PA.0	–2075	–910
27	SEG27	2075	–1610	63	V_{DDH}	375	2265	99	P1.3	–2075	–1050
28	SEG26	2075	–1470	64	CB1	225	2265	100	P1.2	–2075	–1190
29	SEG25	2075	–1330	65	CB2	75	2265	101	P1.1	–2075	–1330
30	SEG24	2075	–1190	66	V_{DD}	–75	2265	102	P1.0	–2075	–1470
31	SEG23	2075	–1050	67	V_{DDL}	–225	2265	103	P6.3	–2075	–1610
32	SEG22	2075	–910	68	OSC1	–375	2265	104	P6.2	–2075	–1750
33	SEG21	2075	–770	69	OSC0	–525	2265	105	P6.1	–2075	–1890
34	SEG20	2075	–630	70	RESET	–675	2265	106	P6.0	–2075	–2030
35	SEG19	2075	–490	71	XT1	–825	2265	107	P7.3	–2075	–2170
36	SEG18	2075	–350	72	XT0	–975	2265				

PIN DESCRIPTIONS

The basic functions of each pin of the MSM63182 are described in Table 1.
A symbol with a slash (/) denotes a pin that has a secondary function.
Refer to Table 2 for secondary functions.
For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

Table 1 Pin Descriptions (Basic Functions)

Function	Symbol	Pin	Type	Description
Power Supply	V_{DD}	52	—	Positive power supply
	V_{SS}	41	—	Negative power supply
	V_{DD1}	42	—	Power supply pins for LCD bias (internally generated). Capacitors (0.1 μF) should be connected between these pins and V_{SS}.
	V_{DD2}	43		
	V_{DD3}	44		
	V_{DD4}	45		
	V_{DD5}	46		
	C1	47	—	Capacitor connection pins for LCD bias generation. A capacitor (0.1 μF) should be connected between C1 and C2.
	C2	48	—	
	V_{DDI}	110	—	Positive power supply pin for external interface (power supply for input, output, and input-output ports)
	V_{DDL}	53	—	Positive power supply pin for internal logic (internally generated). A capacitor (0.1 μF) should be connected between this pin and V_{SS}.
	V_{DDH}	49	—	Voltage multiplier pin for power supply backup (internally generated). A capacitor (1.0 μF) should be connected between this pin and V_{SS}.
	CB1	50	—	Pins to connect a capacitor for voltage multiplier. A capacitor (1.0 μF) should be connected between CB1 and CB2.
	CB2	51	—	
Oscillation	XT0	58	I	Low-speed clock oscillation pins. A 32.768 kHz crystal should be connected between XT0 and XT1, and C_G (5 to 25 pF) should be connected between XT0 and V_{SS}.
	XT1	57	O	
	OSC0	55	I	High-speed clock oscillation pins. A ceramic resonator and capacitors (C_{L0}, C_{L1}) or external oscillation resistor (R_{OS}) should be connected to these pins.
	OSC1	54	O	
Test	TST1	60	I	Input pins for testing. A pull-down resistor is internally connected to these pins. The user cannot use these pins.
	TST2	59	I	
Reset	RESET	56	I	Reset input pin. Setting this pin to "H" level puts this device into a reset state. Then, setting this pin to "L" level starts executing an instruction from address 0000H. A pull-down resistor is internally connected to this pin.
Buzzer	BD	108	O	Buzzer output pin (non-inverted output)
	BDB	109	O	Buzzer output pin (inverted output)

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin	Type	Description
Port	P0.0/INT5	78	I	4-bit input ports. Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P0.1/INT5	77		
	P0.2/INT5	76		
	P0.3/INT5	75		
	P1.0/INT5	94	I	
	P1.1/INT5	93		
	P1.2/INT5	92		
	P1.3/INT5	91		
	P4.0/A0	74	O	4-bit output ports. P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P4.1/A1	73		
	P4.2/A2	72		
	P4.3/A3	71		
	P5.0/A4	70	O	
	P5.1/A5	69		
	P5.2/A6	68		
	P5.3/A7	61		
	P6.0/A8	98	O	
	P6.1/A9	97		
	P6.2/A10	96		
	P6.3/A11	95		
	P7.0/A12	107	O	
	P7.1/A13	106		
	P7.2/A14	105		
	P7.3/A15	99		
	P8.0/$\overline{RD}$	82	I/O	4-bit input-output ports. In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit. In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P8.1/$\overline{WR}$	81		
	P8.2	80		
	P8.3/INT4	79		
	P9.0/D0	86	I/O	
	P9.1/D1	85		
	P9.2/D2	84		
	P9.3/D3	83		
	PA.0/D4	90	I/O	
	PA.1/D5	89		
	PA.2/D6	88		
	PA.3/D7	87		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin	Type	Description
LCD	COM1	111	O	LCD common signal output pins
	COM2	112		
	COM3	113		
	COM4	114		
	COM5	115		
	COM6	116		
	COM7	117		
	COM8	118		
	COM9	119		
	COM10	120		
	COM11	121		
	COM12	122		
	COM13	123		
	COM14	124		
	COM15	125		
	COM16	126		
	SEG0	35	O	LCD segment signal output pins
	SEG1	34		
	SEG2	33		
	SEG3	32		
	SEG4	31		
	SEG5	30		
	SEG6	29		
	SEG7	28		
	SEG8	27		
	SEG9	26		
	SEG10	25		
	SEG11	24		
	SEG12	23		
	SEG13	22		
	SEG14	21		
	SEG15	20		
	SEG16	19		
	SEG17	18		
	SEG18	17		
	SEG19	16		
	SEG20	15		
	SEG21	14		
	SEG22	13		
	SEG23	12		
	SEG24	11		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin	Type	Description
LCD	SEG25	10	O	LCD segment signal output pins
	SEG26	9		
	SEG27	8		
	SEG28	7		
	SEG29	6		
	SEG30	5		
	SEG31	4		

Table 2 shows the secondary functions of each pin of the MSM63182.

Table 2 Pin Descriptions (Secondary Functions)

Function	Symbol	Pin	Type	Description
External Interrupt	P8.3/INT4	79	I	External 4 interrupt input pin. The change of input signal level causes an interrupt to occur.
	P0.0/INT5	78	I	External 5 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port 0 Interrupt Enable register (P0IE) and Port 1 Interrupt Enable register (P1IE) enable or disable an interrupt for each bit.
	P0.1/INT5	77		
	P0.2/INT5	76		
	P0.3/INT5	75		
	P1.0/INT5	94		
	P1.1/INT5	93		
	P1.2/INT5	92		
	P1.3/INT5	91		

Table 2 Pin Descriptions (Secondary Functions) (continued)

Function	Symbol	Pin	Type	Description
External Memory	P4.0/A0	74	O	Address output bus for external memory
	P4.1/A1	73		
	P4.2/A2	72		
	P4.3/A3	71		
	P5.0/A4	70		
	P5.1/A5	69		
	P5.2/A6	68		
	P5.3/A7	61		
	P6.0/A8	98		
	P6.1/A9	97		
	P6.2/A10	96		
	P6.3/A11	95		
	P7.0/A12	107		
	P7.1/A13	106		
	P7.2/A14	105		
	P7.3/A15	99		
	P9.0/D0	86	I/O	Data bus for external memory
	P9.1/D1	85		
	P9.2/D2	84		
	P9.3/D3	83		
	PA.0/D4	90		
	PA.1/D5	89		
	PA.2/D6	88		
	PA.3/D7	87		
	P8.0/$\overline{RD}$	82	O	Read signal output pin for external memory (negative logic)
	P8.1/$\overline{WR}$	81	O	Write signal output pin for external memory (negative logic)

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{DD1}	Ta = 25°C	–0.3 to +1.6	V
Power Supply Voltage 2	V_{DD2}	Ta = 25°C	–0.3 to +2.9	V
Power Supply Voltage 3	V_{DD3}	Ta = 25°C	–0.3 to +4.2	V
Power Supply Voltage 4	V_{DD4}	Ta = 25°C	–0.3 to +5.5	V
Power Supply Voltage 5	V_{DD5}	Ta = 25°C	–0.3 to +6.8	V
Power Supply Voltage 6	V_{DD}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 7	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 8	V_{DDH}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 9	V_{DDL}	Ta = 25°C	–0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} Input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} Input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD1} Output, Ta = 25°C	–0.3 to V_{DD1} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DD2} Output, Ta = 25°C	–0.3 to V_{DD2} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DD3} Output, Ta = 25°C	–0.3 to V_{DD3} + 0.3	V
Output Voltage 4	V_{OUT4}	V_{DD4} Output, Ta = 25°C	–0.3 to V_{DD4} + 0.3	V
Output Voltage 5	V_{OUT5}	V_{DD5} Output, Ta = 25°C	–0.3 to V_{DD5} + 0.3	V
Output Voltage 6	V_{OUT6}	V_{DD} Output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output Voltage 7	V_{OUT7}	V_{DDI} Output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 8	V_{OUT8}	V_{DDH} Output, Ta = 25°C	–0.3 to V_{DDH} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

• When backup is used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	0.9 to 2.7	V
	V_{DDI}	—	0.9 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 1.2 to 2.7 V	300k to 500k	Hz
		V_{DD} = 1.5 to 2.7 V	200k to 1M	
External RC Oscillator Resistance	R_{OS}	V_{DD} = 1.2 to 2.7 V	100 to 300	kΩ
		V_{DD} = 1.5 to 2.7 V	50 to 300	

• When backup is not used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	1.8 to 5.5	V
	V_{DDI}	—	1.8 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 1.8 to 5.5 V	300k to 500k	Hz
		V_{DD} = 2.2 to 5.5 V	300k to 1M	
		V_{DD} = 2.7 to 5.5 V	200k to 2M	
External RC Oscillator Resistance	R_{OS}	V_{DD} = 1.8 to 5.5 V	100 to 300	kΩ
		V_{DD} = 2.2 to 5.5 V	50 to 300	
		V_{DD} = 2.7 to 5.5 V	30 to 300	

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD} = V_{DDI}$ = 0.9 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD2} Voltage	V_{DD2}	1/5 bias, 1/4 bias (Ta = 25°C)	1.7	1.8	1.9	V	
V_{DD2} Voltage Temperature Deviation	ΔV_{DD2}	—	—	–4	—	mV/°C	
V_{DD1} Voltage	V_{DD1}	1/5 bias, 1/4 bias	Typ.– 0.2	1/2 × V_{DD2}	Typ.+ 0.2	V	
V_{DD3} Voltage	V_{DD3}	1/5 bias	Typ.– 0.3	3/2 × V_{DD2}	Typ.+ 0.3	V	
		1/4 bias (connect V_{DD3} and V_{DD2})	Typ.– 0.2	V_{DD2}	Typ.+ 0.2		
V_{DD4} Voltage	V_{DD4}	1/5 bias	Typ.– 0.4	2 × V_{DD2}	Typ.+ 0.4	V	
		1/4 bias	Typ.– 0.3	3/2 × V_{DD2}	Typ.+ 0.3		
V_{DD5} Voltage	V_{DD5}	1/5 bias	Typ.– 0.5	5/2 × V_{DD2}	Typ.+ 0.5	V	
		1/4 bias	Typ.– 0.4	2 × V_{DD2}	Typ.+ 0.4		
V_{DDH} Voltage (Backup used)	V_{DDH}	High-speed clock oscillation stopped V_{DD} = 1.5 V	2.8	—	3.0	V	1
		High-speed clock oscillation (Ceramic oscillation, 1 MHz) V_{DD} = 1.5 V	2.0	—	2.7	V	
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillation stopped	1.0	1.5	2.0	V	
		High-speed clock oscillation (V_{DD} = 1.2 to 5.5 V)	1.2	—	5.5	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	1.0	—	—	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	Backup	0.9	—	—	V	
		Backup not used	1.7	—	—	V	
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External Crystal Oscillator Capacitance	C_G	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C_D	—	20	25	30	pF	
External Ceramic Oscillator Capacitance	$C_{L0, 1}$	CSA2.00MG (Murata MFG.-make) used V_{DD} = 3.0 V	—	30	—	pF	
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16	pF	
POR Voltage	V_{POR1}	V_{DD} = 1.5 V	0.0	—	0.4	V	
		V_{DD} = 3.0 V	0.0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD} = 1.5 V	1.2	—	1.5	V	
		V_{DD} = 3.0 V	2.0	—	3.0	V	

Notes: 1. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.
2. "POR" denotes Power On Reset.
3. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}.
4. "V_{POR2}" indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD}.

DC Characteristics (continued)

• When backup is used

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	—	7.0	35	µA	1
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	—	5.5	30	µA	
Supply Current 3	I_{DD3}	CPU is in operating state. (High-speed clock oscillation stopped)	—	24	40	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation, R_{OS} = 51 kΩ)	—	600	800	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)	—	700	900	µA	

• When backup is not used

(V_{DD} = V_{DDI} = 3.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	—	3.0	20	µA	1
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	—	2.0	18	µA	
Supply Current 3	I_{DD3}	CPU is in operating state. (High-speed clock oscillation stopped)	—	11	20	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation, R_{OS} = 51 kΩ)	—	450	600	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)	—	850	1000	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{SS} = 0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) (PA.0 to PA.3)	I_{OH1}	V_{OH1} = V_{DDI} – 0.5 V	V_{DDI} = 1.5 V	–2.0	–1.2	–0.2	mA	
			V_{DDI} = 3.0 V	–5.0	–3.0	–1.0	mA	
			V_{DDI} = 5.0 V	–8.0	–4.0	–1.5	mA	
	I_{OL1}	V_{OL1} = 0.5 V	V_{DDI} = 1.5 V	0.2	1.2	2.0	mA	
			V_{DDI} = 3.0 V	1.0	3.0	5.0	mA	
			V_{DDI} = 5.0 V	1.5	4.0	8.0	mA	
Output Current 2 (BD, BDB)	I_{OH2}	V_{OH2} = V_{DD} – 0.7 V	V_{DD} = 1.5 V	–2.5	–1.3	–0.4	mA	
			V_{DD} = 3.0 V	–6.0	–4.0	–2.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	–9.0	–5.5	–3.0	mA	
	I_{OL2}	V_{OL2} = 0.7 V	V_{DD} = 1.5 V	0.4	1.3	2.5	mA	
			V_{DD} = 3.0 V	2.0	4.0	6.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	3.0	5.5	9.0	mA	
Output Current 3 (SEG0 to SEG31) (COM1 to COM16)	I_{OH3}	V_{OH3} = V_{DD5} – 0.2 V (V_{DD5} level)		—	—	–4	µA	2
	I_{OHM3}	V_{OHM3} = V_{DD4} + 0.2 V (V_{DD4} level)		4	—	—	µA	
	I_{OHM3S}	V_{OHM3S} = V_{DD4} – 0.2 V (V_{DD4} level)		—	—	–4	µA	
	I_{OMH3}	V_{OMH3} = V_{DD3} + 0.2 V (V_{DD3} level)		4	—	—	µA	
	I_{OMH3S}	V_{OMH3S} = V_{DD3} – 0.2 V (V_{DD3} level)		—	—	–4	µA	
	I_{OML3}	V_{OML3} = V_{DD2} + 0.2 V (V_{DD2} level)		4	—	—	µA	
	I_{OML3S}	V_{OML3S} = V_{DD2} – 0.2 V (V_{DD2} level)		—	—	–4	µA	
	I_{OLM3}	V_{OLM3} = V_{DD1} + 0.2 V (V_{DD1} level)		4	—	—	µA	
	I_{OLM3S}	V_{OLM3S} = V_{DD1} – 0.2 V (V_{DD1} level)		—	—	–4	µA	
	I_{OL3}	V_{OL3} = V_{SS} + 0.2 V (V_{SS} level)		4	—	—	µA	
Output Current 4 (OSC1)	I_{OH4R}	V_{OH4R} = V_{DDH} – 0.5 V (RC oscillation)	V_{DD} = V_{DDH} = 3.0 V	–2.5	–1.5	–0.75	mA	
			V_{DD} = V_{DDH} = 5.0 V	–3.5	–2.0	–1.0	mA	
	I_{OL4R}	V_{OL4R} = 0.5 V (RC oscillation)	V_{DD} = V_{DDH} = 3.0 V	0.75	1.5	2.5	mA	
			V_{DD} = V_{DDH} = 5.0 V	1.0	2.0	3.5	mA	
	I_{OH4C}	V_{OH4C} = V_{DDH} – 0.5 V (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	–300	–180	–60	µA	
			V_{DD} = V_{DDH} = 5.0 V	–450	–280	–100	µA	
	I_{OL4C}	V_{OL4C} = 0.5 V (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	60	120	300	µA	
			V_{DD} = V_{DDH} = 5.0 V	100	200	450	µA	
Output Leakage (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) (PA.0 to PA.3)	I_{OOH}	V_{OH} = V_{DDI}		—	—	0.3	µA	
	I_{OOL}	V_{OL} = V_{SS}		–0.3	—	—	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{SS} = 0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

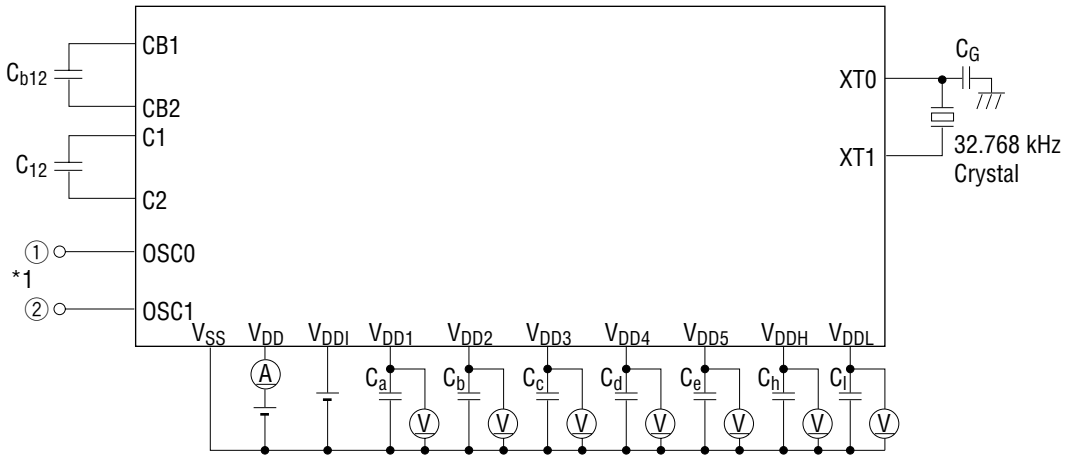
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) (PA.0 to PA.3)	I_{IH1}	V_{IH1} = V_{DDI} (when pulled down)	V_{DDI} = 1.5 V	2	10	30	µA	3
			V_{DDI} = 3.0 V	30	90	180	µA	
			V_{DDI} = 5.0 V	70	250	600	µA	
	I_{IL1}	V_{IL1} = V_{SS} (when pulled up)	V_{DDI} = 1.5 V	–30	–10	–2	µA	
			V_{DDI} = 3.0 V	–180	–90	–30	µA	
			V_{DDI} = 5.0 V	–600	–250	–70	µA	
	I_{IH1Z}	V_{IH1} = V_{DDI} (in a high impedance state)		0.0	—	1.0	µA	
	I_{IL1Z}	V_{IL1} = V_{SS} (in a high impedance state)		–1.0	—	0.0	µA	
Input Current 2 (OSC0)	I_{IL2}	V_{IL2} = V_{SS} (when pulled up)	V_{DD} = V_{DDH} = 3.0 V	–200	–110	–30	µA	
			V_{DD} = V_{DDH} = 5.0 V	–600	–350	–150	µA	
	I_{IH2R}	V_{IH2R} = V_{DDH} (RC oscillation)		0.0	—	1.0	µA	
	I_{IL2R}	V_{IL2R} = V_{SS} (RC oscillation)		–1.0	—	0.0	µA	
	I_{IH2C}	V_{IH2C} = V_{DDH} (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	0.1	0.5	1.0	µA	
			V_{DD} = V_{DDH} = 5.0 V	0.75	1.5	3.0	µA	
	I_{IL2C}	V_{IL2C} = V_{SS} (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	–1.0	–0.5	–0.1	µA	
			V_{DD} = V_{DDH} = 5.0 V	–3.0	–1.5	–0.75	µA	
Input Current 3 (RESET)	I_{IH3}	V_{IH3} = V_{DD}	V_{DD} = 1.5 V	10	50	80	µA	
			V_{DD} = 3.0 V	150	350	600	µA	
			V_{DD} = V_{DDH} = 5.0 V	0.5	1.0	2.0	mA	
	I_{IL3}	V_{IL3} = V_{SS}		–1.0	—	0.0	µA	
Input Current 4 (TST1, TST2)	I_{IH4}	V_{IH4} = V_{DD}	V_{DD} = 1.5 V	50	150	300	µA	
			V_{DD} = 3.0 V	0.5	1.0	1.5	mA	
			V_{DD} = V_{DDH} = 5.0 V	1.25	2.5	4.0	mA	
	I_{IL4}	V_{IL4} = V_{SS}		–1.0	—	0.0	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{SS} = 0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

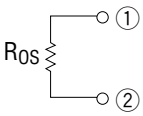
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) (PA.0 to PA.3)	V_{IH1}	V_{DDI} = 1.5 V	1.2	—	1.5	V	
		V_{DDI} = 3.0 V	2.4	—	3.0	V	
		V_{DDI} = 5.0 V	4.0	—	5.0	V	
	V_{IL1}	V_{DDI} = 1.5 V	0.0	—	0.3	V	
		V_{DDI} = 3.0 V	0.0	—	0.6	V	
		V_{DDI} = 5.0 V	0.0	—	1.0	V	
Input Voltage 2 (OSC0)	V_{IH2}	V_{DD} = V_{DDH} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL2}	V_{DD} = V_{DDH} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = V_{DDH} = 5.0 V	0.0	—	1.0	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	V_{DD} = 1.5 V	1.35	—	1.5	V	
		V_{DD} = 3.0 V	2.4	—	3.0	V	4
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL3}	V_{DD} = 1.5 V	0.0	—	0.15	V	
		V_{DD} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = V_{DDH} = 5.0 V	0.0	—	1.0	V	
Hysteresis Width 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (PA.0 to PA.3)	ΔV_{T1}	V_{DDI} = 1.5 V	0.05	0.1	0.3	V	
		V_{DDI} = 3.0 V	0.2	0.5	1.0	V	
		V_{DDI} = 5.0 V	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV_{T2}	V_{DD} = 1.5 V	0.05	0.1	0.3	V	
		V_{DD} = 3.0 V	0.2	0.5	1.0	V	
		V_{DD} = V_{DDH} = 5.0 V	0.25	1.0	1.5	V	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) (PA.0 to PA.3)	C_{IN}	—	—	—	5	pF	1

Measuring circuit 1

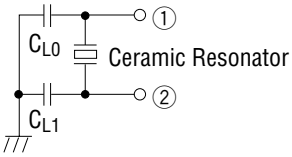


C_a, C_b, C_c, C_d, C_e, C_l, C_{12} : 0.1 µF
C_{b12}, C_h : 1 µF
C_G : 15 pF
C_{L0} : 30 pF
C_{L1} : 30 pF
Ceramic Resonator : CSA2.00MG (2 MHz)
CSB1000J (1 MHz)
(Murata MFG.-make)

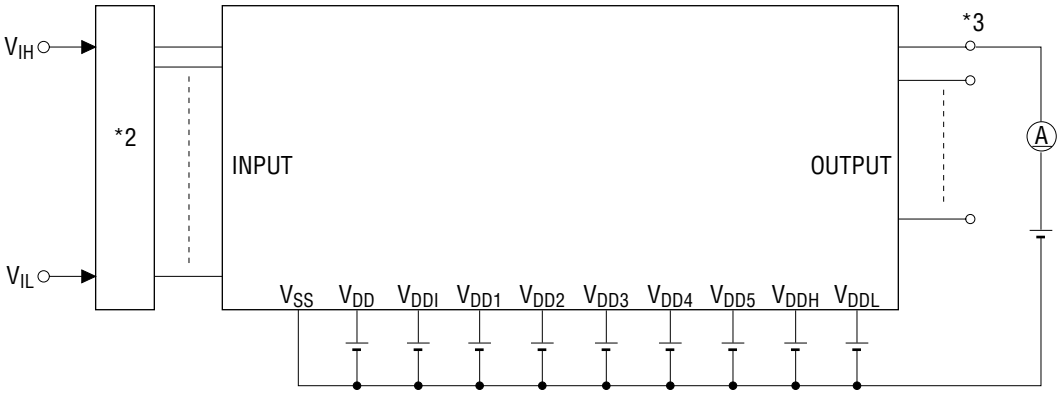
*1 RC Oscillator



Ceramic Oscillator

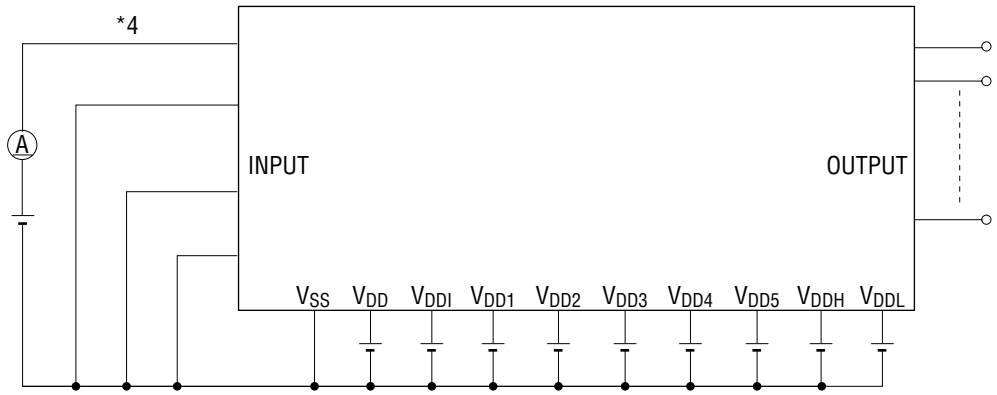


Measuring circuit 2

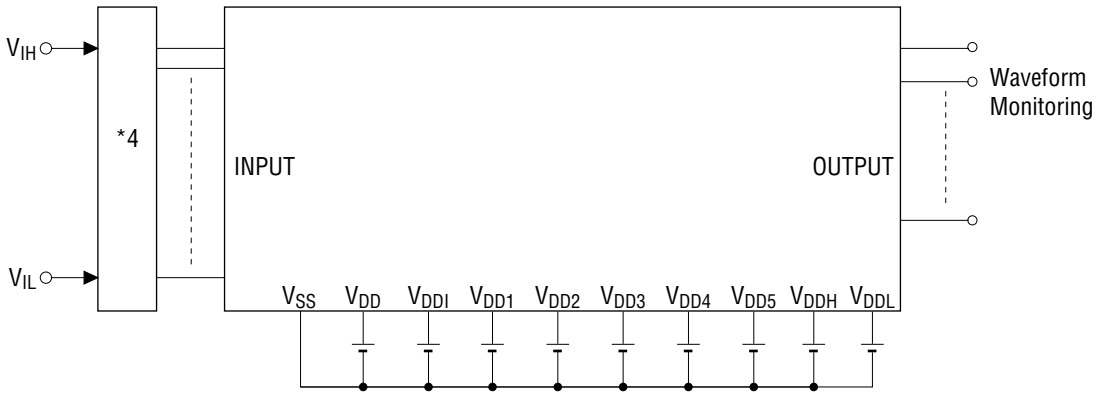


*2 Input logic circuit to determine the specified measuring conditions.
*3 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*4 Measured at the specified input pins.

AC Characteristics (External Memory Interface)

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Reading from External Memory

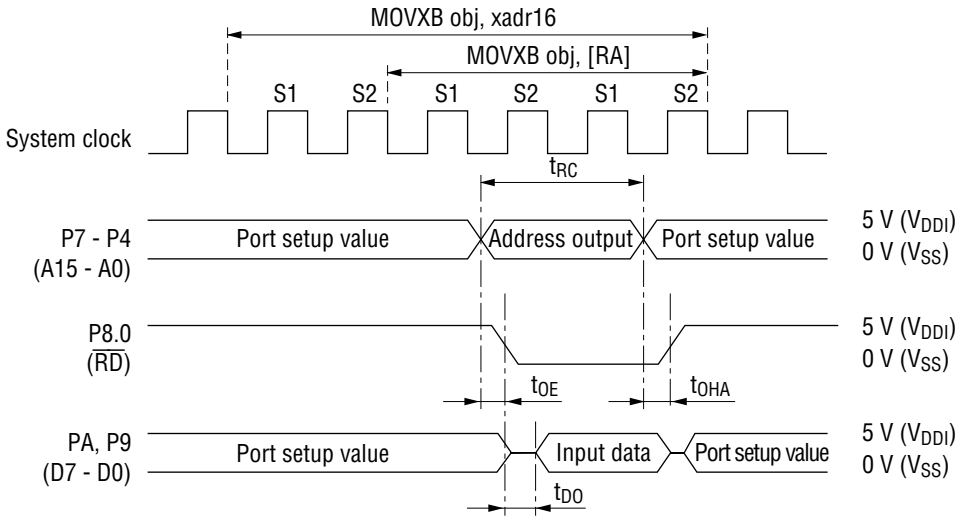
(a) When CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61.0	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	5.0	µs
Output Valid Time	t_{OHA}	—	—	—	5.0	µs
External Memory Output Delay Time	t_{DO}	—	—	—	5.0	µs

(b) When CPU operates at 2 MHz (V_{DDH} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1.0	—	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	100	ns
Output Valid Time	t_{OHA}	—	—	—	100	ns
External Memory Output Delay Time	t_{DO}	—	—	—	150	ns

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



(2) Writing to External Memory

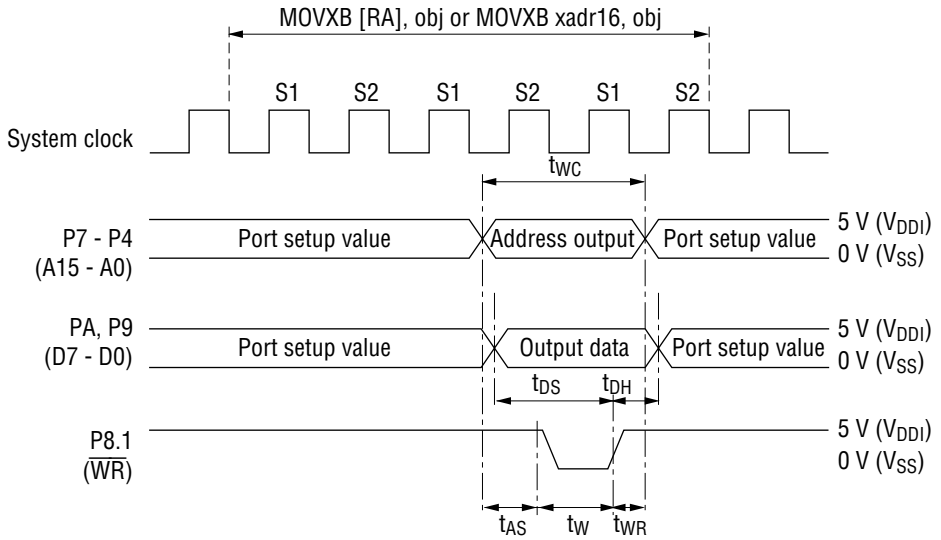
(a) When CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61.0	—	µs
Address Setup Time	t_{AS}	—	—	30.5	—	µs
Write Time	t_{W}	—	—	15.3	—	µs
Write Recovery Time	t_{WR}	—	—	15.3	—	µs
Data Setup Time	t_{DS}	—	—	45.8	—	µs
Data Hold Time	t_{DH}	—	—	15.3	—	µs

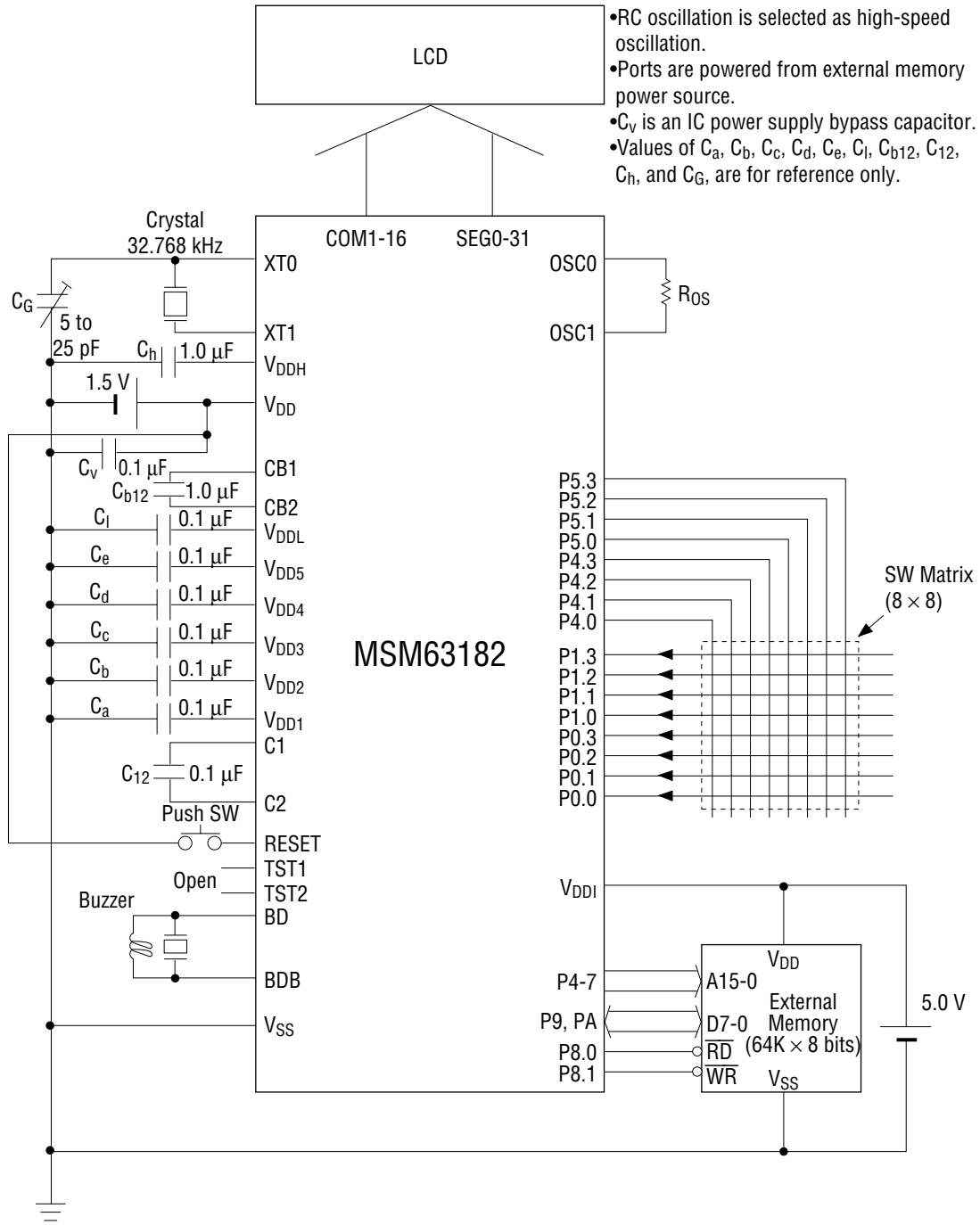
(b) When CPU operates at 2 MHz (V_{DDH} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1.0	—	—	µs
Address Setup Time	t_{AS}	—	0.4	—	—	µs
Write Time	t_{W}	—	0.2	—	—	µs
Write Recovery Time	t_{WR}	—	0.2	—	—	µs
Data Setup Time	t_{DS}	—	0.7	—	—	µs
Data Hold Time	t_{DH}	—	0.2	—	—	µs

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



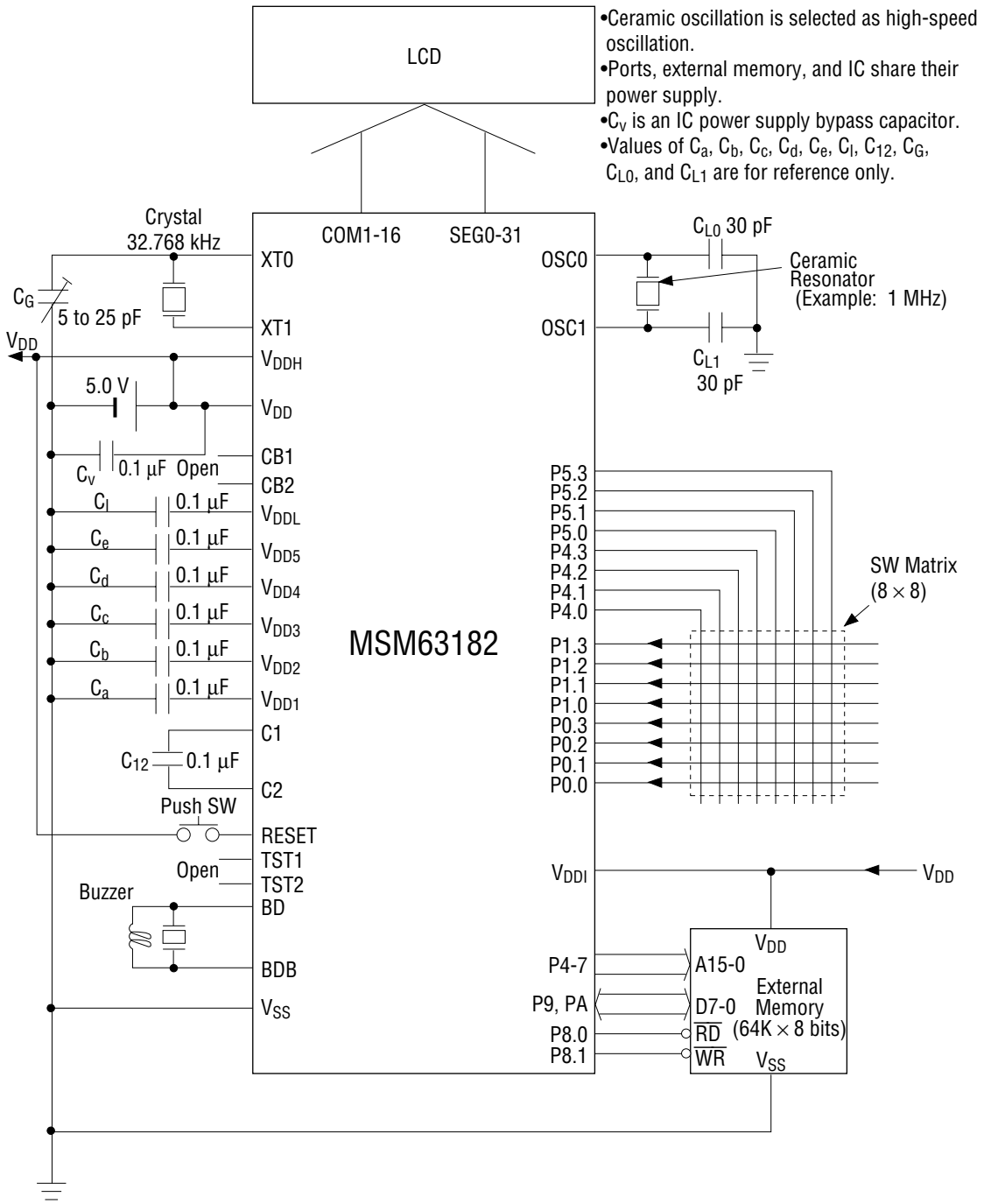
APPLICATION CIRCUITS



Note: V_{DDI} is the power supply pin for the input, output, and input-output ports. Be sure to connect the V_{DDI} pin either to the positive power supply pin (V_{DD}) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with Power Supply Backup

APPLICATION CIRCUITS (continued)



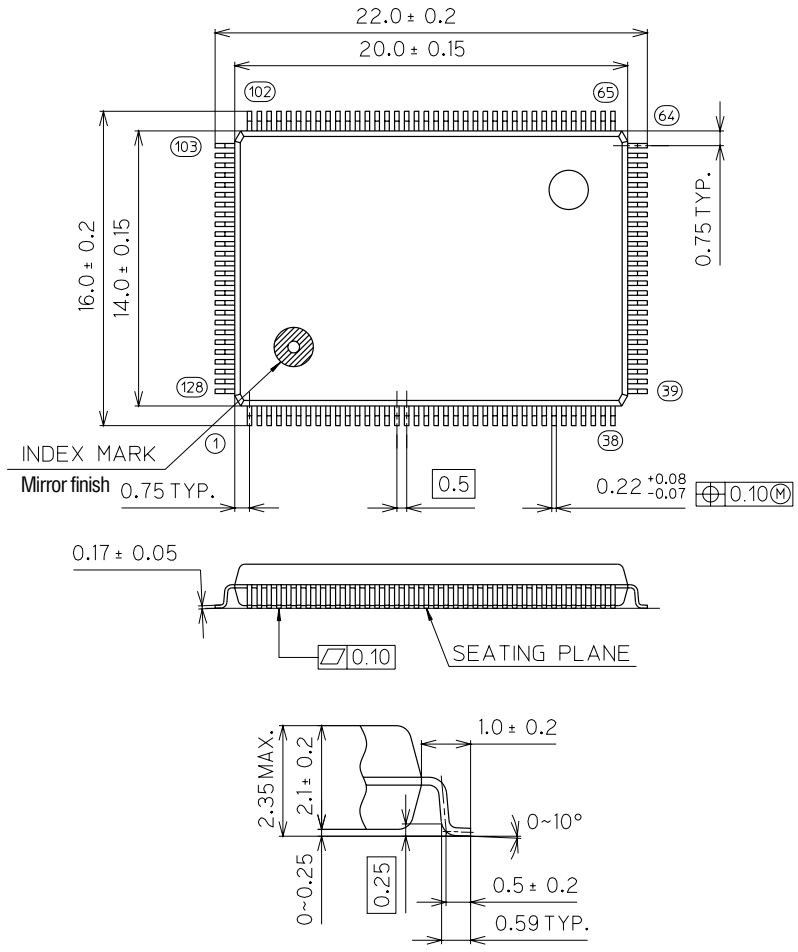
Note: V_{DDI} is the power supply pin for the input, output, and input-output ports. Be sure to connect the V_{DDI} pin either to the positive power supply pin (V_{DD}) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with No Power Supply Backup

PACKAGE DIMENSIONS

(Unit : mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.19 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).