

FEATURES

- 64K x 8 organization
- Wide voltage range, 2.7V to 3.6V
- +12.5V programming voltage
- Fast access time: 120/150/200/250ns
- Totally static operation
- Completely TTL compatible
- Operating current: 10mA @ 3.6V, 5MHz
- Standby current: 10uA
- Package type:
 - 28 pin plastic DIP
 - 32 pin PLCC
 - 28 pin 8 x 13.4 mm TSOP(I)

GENERAL DESCRIPTION

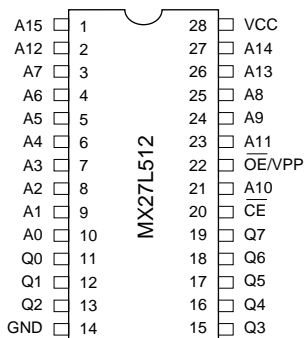
The MX27L512 is a 3V only, 512K-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 64K words by 8 bits per word, operates from a single +3volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM

programmers may be used. The MX27L512 supports intelligent fast programming algorithm which can result in programming time of less than fifteen seconds.

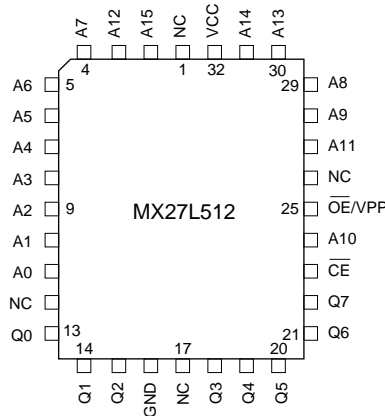
This EPROM is packaged in industry standard 28 pin dual-in-line packages , 32 lead PLCC, and 28 lead TSOP(I) packages.

PIN CONFIGURATIONS

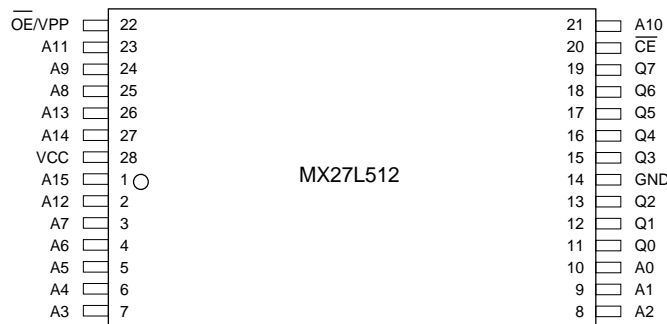
PDIP



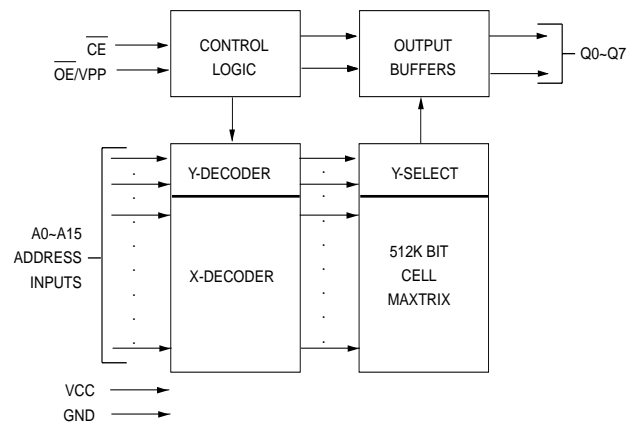
PLCC



8 x 13.4mm 28TSOP(I)



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A15	Address Input
Q0~Q7	Data Input/Output
CE	Chip Enable Input
OE/VPP	Output Enable Input/Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE PROGRAMMING OF THE MX27L512

When the MX27L512 is delivered, or it is erased, the chip has all 512K bits in the "ONE", or HIGH state. "ZEROS" are loaded into the MX27L512 through the procedure of programming.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

Vcc must be applied simultaneously or before Vpp, and removed simultaneously or after Vpp. When programming an MXIC EPROM, a 0.1uF capacitor is required across Vpp and ground to suppress spurious voltage transients which may damage the device.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage $\overline{OE}/VPP = 12.75V$ is applied, with $VCC = 6.25V$, (Algorithm is shown in Figure 1). The programming is achieved by applying a single TTL low level 100us pulse to the \overline{CE} input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at $VCC = 5V \pm 10\%$.

PROGRAM INHIBIT MODE

Programming of multiple MX27L512s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for \overline{CE} and \overline{OE} , all like inputs of the parallel MX27L512 may be common. A TTL low-level program pulse applied to an MX27L512 \overline{CE} input with $\overline{OE}/VPP = 12.5 \pm 0.5V$ will program that MX27L512. A high-level \overline{CE} input inhibits the other MX27L512s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with \overline{OE}/VPP and \overline{CE} , at VIL. Data should be verified tDV after the falling edge of \overline{CE} .

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}C \pm 5^{\circ}C$ ambient temperature range that is required when programming the MX27L512.

To activate this mode, the programming equipment must force $12.0 \pm 0.5(VH)$ on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27L512, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (Q7) defined as the parity bit.

READ MODE

The MX27L512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from \overline{CE} to output (tCE). Data is available at the outputs tOE after the falling edge of \overline{OE} , assuming that \overline{CE} has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27L512 has a CMOS standby mode which reduces the maximum VCC current to 10 uA. It is placed in CMOS standby when \overline{CE} is at $VCC \pm 0.3V$. The MX27L512 also has a TTL-standby mode which reduces the maximum VCC current to 0.25 mA. It is placed in TTL-standby when \overline{CE} is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the \overline{OE} input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that \overline{CE} be decoded and used as the primary device-selecting function, while \overline{OE} be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

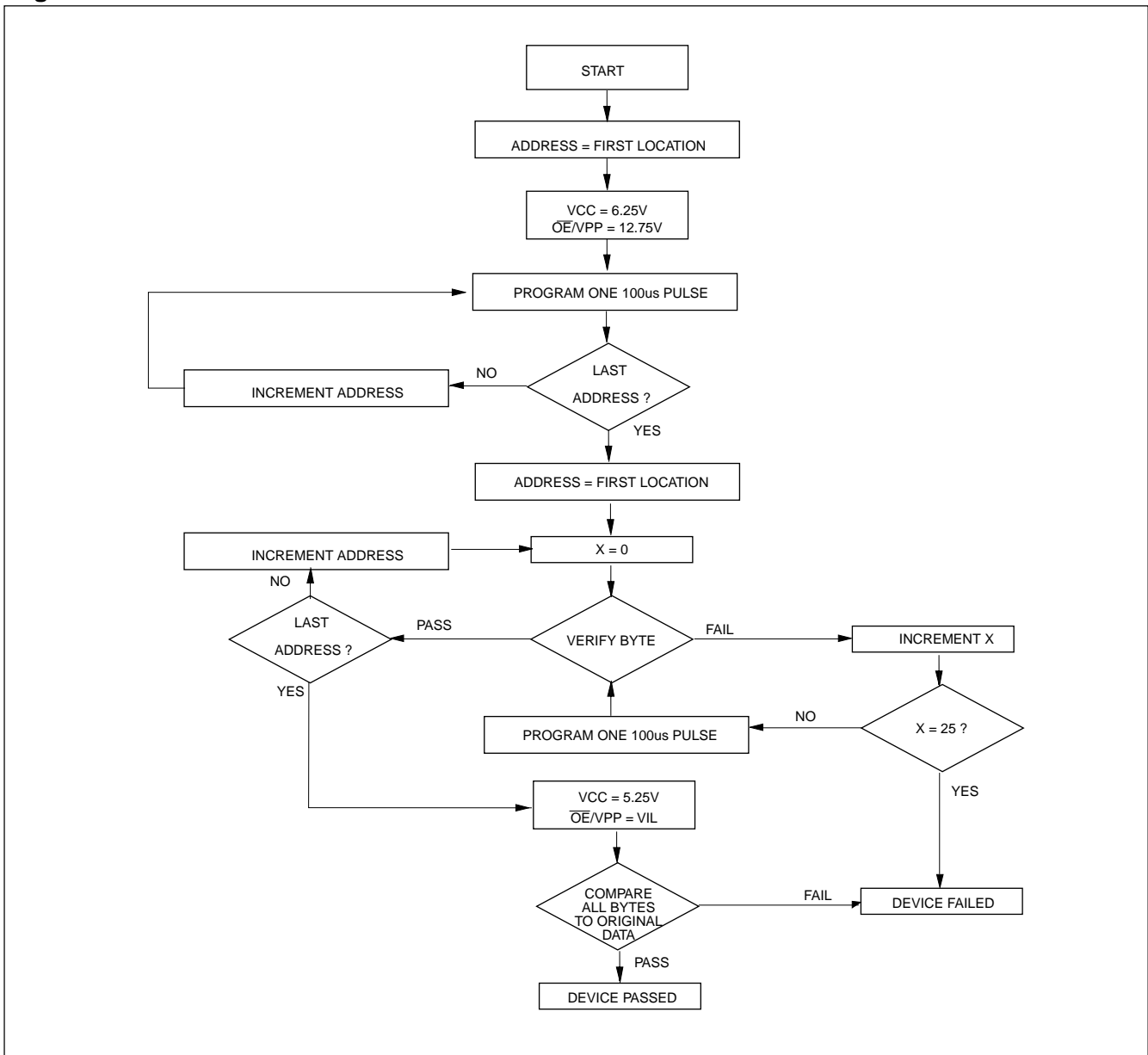
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

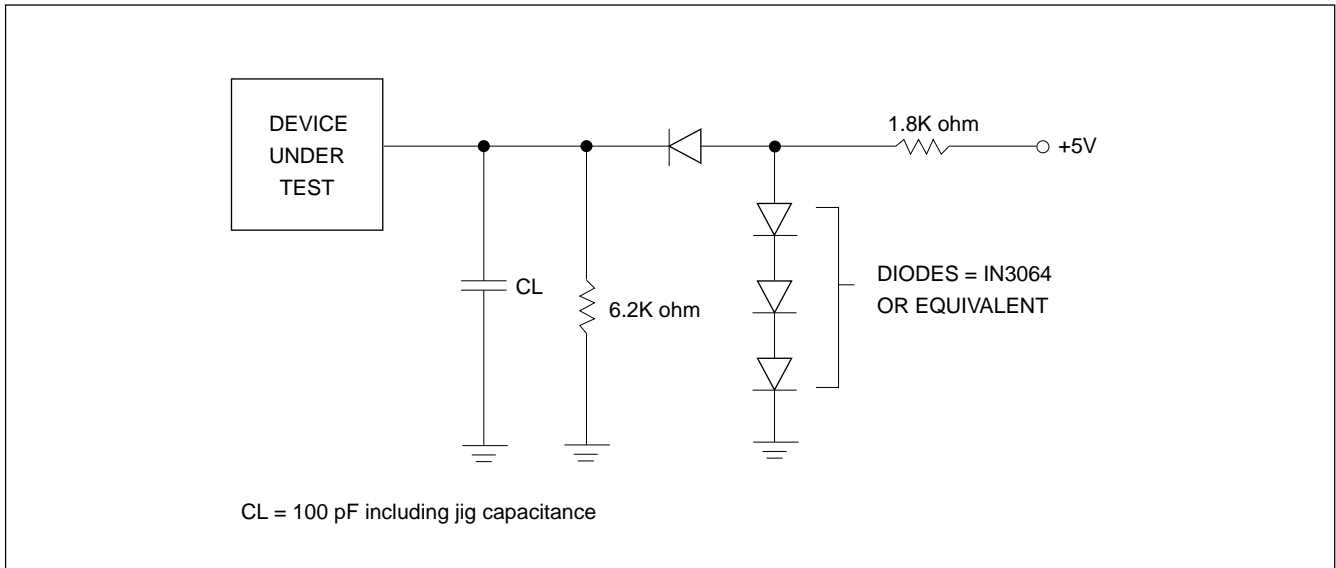
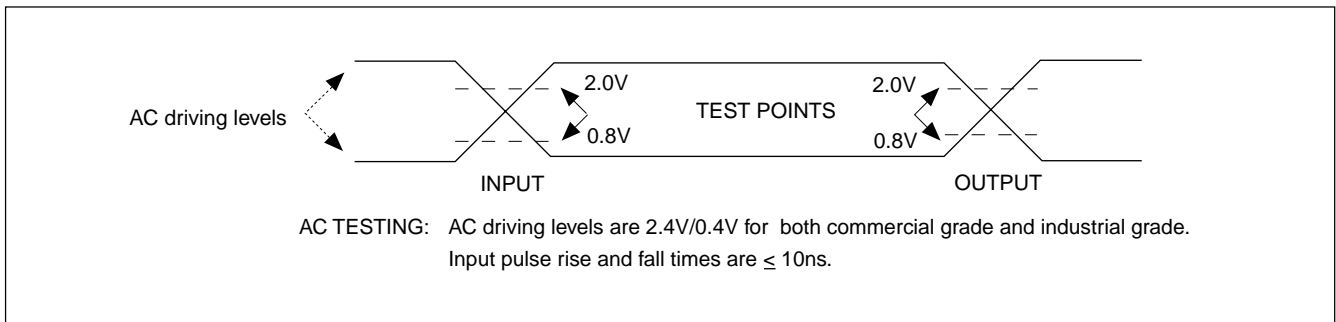
MODE SELECT TABLE

MODE	PINS				
	\overline{CE}	\overline{OE}/VPP	A0	A9	OUTPUTS
Read	VIL	VIL	X	X	DOUT
Output Disable	VIL	VIH	X	X	High Z
Standby (TTL)	VIH	X	X	X	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	High Z
Program	VIL	VPP	X	X	DIN
Program Verify	VIL	VIL	X	X	DOUT
Program Inhibit	VIH	VPP	X	X	High Z
Manufacturer Code(3)	VIL	VIL	VIL	VH	C2H
Device Code(3)	VIL	VIL	VIH	VH	91H

- NOTES:**
1. VH = 12.0 V ± 0.5 V
 2. X = Either VIH or VIL

3. A1 - A8 = A10 - A15 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

Figure1. FAST PROGRAMMING FLOW CHART


SWITCHING TEST CIRCUITS

SWITCHING TEST WAVEFORMS


ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:

Specifications contained within the following tables are subject to change.

DC/AC Operating Conditions for Read Operation

		MX27L512			
		-12	-15	-20	-25
Operating Temperature	Commercial	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
	Industrial	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
Vcc Power Supply		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc-0.3		V	IOH = -100uA, VCC = 3.0V
VOL	Output Low Voltage		0.3	V	IOL = 2.1mA, VCC = 3.0V
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.6	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 3.6V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 3.6V
ICC3	VCC Power-Down Current		10	uA	$\overline{CE} = VCC \pm 0.3V$
ICC2	VCC Standby Current		0.25	mA	$\overline{CE} = VIH$
ICC1	VCC Active Current		10	mA	$\overline{CE} = VIL, f=5MHz, Iout = 0mA, Vcc=3.6V$
IPP	VPP Supply Current Read		10	uA	$\overline{CE} = VIL, VPP = VCC$

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
Vpp	VPP Capacitance	18	25	pF	VPP = 0V

**AC CHARACTERISTICS**

SYMBOL	PARAMETER	27L512-12		27L512-15		27L512-20		27L512-25		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		120		150		200		250	ns	$\overline{CE} = \overline{OE} = VIL$
tCE	Chip Enable to Output Delay		120		150		200		250	ns	$\overline{OE} = VIL$
tOE	Output Enable to Output Delay		60		65		100		120	ns	$\overline{CE} = VIL$
tDF	\overline{OE} High to Output Float, or \overline{CE} High to Output Float	0	40	0	50	0	60	0	70	ns	
tOH	Output Hold from Address, \overline{CE} or \overline{OE} which ever occurred first	0		0		0		0		ns	

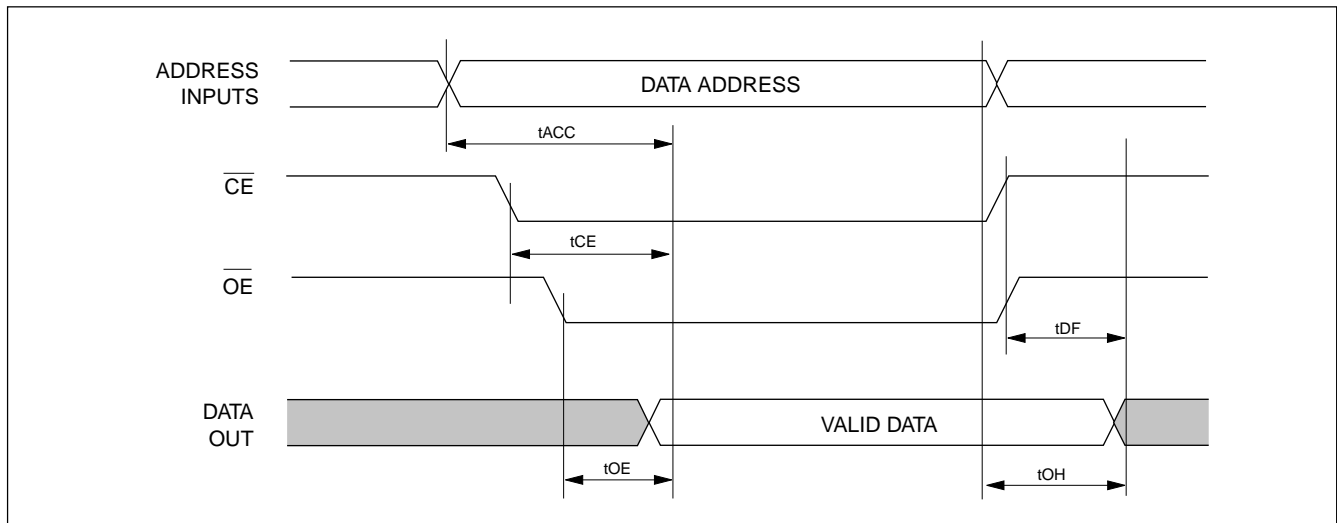
DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.2	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current(Program & Verify)		40	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE} = VIL$
VCC1	Fast Programming Supply Voltage	6.00	6.50	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

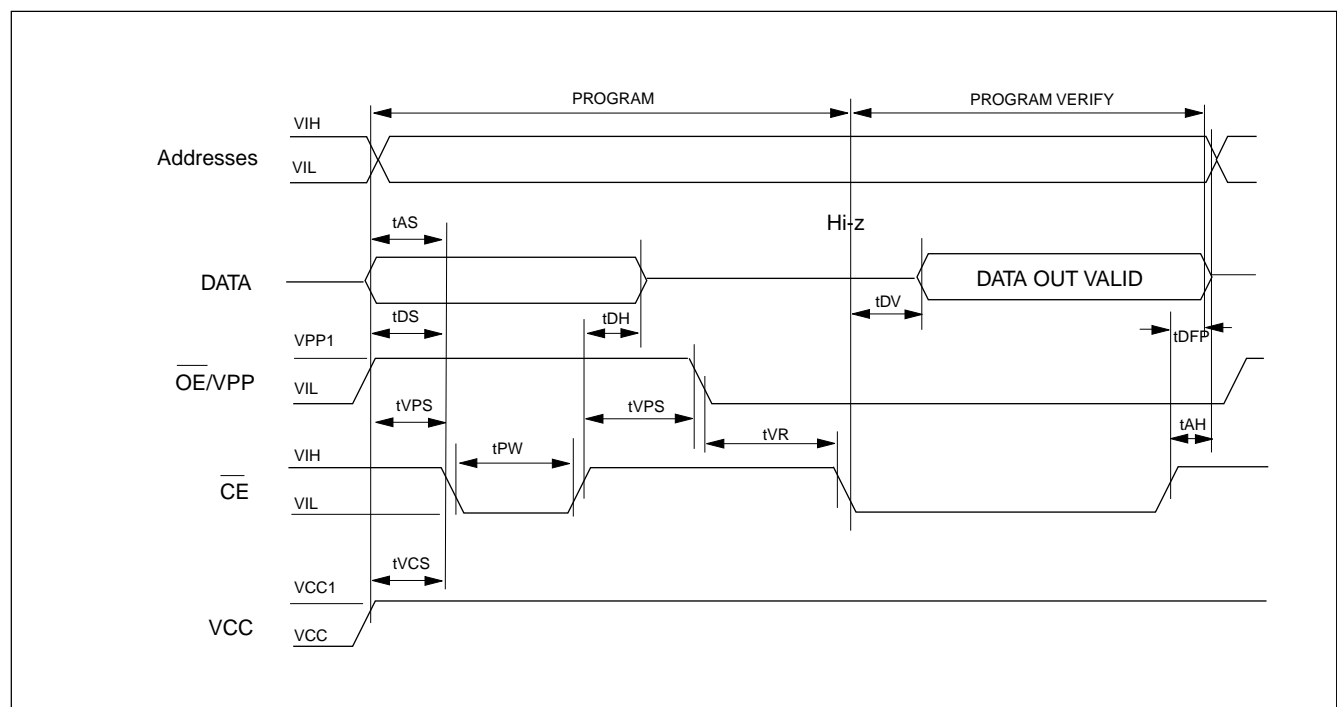
AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time	2		us	
tDS	Data Setup Time	2		us	
tAH	Address Hold Time	0		us	
tDH	Data Hold Time	2		us	
tDFP	Chip Enable to Output Float Delay	0	130	ns	
tVPS	VPP Setup Time	2		us	
tPW	\overline{CE} Program Pulse Width	95	105	us	
tVCS	Vcc Setup Time	2		us	
tDV	Data Valid from \overline{CE}		150	ns	
tOEH	\overline{OE} /VPP Hold Time	2		ns	
tVR	\overline{OE} /VPP Recovery Time	2		ns	

WAVEFORMS READ CYCLE



FAST PROGRAMMING ALGORITHM WAVEFORM

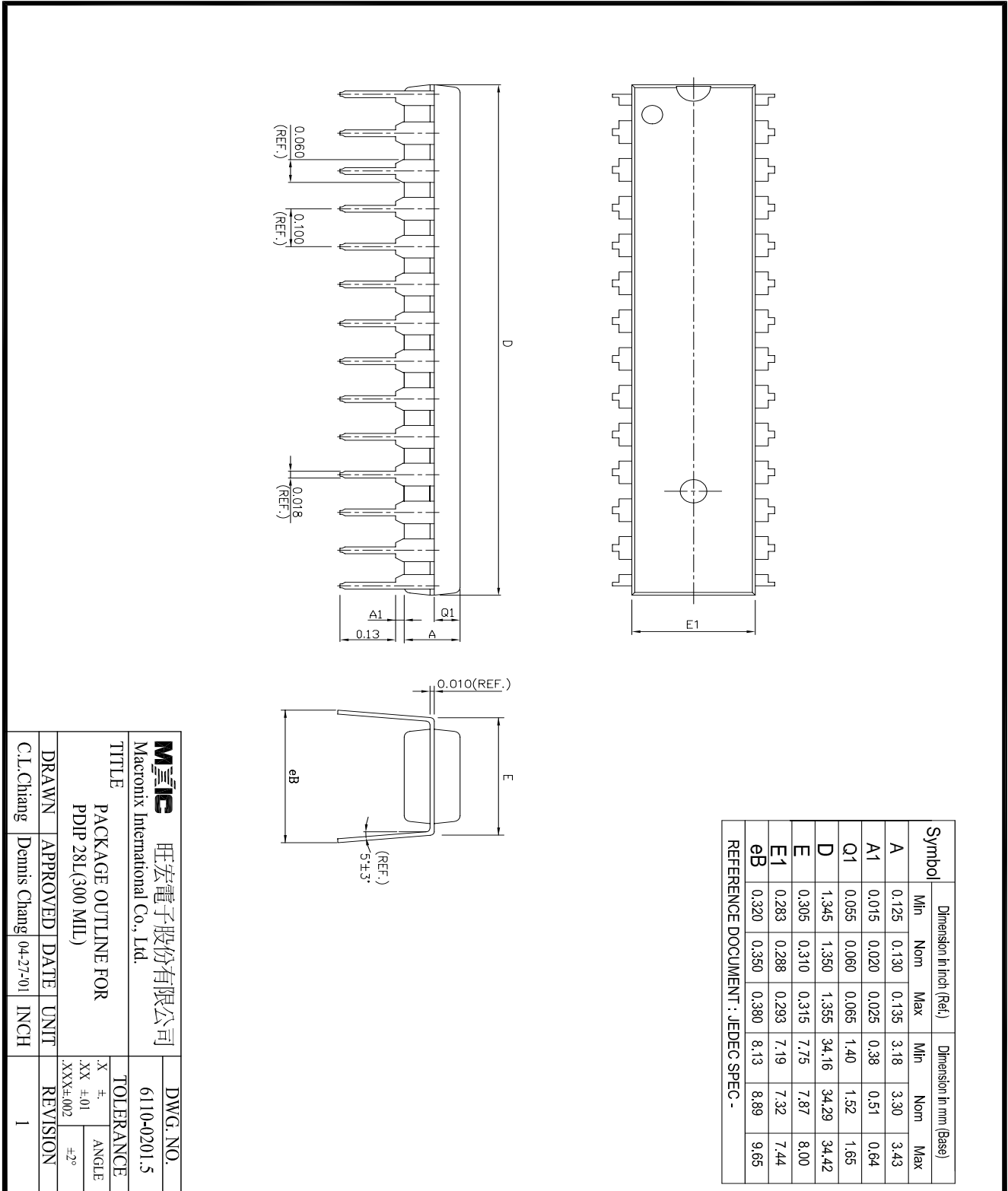


ORDERING INFORMATION**PLASTIC PACKAGE**

PART NO.	ACCESS TIME(ns)	OPERATING	STANDBY	OPERATING	PACKAGE
		CURRENT MAX.(mA)	CURRENT MAX.(uA)	TEMPERATURE	
MX27L512PC-12	120	10	10	0°C to 70°C	28 Pin DIP
MX27L512QC-12	120	10	10	0°C to 70°C	32 Pin PLCC
MX27L512TC-12	120	10	10	0°C to 70°C	28 Pin TSOP(I)
MX27L512PC-15	150	10	10	0°C to 70°C	28 Pin DIP
MX27L512QC-15	150	10	10	0°C to 70°C	32 Pin PLCC
MX27L512TC-15	150	10	10	0°C to 70°C	28 Pin TSOP(I)
MX27L512PC-20	200	10	10	0°C to 70°C	28 Pin DIP
MX27L512QC-20	200	10	10	0°C to 70°C	32 Pin PLCC
MX27L512TC-20	200	10	10	0°C to 70°C	28 Pin TSOP(I)
MX27L512PC-25	250	10	10	0°C to 70°C	28 Pin DIP
MX27L512QC-25	250	10	10	0°C to 70°C	32 Pin PLCC
MX27L512TC-25	250	10	10	0°C to 70°C	28 Pin TSOP(I)
MX27L512PI-12	120	10	10	-40°C to 85°C	28 Pin DIP
MX27L512QI-12	120	10	10	-40°C to 85°C	32 Pin PLCC
MX27L512TI-12	120	10	10	-40°C to 85°C	28 Pin TSOP(I)
MX27L512PI-15	150	10	10	-40°C to 85°C	28 Pin DIP
MX27L512QI-15	150	10	10	-40°C to 85°C	32 Pin PLCC
MX27L512TI-15	150	10	10	-40°C to 85°C	28 Pin TSOP(I)
MX27L512PI-20	200	10	10	-40°C to 85°C	28 Pin DIP
MX27L512QI-20	200	10	10	-40°C to 85°C	32 Pin PLCC
MX27L512TI-20	200	10	10	-40°C to 85°C	28 Pin TSOP(I)
MX27L512PI-25	250	10	10	-40°C to 85°C	28 Pin DIP
MX27L512QI-25	250	10	10	-40°C to 85°C	32 Pin PLCC
MX27L512TI-25	250	10	10	-40°C to 85°C	28 Pin TSOP(I)

PACKAGE INFORMATION

28-PIN PLASTIC DIP (600 mil)

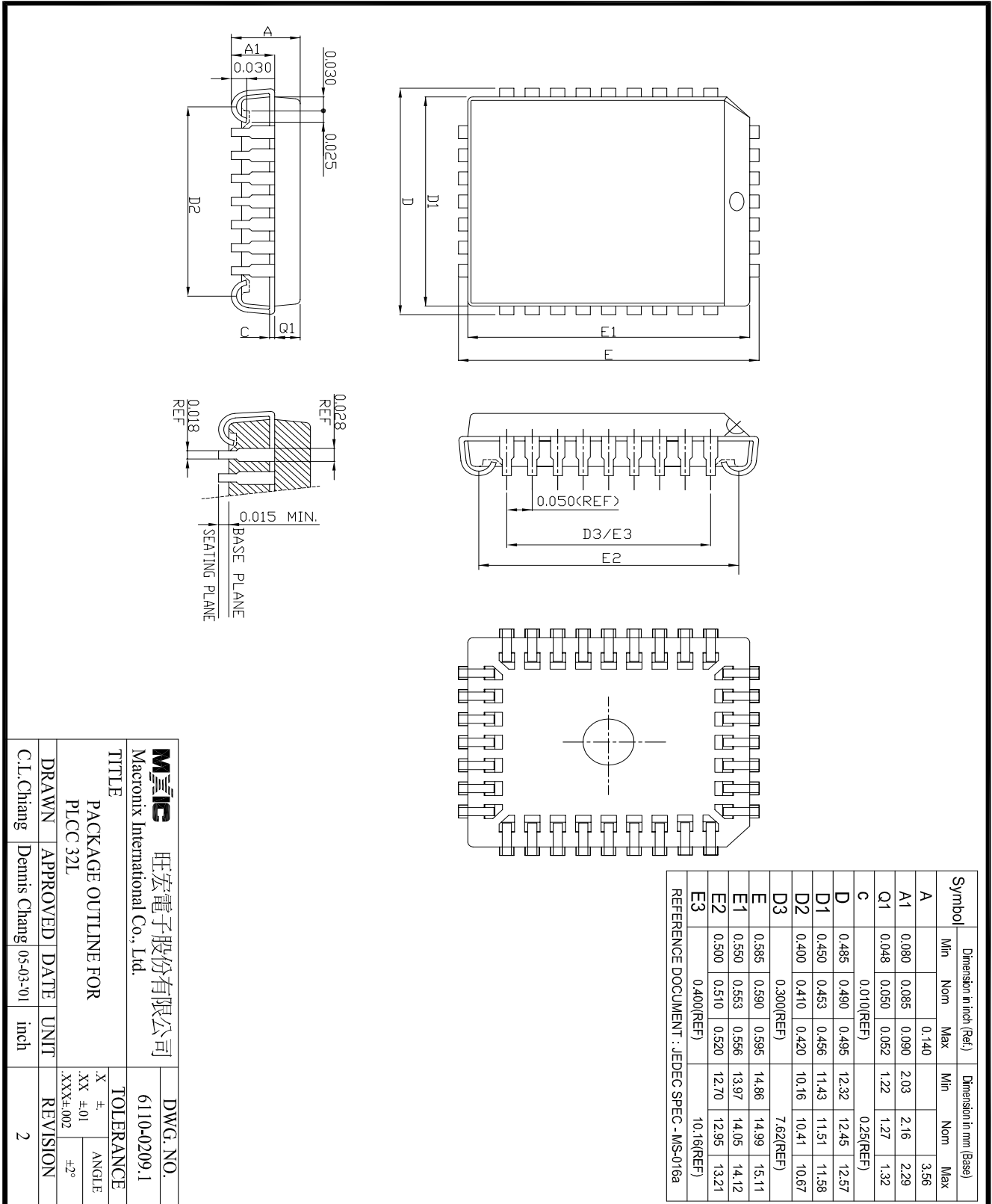


Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	0.125	0.130	0.135	3.18	3.30	3.43
A1	0.015	0.020	0.025	0.38	0.51	0.64
Q1	0.055	0.060	0.065	1.40	1.52	1.65
D	1.345	1.350	1.355	34.16	34.29	34.42
E	0.305	0.310	0.315	7.75	7.87	8.00
E1	0.283	0.288	0.293	7.19	7.32	7.44
eB	0.320	0.350	0.380	8.13	8.89	9.65

REFERENCE DOCUMENT : JEDEC SPEC -

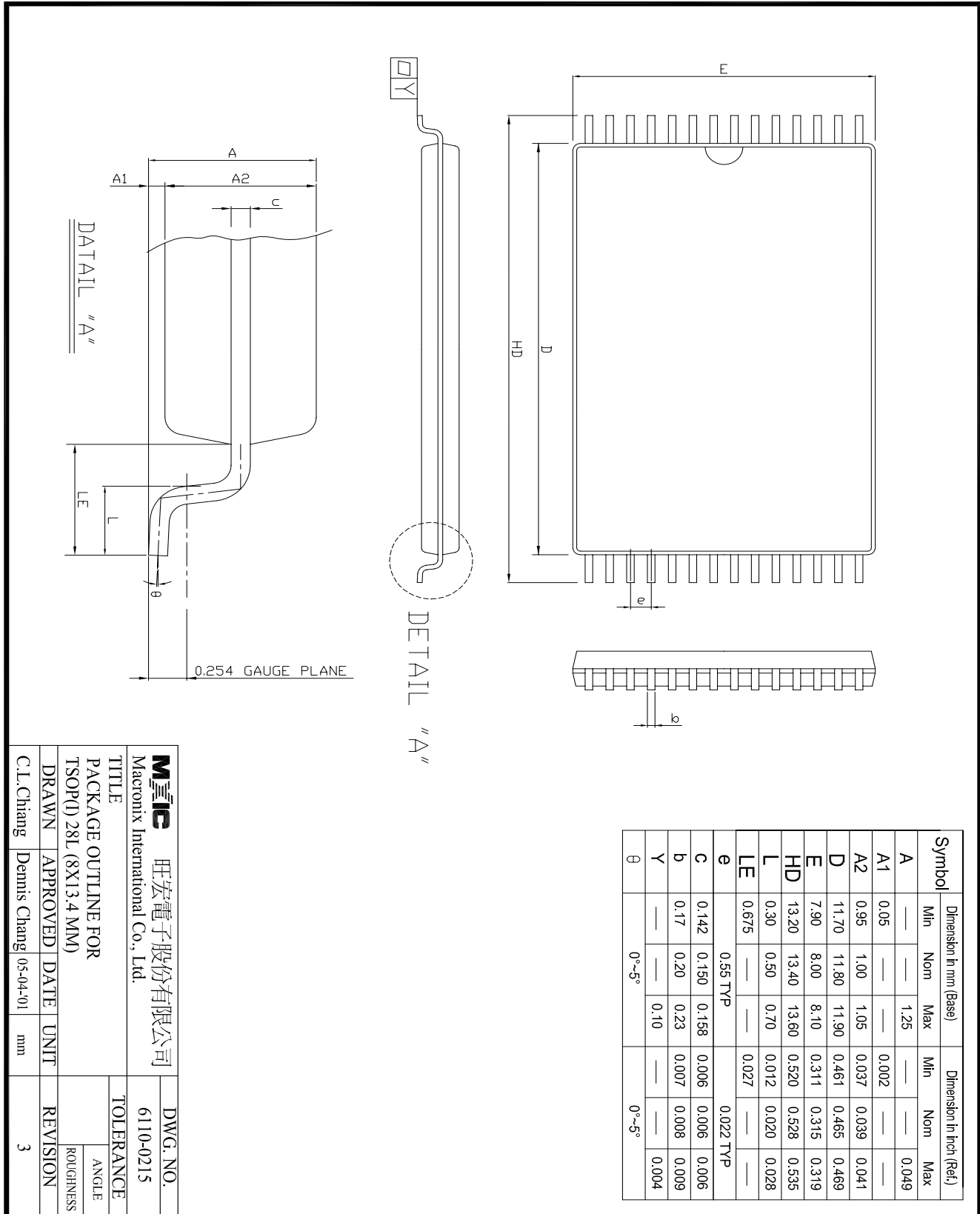
MAGIC 旺宏電子股份有限公司		DWG. NO.	
Macronix International Co., Ltd.		6110-0201.5	
TITLE		TOLERANCE	
PACKAGE OUTLINE FOR		X ±	
PDIP 28L(300 MIL)		XX ±01	
		.XXX±.002	
DRAWN		REVISION	
APPROVED		DATE	
C.L.Chiang		Dennis Chang	
04-27-01		INCH	
		UNIT	
		1	

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



MIC 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0209.1	
TITLE PACKAGE OUTLINE FOR PLCC 32L			
DRAWN C.L.Chang		APPROVED Dennis Chang	DATE 05-03-01
UNIT inch		REVISION 2	
TOLERANCE .X ± .XX ±.01 .XXX±.002		ANGLE ±2°	

8 x 13.4mm 28-PIN PLASTIC TSOP



MAGIC 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 61110-0215	
TITLE PACKAGE OUTLINE FOR TSOP(0) 28L (8X13.4 MM)			
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-04-01	mm
REVISION			3
TOLERANCE		ANGLE	
ROUGHNESS			

REVISION HISTORY

Revision No.	Description	Page	Date
2.0	1)Programming Flow Chart corrected, programming verify after whole array programmed with 1 pulse. 2) Eliminate Interactive Programming Mode. 3) Add 28-TSOP(I) and 28-SOP packages offering. 4) AC driving levels are changed from 2.4V/0.3V to 2.4V/0.4V.		6/05/1997
2.1	General description, "... is a 5V only..." ==> "...is a 3V only...."		9/25/1998
2.2	Cancel ceramic DIP package type	P1,2,9,11	MAR/02/2000
2.3	Remove 28-pin SOP Package Package Information format changed	P1,9 P10~12	SEP/19/2001



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