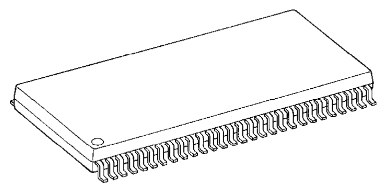
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16821FT

LOW-VOLTAGE 20-BIT D-TYPE FLIP-FLOP WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16821FT is a high performance CMOS 20-bit D-TYPE FLIP-FLOP. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.
The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. The twenty flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CK) transition.
When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

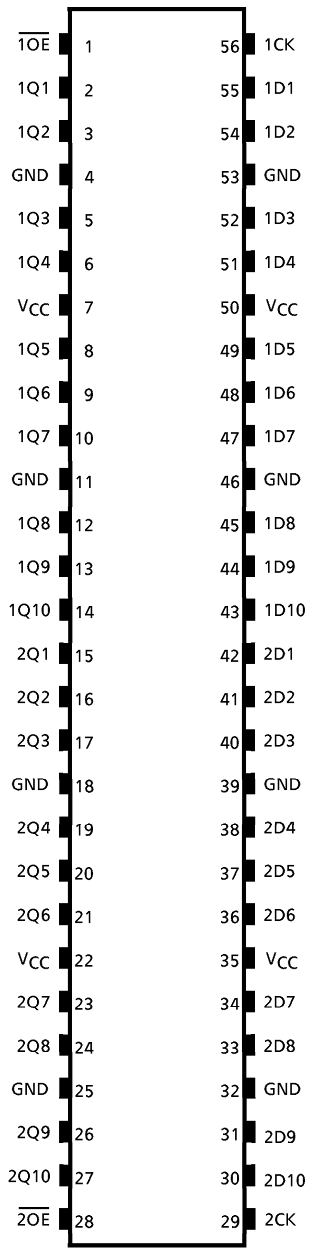
Weight : 0.25 g (Typ.)

FEATURES

- Low Voltage Operation : V_{CC} = 1.8~3.6V
- High Speed Operation : t_{pd} = 3.5 ns (max) at V_{CC} = 3.0~3.6 V
  : t_{pd} = 4.4 ns (max) at V_{CC} = 2.3~2.7 V
  : t_{pd} = 8.8 ns (max) at V_{CC} = 1.8 V
- 3.6V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ±24 mA (min) at V_{CC} = 3.0 V
  : I_{OH} / I_{OL} = ±18 mA (min) at V_{CC} = 2.3 V
  : I_{OH} / I_{OL} = ±6 mA (min) at V_{CC} = 1.8 V
- Latch-up Performance : ±300 mA
- ESD Performance : Human Body Model > ±2000 V
  : Machine Model > ±200 V
- Package : TSSOP
  (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 1)

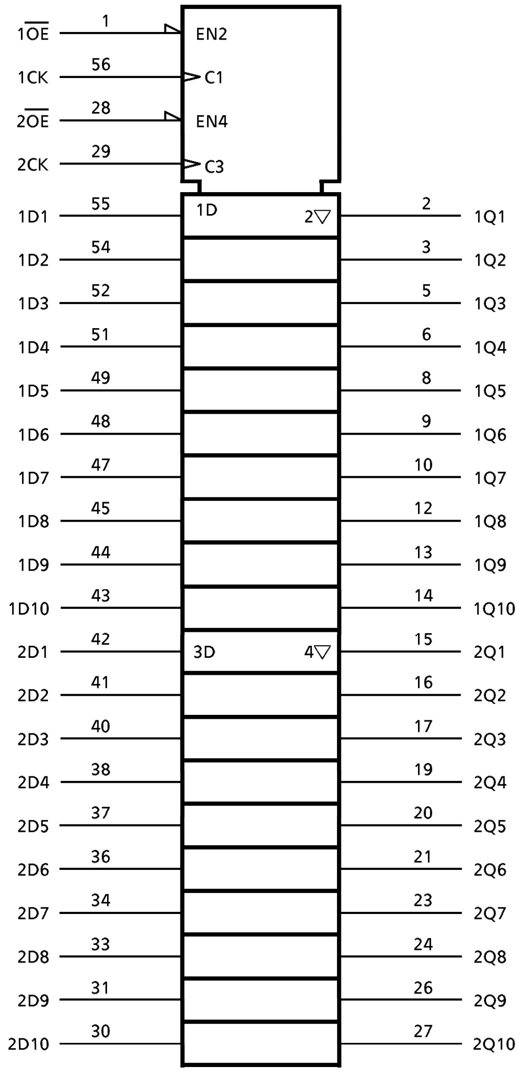
(Note 1) : To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



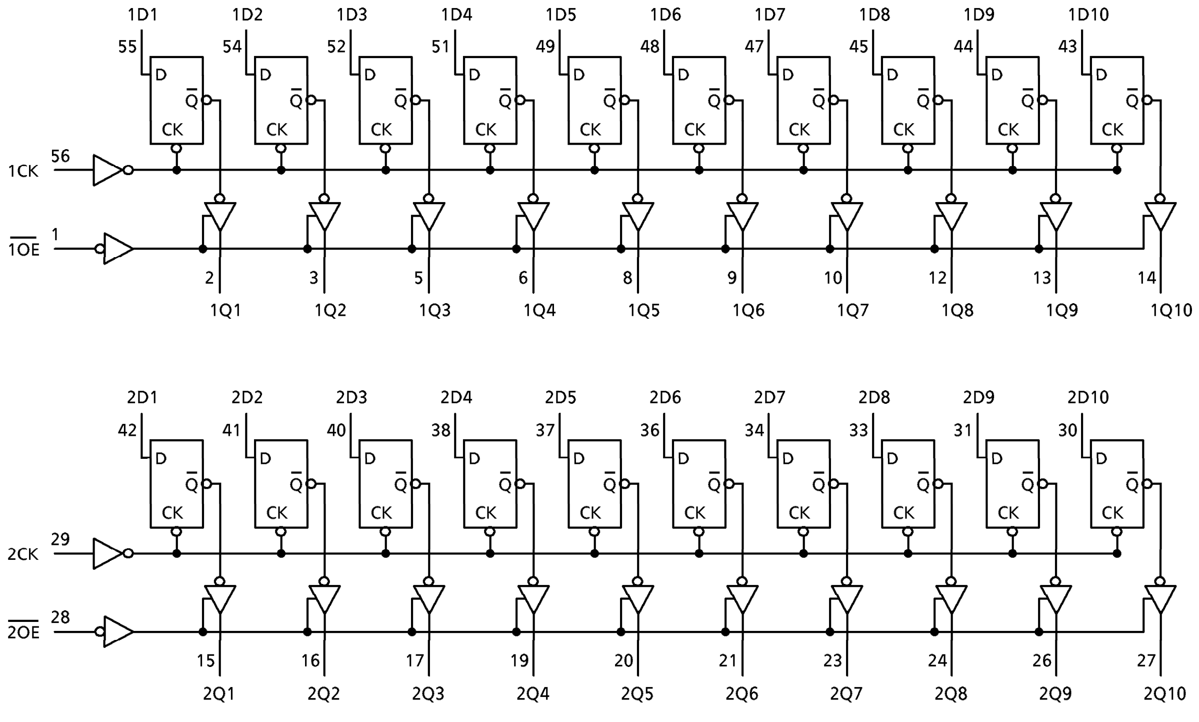
TRUTH TABLE

INPUT			OUTPUT
$\overline{1OE}$	1CK	1D1-1D10	1Q1-1Q10
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

INPUT			OUTPUT
$\overline{2OE}$	2CK	2D1-2D10	2Q1-2Q10
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High impedance
Qn : No change

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	−0.5~4.6	V
DC Input Voltage	V_{IN}	−0.5~4.6	V
DC Output Voltage	V_{OUT}	−0.5~4.6 (Note 1)	V
		−0.5~V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	400	mW
DC V_{CC}/Ground Current Per Supply Pin	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) : Off-State
(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage	V_{IN}	−0.3~3.6	V
Output Voltage	V_{OUT}	0~3.6 (Note 5)	V
		0~V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	±24 (Note 7)	mA
		±18 (Note 8)	
		±6 (Note 9)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns/V

(Note 4) : Data Retention Only
(Note 5) : Off-State
(Note 6) : High or Low State
(Note 7) : V_{CC} = 3.0~3.6 V
(Note 8) : V_{CC} = 2.3~2.7 V
(Note 9) : V_{CC} = 1.8 V
(Note 10) : V_{IN} = 0.8~2.0 V, V_{CC} = 3.0 V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C, 2.7 V < V_{CC} ≦ 3.6 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7~3.6	V_{CC} − 0.2	—	V
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7~3.6	—	0.2	V
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 18 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		2.7~3.6	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.7~3.6	—	±20.0	
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7~3.6	—	750	μA

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C, 2.3 V ≦ V_{CC} ≦ 2.7 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			2.3~2.7	1.6	—	V
	"L" Level	V_{IL}			2.3~2.7	—	0.7	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.3~2.7	V_{CC} − 0.2	—	V
				I_{OH} = −6 mA	2.3	2.0	—	
				I_{OH} = −12 mA	2.3	1.8	—	
				I_{OH} = −18 mA	2.3	1.7	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3~2.7	—	0.2	V
				I_{OL} = 12 mA	2.3	—	0.4	
				I_{OL} = 18 mA	2.3	—	0.6	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		2.3~2.7	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0~3.6 V		2.3~2.7	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.3~2.7	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.3~2.7	—	±20.0	

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C, 1.8 V ≦ V_{CC} < 2.3 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			1.8~2.3	0.7 × V_{CC}	—	V
	"L" Level	V_{IL}			1.8~2.3	—	0.2 × V_{CC}	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	1.8	V_{CC} −0.2	—	V
				I_{OH} = −6 mA	1.8	1.4	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.8	—	0.2	V
				I_{OL} = 6 mA	1.8	—	0.3	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		1.8	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		1.8	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		1.8	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		1.8	—	±20.0	

AC characteristics (Ta = −40~85°C, Input t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN	MAX	UNIT
Maximum Clock Frequency	f_{MAX}	(Fig.1, 2)	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}	(Fig.1, 2)	1.8	1.5	8.8	ns
			2.5 ± 0.2	1.0	4.4	
			3.3 ± 0.3	0.8	3.5	
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 3)	1.8	1.5	9.8	ns
			2.5 ± 0.2	1.0	4.7	
			3.3 ± 0.3	0.8	3.7	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 3)	1.8	1.5	7.6	ns
			2.5 ± 0.2	1.0	4.2	
			3.3 ± 0.3	0.8	3.7	
Minimum Pulse Width (CK)	t_{W} (H) t_{W} (L)	(Fig.1, 2)	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Set-up Time	t_s	(Fig.1, 2)	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Hold Time	t_h	(Fig.1, 2)	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic switching characteristics (Ta = 25°C, Input $t_r = t_f = 2.0$ ns, $C_L = 30$ pF)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 12)	1.8	0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 12)	2.5	0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 12)	3.3	0.8	
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 12)	1.8	−0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 12)	2.5	−0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 12)	3.3	−0.8	
Quiet Output Minimum Dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 12)	1.8	1.5	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 12)	2.5	1.9	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 12)	3.3	2.2	

(Note 12) : Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

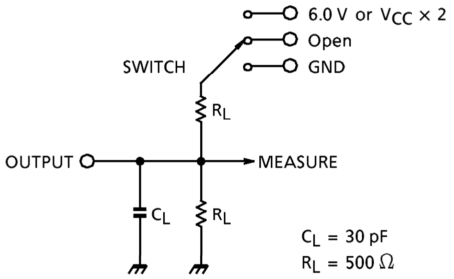
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Input Capacitance	C_{IN}		1.8, 2.5, 3.3	6	pF
Output Capacitance	C_O		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10 MHz (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 20$ (per bit)

TEST CIRCUIT

Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @V_{CC} = 3.3 ± 0.3 V V_{CC} × 2 @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}, t_w, t_s, t_h

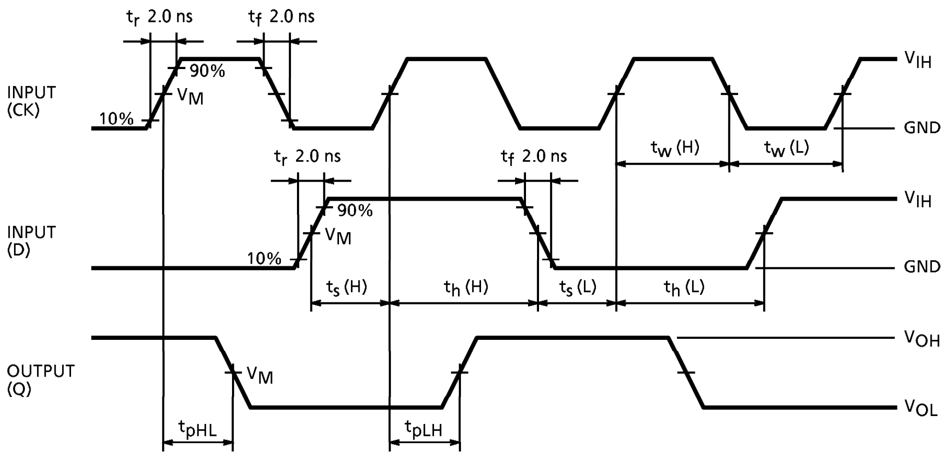
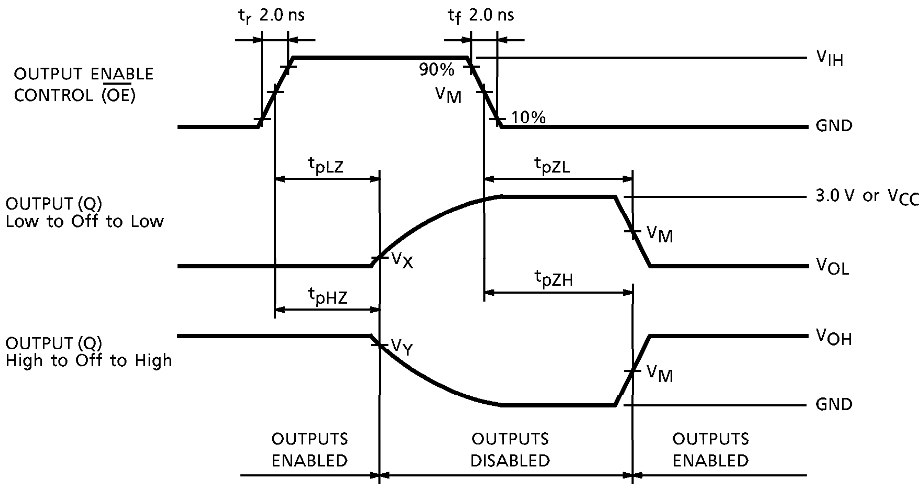


Fig.3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

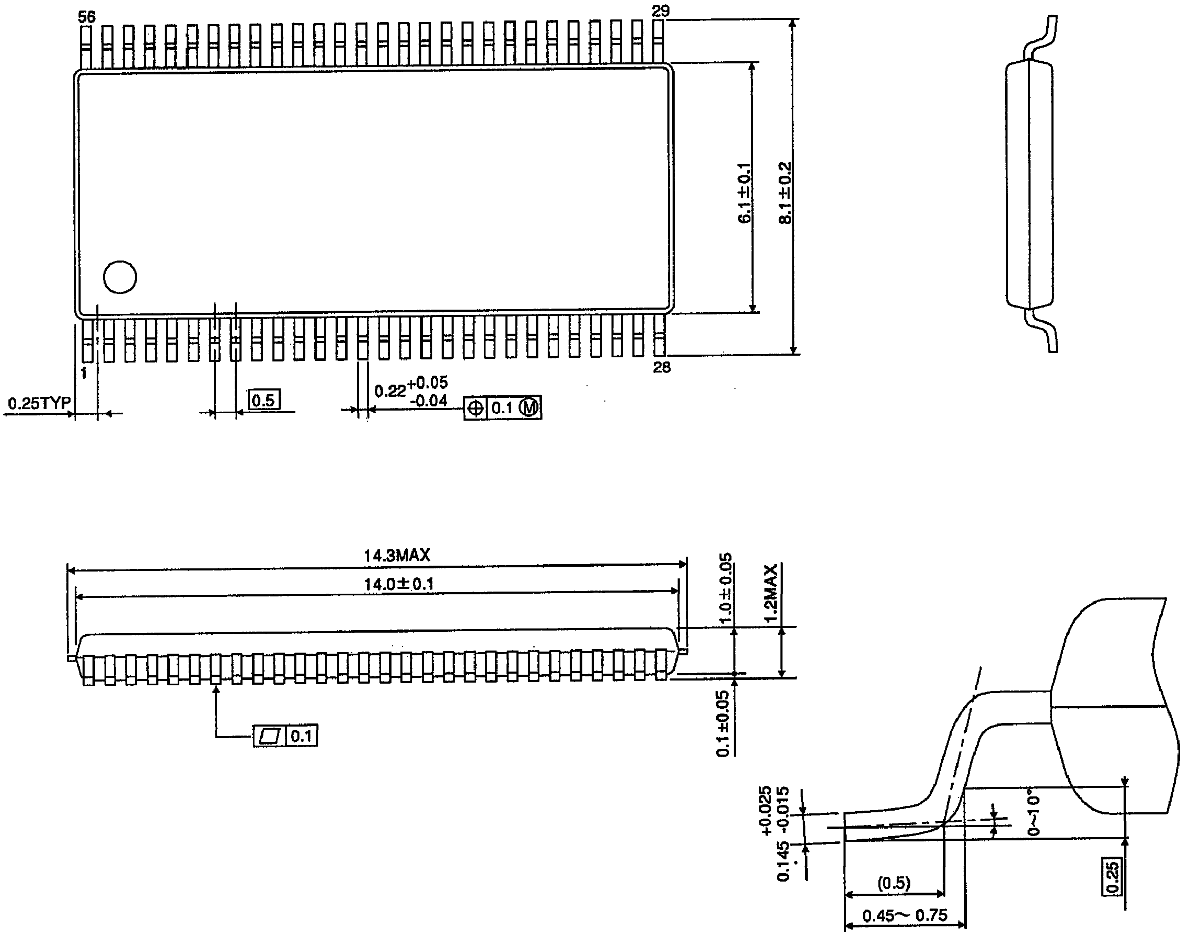


SYMBOL	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	V_{CC} / 2	V_{CC} / 2
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

PACKAGE DIMENSIONS

TSSOP56-P-0061-0.50

Unit : mm



Weight : 0.25 g (Typ.)