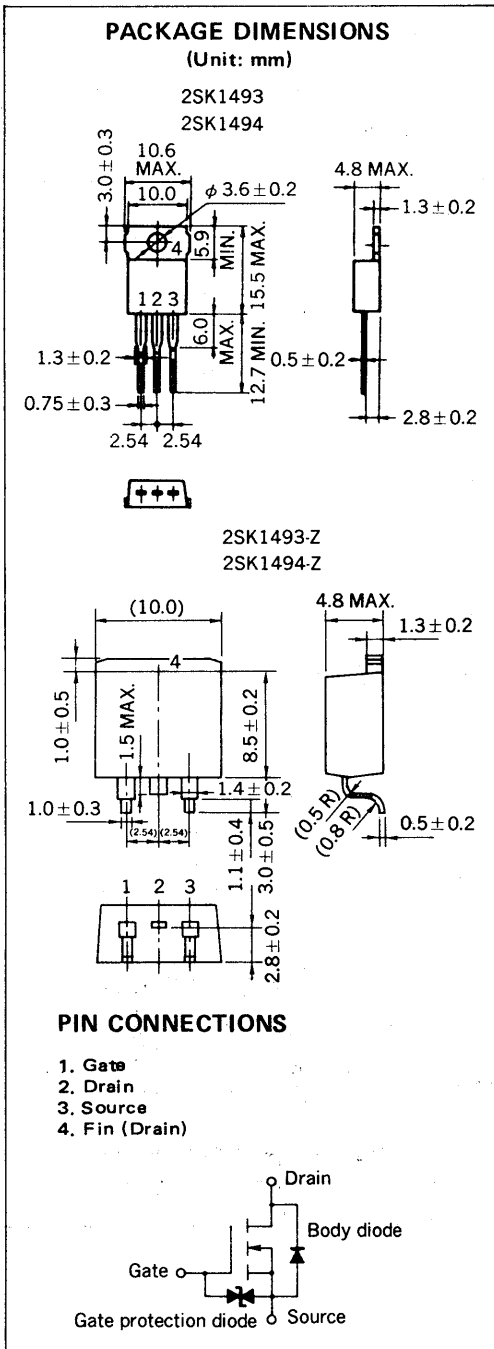


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P1 98.2

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTORS
 2SK1493, 2SK1493-Z/2SK1494, 2SK1494-Z

SWITCHING N-CHANNEL POWER MOS FET
 INDUSTRIAL USE



DESCRIPTION

The 2SK1495/2SK1496 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 2.8 \Omega \text{ MAX.}/3.0 \Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$)
- Low C_{iss} $C_{iss} = 350 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	T_{stg}	-55 to +150	°C
Channel Temperature	T_c	150	°C MAX.

Maximum power Dissipation

Total Power Dissipation ($T_A = 25 \text{ °C}$)	P_T	50	W
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Maximum Voltages and Currents ($T_A = 25 \text{ °C}$)

Drain to Source Voltage	V_{DSS}	450/500	V
(2SK1493/2SK1494)			
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±3	A
Drain Current (pulse)	$I_{D(pulse)}^*$	±12	A

* $PW \leq 10 \mu s, \text{ Duty Cycle} \leq 1 \%$

Maximum Avalanche Capability Ratings**

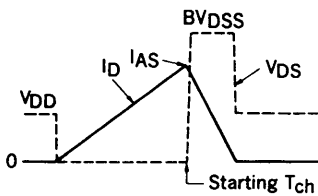
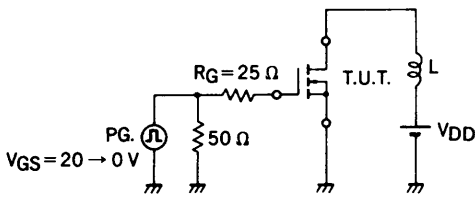
Single Avalanche Current	I_{AS}	4.5	A
Single Avalanche Energy	E_{AS}	57	mJ

** Starting $T_{ch} = 25 \text{ °C}, R_G = 25 \Omega, V_{GS} = 20 \text{ V} \rightarrow 0$

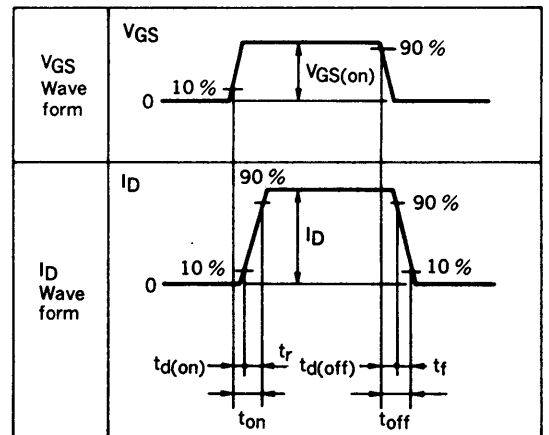
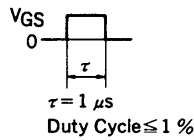
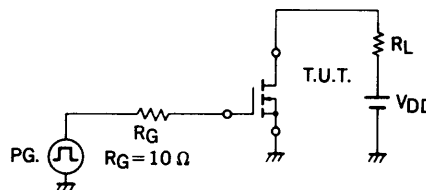
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1493/2SK1494)	R _{DS(on)}		2.2	2.8	Ω	V _{GS} = 10 V, I _D = 2 A
			2.4	3.0	Ω	
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	1.0			S	V _{DS} = 10 V, I _D = 2 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 450 V/500 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		350		pF	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz
Output Capacitance	C _{oss}		120		pF	
Reverse Transfer Capacitance	C _{rss}		45		pF	
Turn-On Delay Time	t _{d(on)}		5		ns	V _{GS} = 10 V, V _{DD} = 150 V, I _D = 2 A, R _G = 10 Ω, R _L = 75 Ω
Rise Time	t _r		10		ns	
Turn-Off Delay Time	t _{d(off)}		30		ns	
Fall Time	t _f		15		ns	
Total Gate Charge	Q _G		12		nC	V _{GS} = 10 V, I _D = 3 A, V _{DD} = 400 V
Gate to Source Charge	Q _{GS}		3		nC	
Gate to Drain Charge	Q _{GD}		7		nC	
Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 3 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		310		ns	I _F = 3 A, di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		1.2		μC	

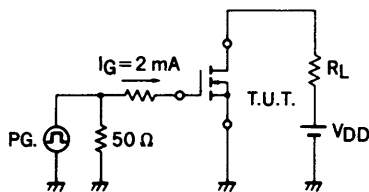
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

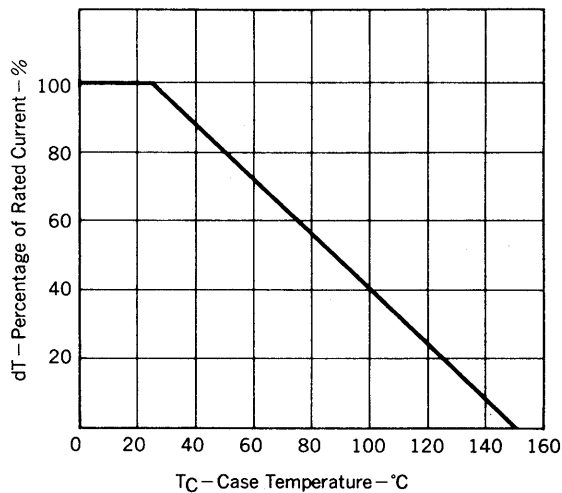


Test Circuit 3: Gate Charge

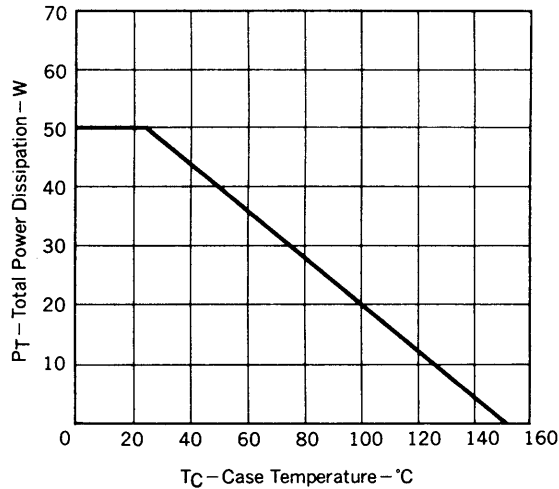


TYPICAL CHARACTERISTICS (T_A = 25 °C)

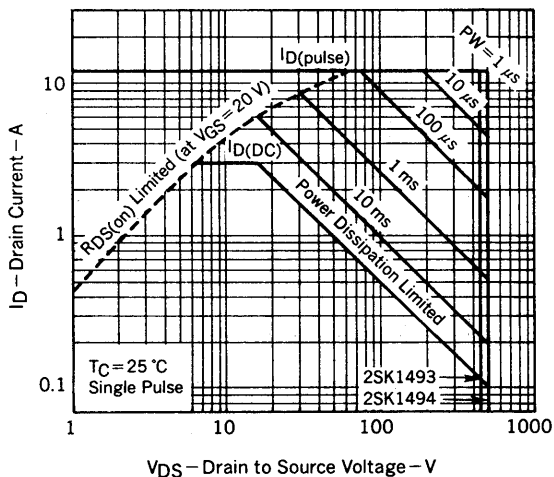
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



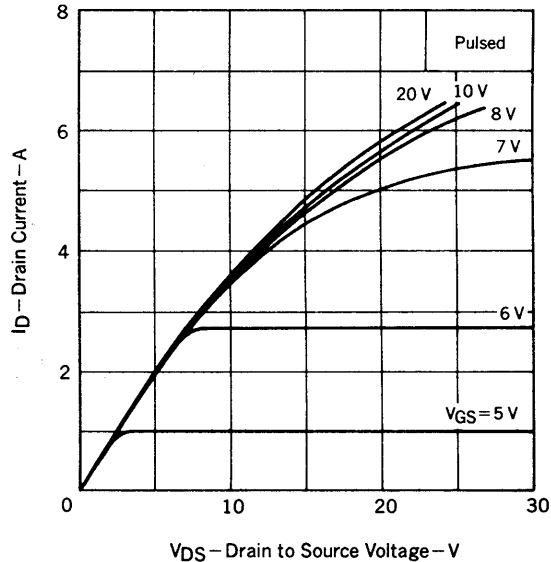
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



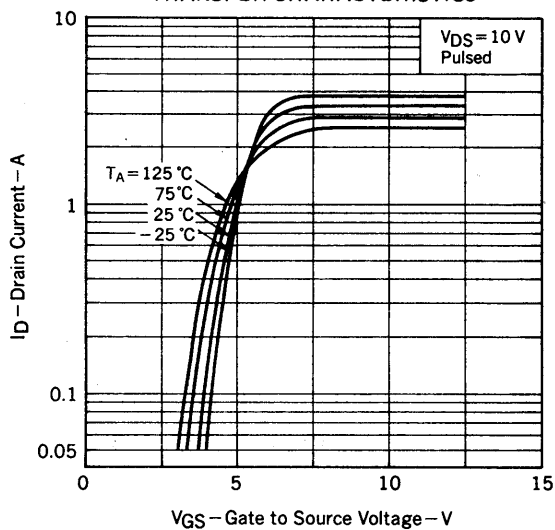
FORWARD BIAS SAFE OPERATING AREA

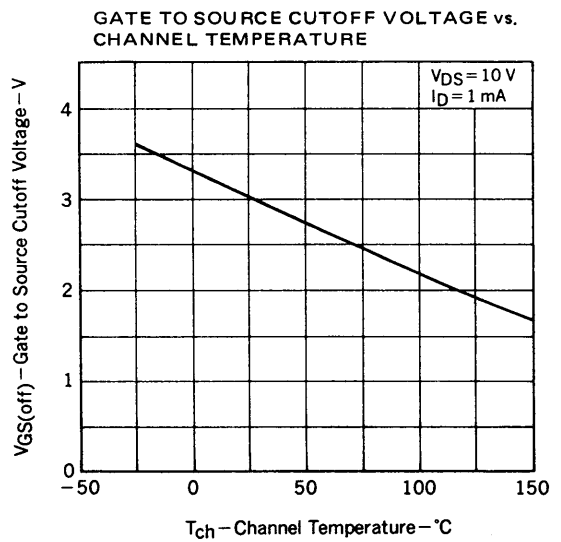
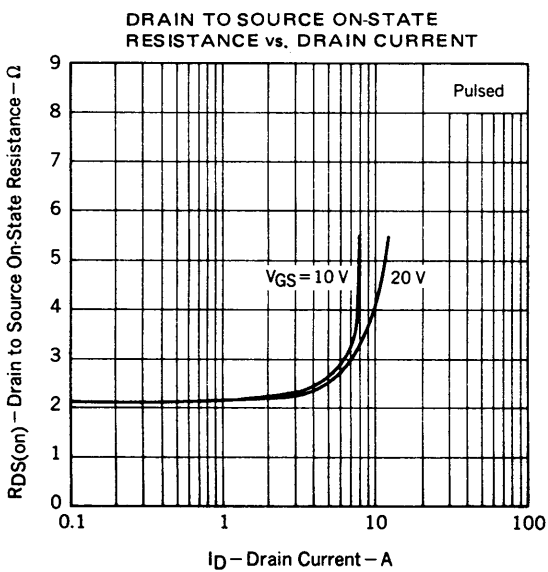
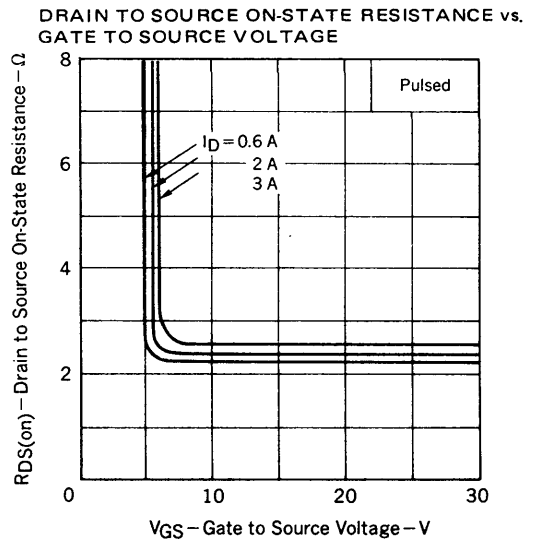
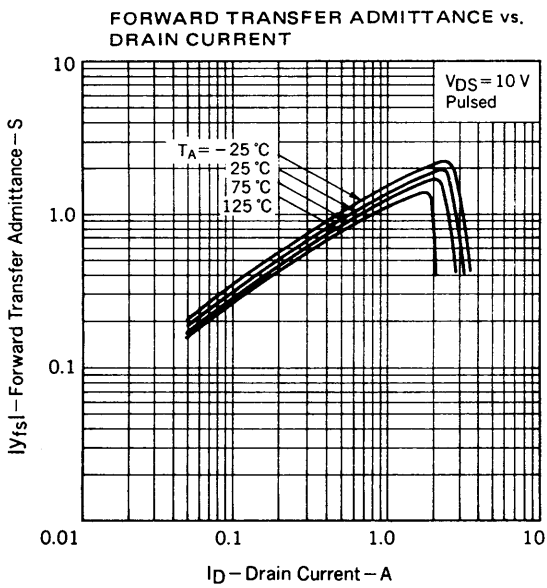
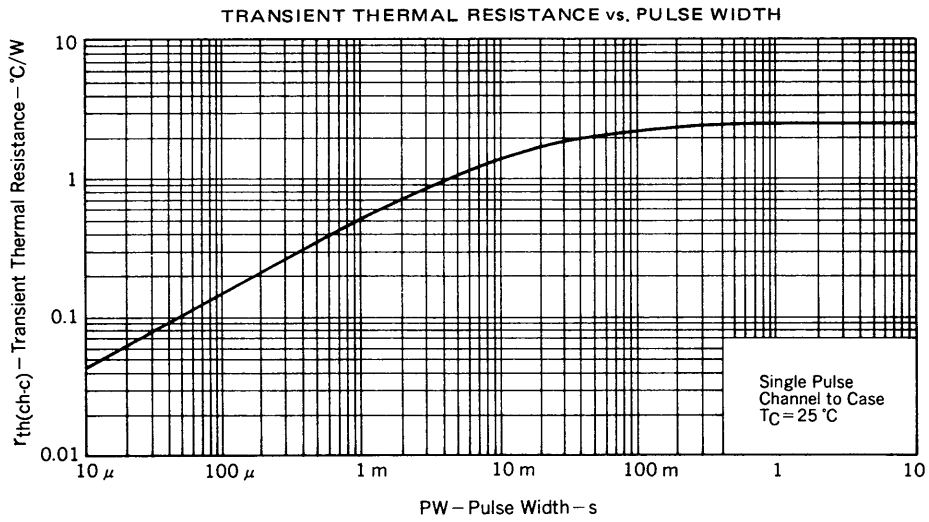


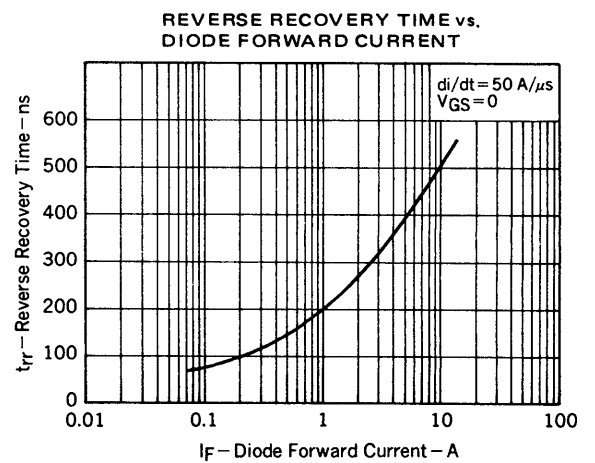
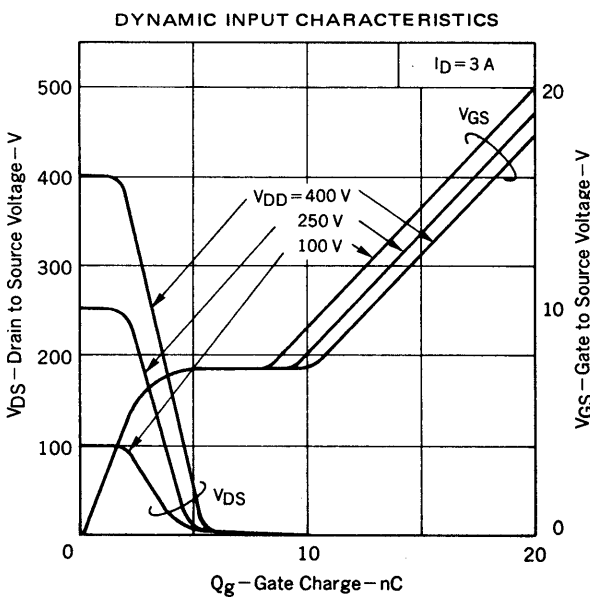
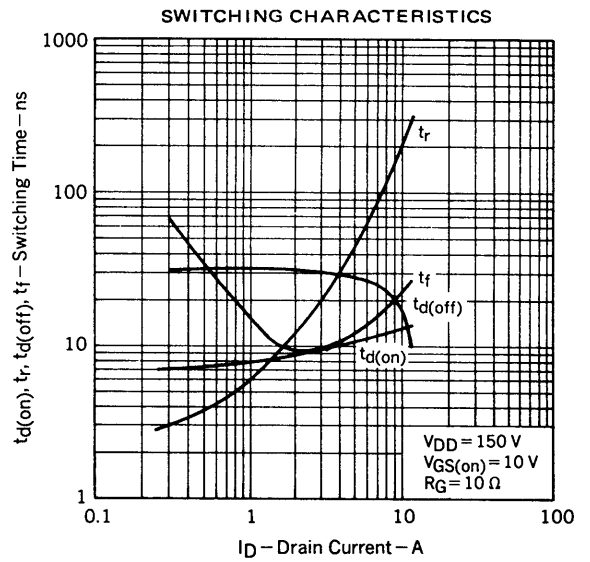
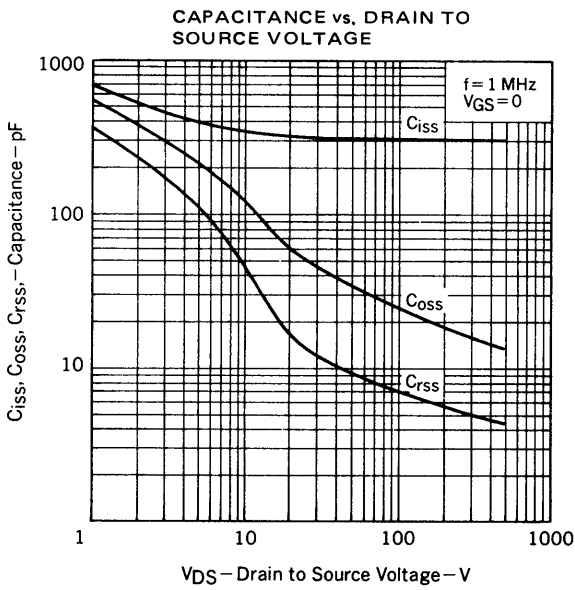
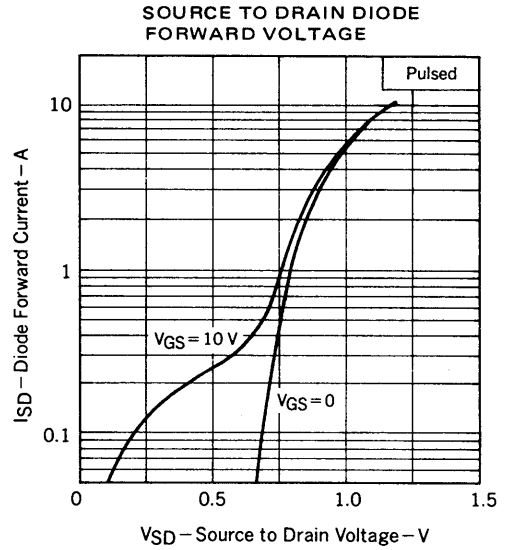
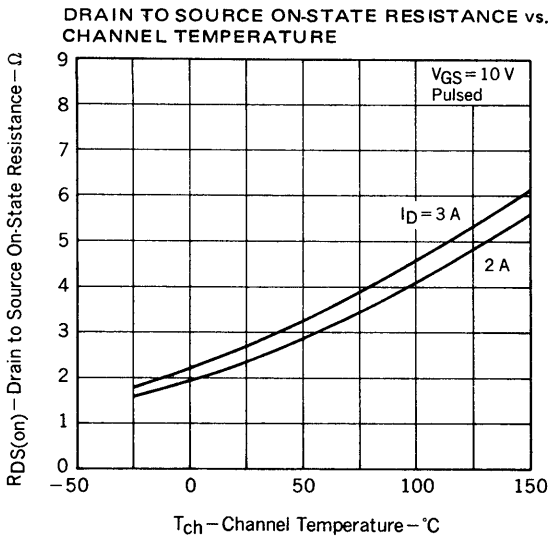
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

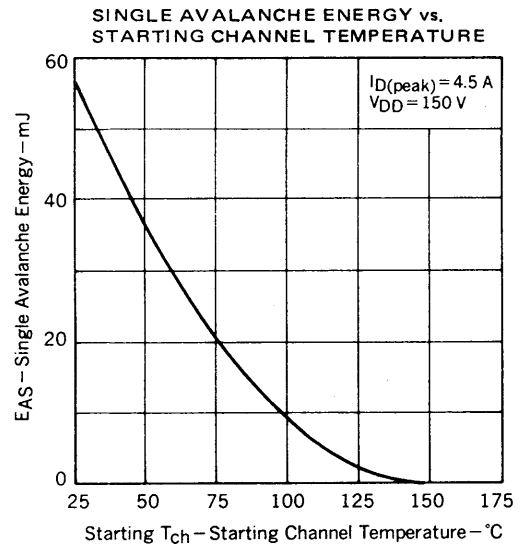
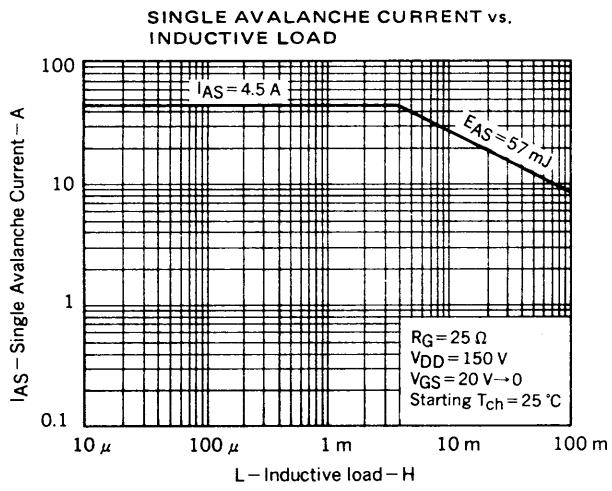


TRANSFER CHARACTERISTICS









REFERENCE

Application note name	No.
Guide to quality assurance for semiconductor device	MEI-1202
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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