![ANALOG DEVICES]

2 GHz Ultralow Distortion Differential RF/IF Amplifier

Preliminary Technical Data

AD8352

FEATURES

- −3 dB bandwidth of 2.0 GHz (Av = 10 dB)
  - Slew rate 11 V/ns
  - Single resistor gain adjust 0 dB ≤ Av ≤ 24 dB
  - Single resistor and capacitor distortion adjust
  - Input resistance 3kΩ , independent of gain
  - Differential or single-ended input
  - Low noise input stage 2.6 nV/√Hz RTI @ A_V = 10 dB
  - Low distortion
- 19 MHz: −87dBc HD2, −90dBc HD3
- 71 MHz: −84dBc HD2, −84dBc HD3
- 180 MHz: −81dBc HD2, −80dBc HD3
  - OIP3 of 41 dBm to 180 MHz @ 2 V p-p out
  - Fast settling and overdrive recovery
  - Single-supply operation: 3 V to 5.0 V
  - Low power dissipation 37 mA @ 5 V
  - Power down capability 4 mA @ 5 V
  - Fabricated on the XFCB3 process

APPLICATIONS

- Differential ADC driver
  - Single-ended to differential conversion
  - RF/IF gain blocks
  - SAW filter interfacing

FUNCTIONAL BLOCK DIAGRAM

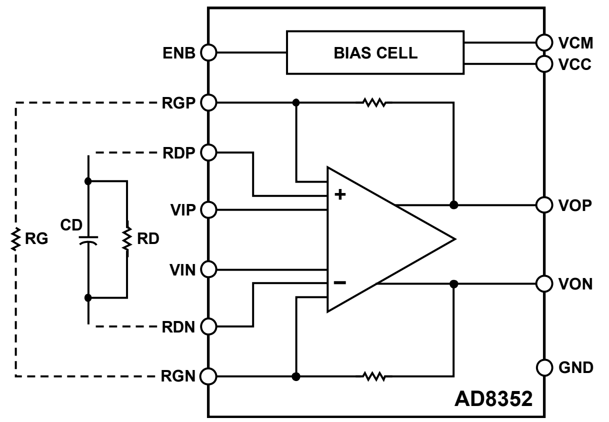

Figure 1.

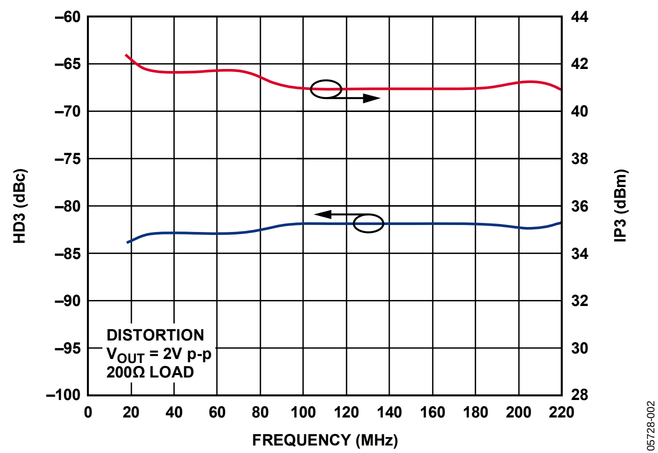

Figure 2. IP3 and Third Harmonic Distortion vs. Frequency

GENERAL DESCRIPTION

The AD8352 is a high performance differential amplifier for RF and IF applications to 500 MHz. It achieves 80 db SFDR at frequencies up to 180 MHz making it an ideal driver for high speed 14- and 16-bit A/D converters.

Unlike other wideband differential amplifiers, the AD8352 has buffers that isolate the gain setting resistor (RG) from the signal inputs. As a result, the AD8352 maintains a constant 3 kΩ input resistance for gains of 0 dB to 24 dB easing matching and input drive requirements. The AD8352 has a nominal 100 Ω differential output resistance. The device is optimized for wide band, low distortion performance at frequencies beyond 500 MHz. These attributes, together with its wide gain adjust capability, make this device the amplifier of choice for general purpose IF and broadband applications where low distortion, noise, and power are critical. In particular, it is ideally suited for driving A/D converters (up to 16 bits), mixers, pin diode attenuators, and multielement discrete and SAW filters. The device comes in a compact 3 mm × 3 mm, 16-pin LFCSP package and operates over a temperature range of –40°C to +85°C.

Rev. PrA

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REVISION HISTORY

10/05—Revision PrA: Preliminary Version

SPECIFICATIONS

V_S = 5 V, R_L=200 Ω differential, RG=100 Ω (A_V = 10 dB), *f* = 100 MHz, T = 25°C; parameters specified differentially, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	Gain = 6 dB, V_{OUT} ≤ 1.0 V p-p		2,200		MHz
	Gain = 12 dB, V_{OUT} ≤ 1.0 V p-p		1,400		MHz
	Gain = 18 dB, V_{OUT} ≤ 1.0 V p-p		1,400		MHz
Bandwidth for 0.2 dB Flatness	6 dB ≤ gain ≤ 12 dB, V_{OUT} ≤ 1.0 V p-p		300		MHz
Gain Accuracy	Using 1% resistor for RG, 0 dB ≤ A_V ≤ 20 dB		TBD		dB
Gain Supply Sensitivity	V_S ± 5%		TBD		dB/V
Gain Temperature Sensitivity	−40°C to +85°C		TBD		mdB/°C
Slew Rate	R_L = 1 kΩ, V_{OUT} = 2 V step		11		V/ns
	R_L = 200 Ω, V_{OUT} = 2 V step		TBD		V/ns
Settling Time	1 V step to 1%		<3		ns
Overdrive Recovery Time	V_{IN} = 4 V to 0 V step, V_{OUT} ≤ ±10 mV		<2		ns
Reverse Isolation (S12)			TBD		dB
INPUT/OUTPUT CHARACTERISTICS					
Common Mode Nominal			VCC/2		V
Voltage Adjustment Range			1.2 to 3.8		V
Maximum Output Voltage Swing	1 dB compressed		6		V p-p
Output Common-Mode Offset	Referenced to VCC/2		−60		mV
Output Common-Mode Drift	−40°C to +85°C		TBD		mV/°C
Output Differential Offset Voltage			±20		mV
CMRR			TBD		dB
Output Differential Offset Drift	−40°C to +85°C		TBD		mV/°C
Input Bias Current			−5		µA
Input Resistance			3		kΩ
Input Capacitance Single-Ended			0.9		pF
Output Resistance			100		Ω
Output Capacitance			3		pF
POWER INTERFACE					
Supply Voltage		3	5	5.5	V
ENB Threshold			1.5		V
ENB Input Bias Current	ENB 3 V		100		µA
	ENB at 0.6 V		220		µA
Quiescent Current	ENB at 3 V		37	TBD	mA
	ENB at 0.6 V		4.5		mA

NOISE DISTORTION SPECIFICATIONS

V_S = 5 V, R_L=200 Ω differential, RG=100 Ω (A_V = 10 dB), T = 25°C; parameters specified differentially, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
19 MHz					
2nd/3rd Harmonic Distortion[1]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		87/90		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		83/84		dBc
Third-Order IMD	R_L = 1 kΩ, f_1 = 9.5 MHz, f_2 = 10.5 MHz, V_{OUT} = 2 V p-p composite		92/87		dBc
	R_L = 200 Ω, f_1 = 9.5 MHz, f_2 = 10.5 MHz, V_{OUT} = 2 V p-p composite		84		dBc
Output Third-Order Intercept			42		dBm
Noise Spectral Density (RTI)			2.6		nV/√Hz
1 dB Compression Point			13		dBm
71 MHz					
2nd/3rd Harmonic Distortion[1]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		84/84		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		83/83		dBc
Third-Order IMD	R_L = 1 kΩ, f_1 = 69.5 MHz, f_2 = 70.5 MHz, V_{OUT} = 2 V p-p composite		TBD		dBc
	R_L = 200 Ω, f_1 = 69.5 MHz, f_2 = 70.5 MHz, V_{OUT} = 2 V p-p composite		85		dBc
Output Third-Order Intercept	f_1 = 69.5 MHz, f_2 = 70.5 MHz @ R_L = 200 Ω		41		dBm
Noise Spectral Density (RTI)			2.6		nV/√Hz
1 dB Compression Point			13		dBm
100 MHz					
2nd/3rd Harmonic Distortion	R_L = 1 kΩ, V_{OUT} = 2 V p-p		83/82		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		80/82		dBc
Third-Order IMD	R_L = 1 kΩ, f_1 = 139.5 MHz, f_2 = 140.5 MHz, V_{OUT} = 2 V p-p composite		TBD		dBc
	R_L = 200 Ω, f_1 = 100 MHz, f_2 = 98 MHz, V_{OUT} = 2 V p-p composite		86		dBc
Output Third-Order Intercept	f_1 = 100 MHz, f2 = 98 MHz		41		dBm
Noise Spectral Density (RTI)			2.6		nV/√Hz
1 dB Compression Point			13		dBm
180 MHz					
2nd/3rd Harmonic Distortion[2]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		81/82		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		79/82		dBc
Third-Order IMD	R_L = 1 kΩ, f_1 = 239.5 MHz, f_2 = 240.5 MHz, V_{OUT} = 2 V p-p composite		TBD		dBc
	R_L = 200 Ω, f_1 = 239.5 MHz, f_2 = 240.5 MHz, V_{OUT} = 2 V p-p composite		82		dBc
Output Third-Order Intercept	f_1 = 179 MHz, f_2 = 180 MHz	3	40	5.5	dBm
Noise Spectral Density (RTI)			2.6		nV/√Hz
1 dB Compression Point			13		dBm

[1] When using the evaluation board at frequencies below 50 MHz, replace the Output Balun T1 with a transformer such as Mini Circuits ADT1-1WT to obtain low frequency balance required for differential HD2 cancellation.
[2] CD and RD can be optimized for broadband operation below 180 MHz. For operation above 300 MHz, CD and RD components are not required.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage VCC	5.5 V
Internal Power Dissipation	TBD
θ_{JA}[1]	TBD
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] See Applications section for single-ended to differential performance.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

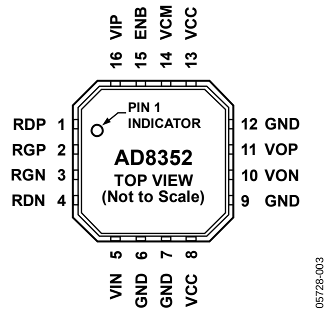

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RDP	Positive Distortion Adjust.
2	RGP	Positive Gain Adjust.
3	RGN	Negative Gain Adjust.
4	RDN	Negative Distortion Adjust.
5	VIN	Balanced Differential Input. Biased to VCM, typically ac-coupled.
6, 7, 9, 12	GND	Ground. Connect to low impedence GND.
8, 13	VCC	Positive Supply.
10	VON	Balanced Differential Output. Biased to VCM, typically ac-coupled.
11	VOP	Balanced Differential Output. Biased to VCM, typically ac-coupled.
14	VCM	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the input and output. Typically decoupled to ground with a 0.1 µF capacitor. With no reference applied, input and output common mode floats to midsupply = VCC/2.
15	ENB	Enable. Apply positive voltage (1.3 V < ENB < VCC) to activate device.
16	VIP	Balanced Differential Input. Biased to VCM, typically ac-coupled.

TYPICAL PERFORMANCE CHARACTERISTICS

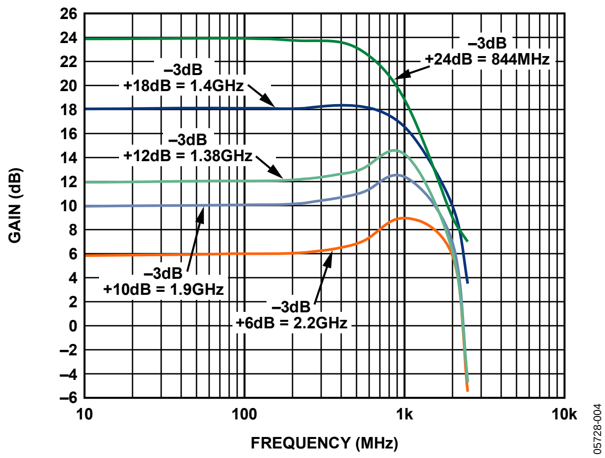

Figure 4. Gain vs. Frequency for a 200 Ω Differential Load (A_V = 24, 18, 12, 10, and 6 dB)

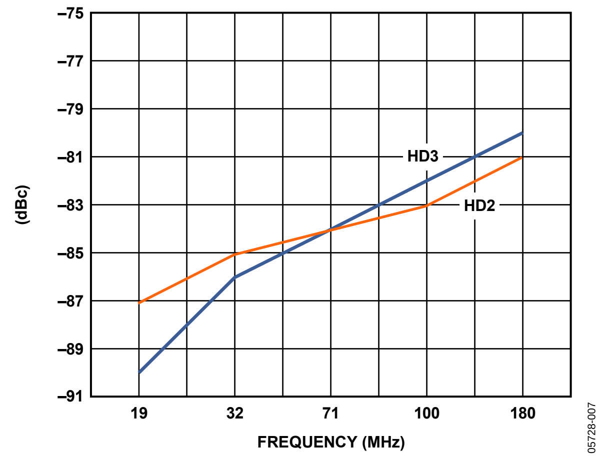

Figure 7. Harmonic Distortion vs. Frequency for 2 V p-p into R_L =1 kΩ (A_V = 10 dB, 5 V Supply) RG = 160 Ω, RD = 6.8 kΩ, CD = 0.1 pF

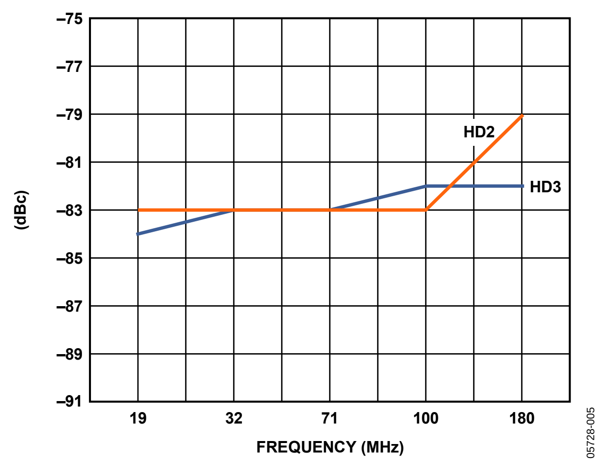

Figure 5. Harmonic Distortion vs. Frequency for 2 V p-p into R_L = 200 Ω (A_V = 10 dB, 5 V Supply) RG = 100 Ω, RD = 4.3 kΩ, CD = 0.3 pF

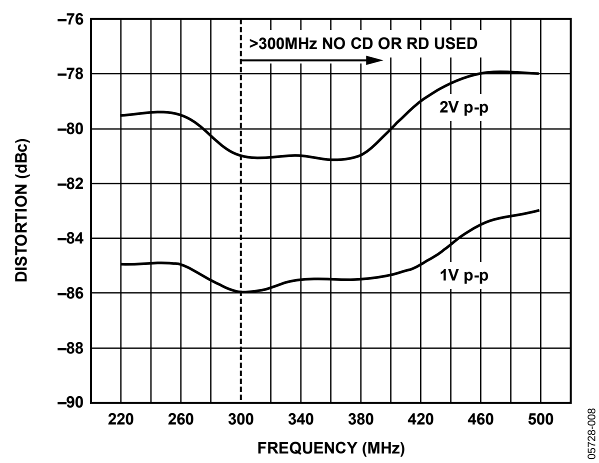

Figure 8. Second-Order Harmonic Distortion HD2 vs. Frequency (A_V = 10 dB, 5 V Supply)

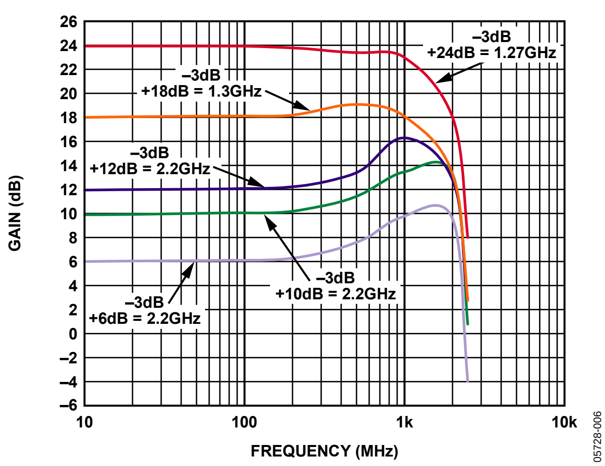

Figure 6. Gain vs. Frequency for a 1 kΩ Differential Load (A_V = 24, 18, 12, 10, and 6 dB)

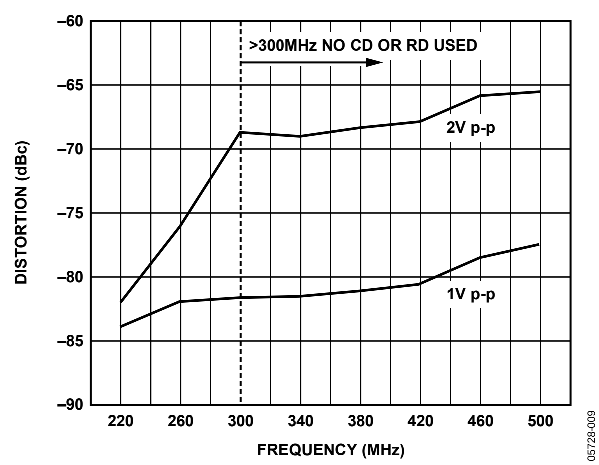

Figure 9. Third-Order Harmonic Distortion HD3 vs. Frequency (A_V = 10 dB, 5 V Supply)

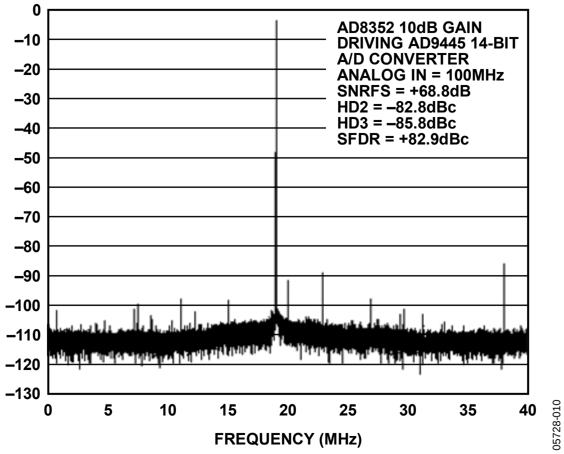

Figure 10. Single Tone Distortion AD8352 Driving AD9445 (A_V = 10 dB). See Figure 12.

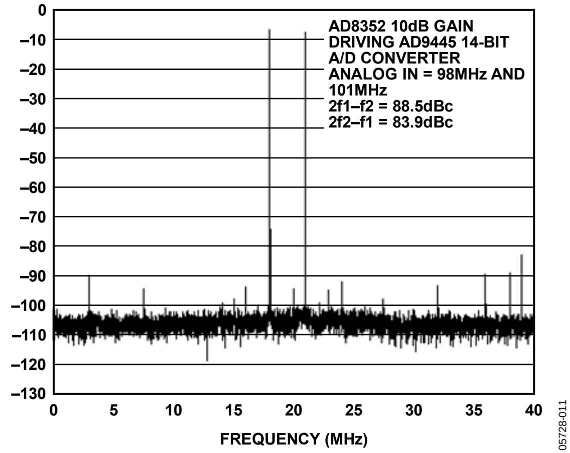

Figure 11. Two Tone Distortion AD8352 Driving AD9445 (A_V = 10 dB) Analog In = 98 MHz and 101 MHz. See Figure 12.

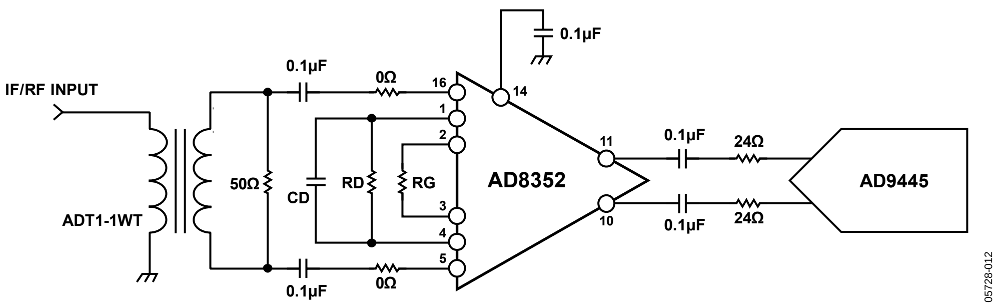

Figure 12. External Circuit Configuration for Distortion Tests. See Figure 10 and Figure 11.

APPLICATIONS

GAIN DISTORTION AND ADJUSTMENT

Broadband selection of RG, CD, and RD for the AD8352 is optimized at frequencies of 180 MHz. These selections are listed at a 200 Ω load in Table 5 and a 1 kΩ load in Table 6. Figure 13 through Figure 16 show the plots for the RG and CD selections at the 200 Ω and 1 kΩ loads, respectively.

Table 5. Broadband Selection of RG, CD, and RD: 200 Ω Load

Gain	RG	CD	RD
3 dB	390 Ω	0 pF	6.8 kΩ
6 dB	210 Ω	0.1 pF	4.3 kΩ
9 dB	120 Ω	0.2 pF	4.3 kΩ
12 dB	82 Ω	0.4 pF	4.3 kΩ
15 dB	51 Ω	0.7 pF	4.3 kΩ
18 dB	30 Ω	1 pF	4.3 kΩ

Table 6. Broadband Selection of RG, CD, and RD: 1 kΩ Load

Gain	RG	CD	RD
3 dB	680 Ω	0 pF	6.8 kΩ
6 dB	330 Ω	0 pF	6.8 kΩ
9 dB	190 Ω	0.1 pF	6.8 kΩ
12 dB	120 Ω	0.25 pF	6.8 kΩ
15 dB	75 Ω	0.5 pF	6.8 kΩ
18 dB	51 Ω	0.7 pF	6.8 kΩ

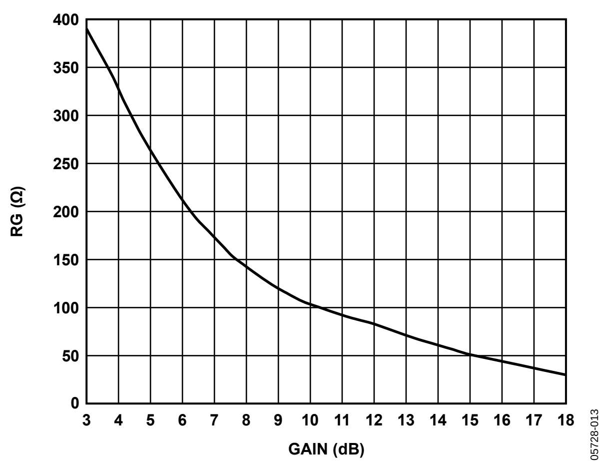

Figure 13. RG vs. Gain, R_L = 200 Ω

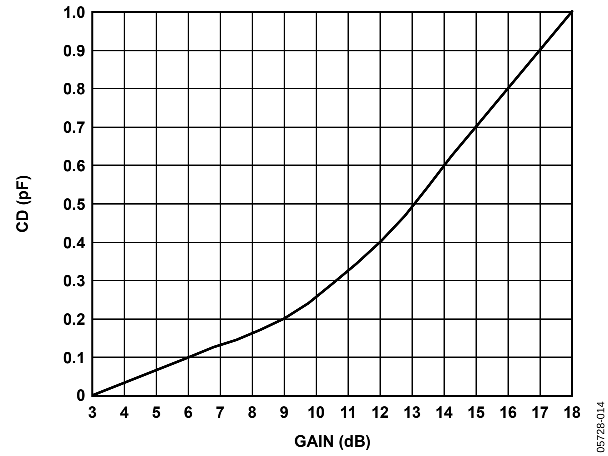

Figure 14. CD vs. Gain, R_L = 200 Ω

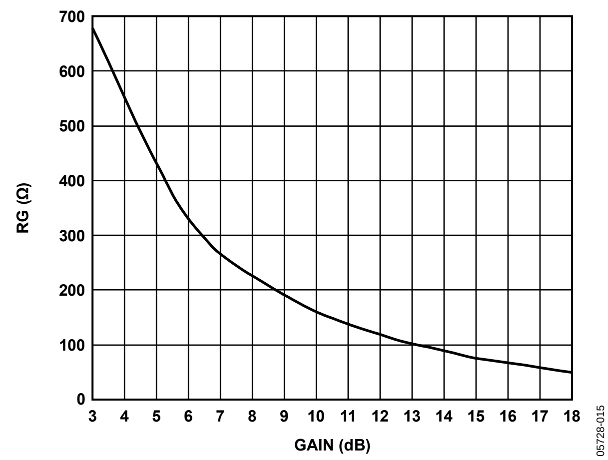

Figure 15. RG vs. Gain, R_L = 1 kΩ

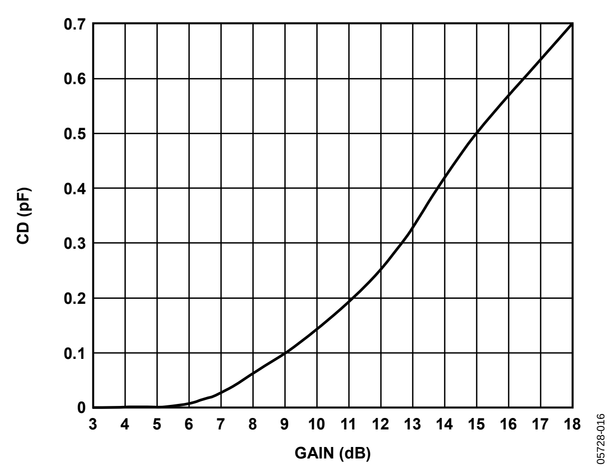

Figure 16. CD vs. Gain, R_L = 1 kΩ

SINGLE-ENDED INPUT TO DIFFERENTIAL OUTPUT OPERATION

The AD8352 can be configured as a single-ended to differential amplifier. To balance the outputs, when only driving the VIP input, an external resistor (RN) of 200 Ω is added between VIP and RGN. Using the gain vs. frequency graph shown in Figure 18, RG can be selected for the desired gain and load. The distortion cancellation selection components, RD and CD, can be determined for the gain and load required (see Table 7 and Table 8). This configuration provides –3dB bandwidths similar to differential drives see Figure 4 and Figure 6.

The distortion results (Figure 19 to Figure 22) were measured using a gain of 12 dB. Though not shown, the gains specified in Table 7 and Table 8 yield similar distortion results.

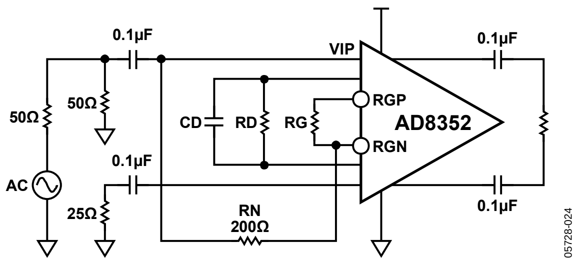

Figure 17. Single Ended Schematic

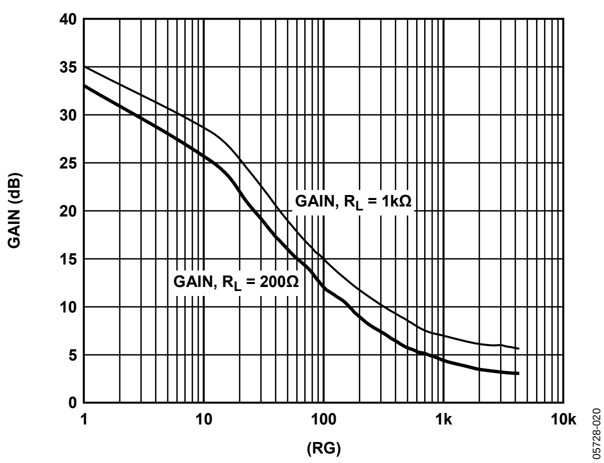

Figure 18. Gain vs. RG

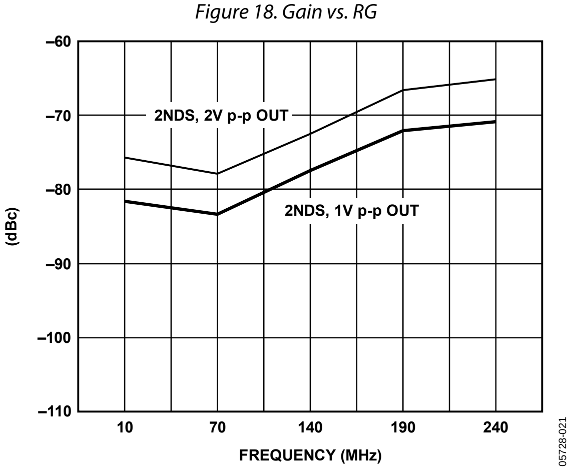

Figure 19. AD8352 Single-Ended Second-Order Harmonic Distortion 200 Ω Load

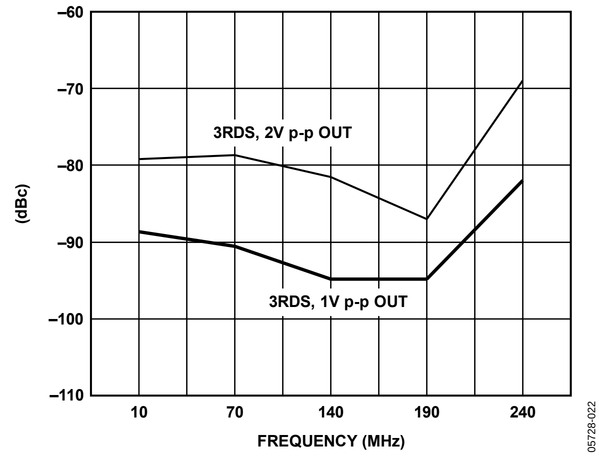

Figure 20. Single-Ended Third-Order Harmonic Distortion 200 Ω Load.

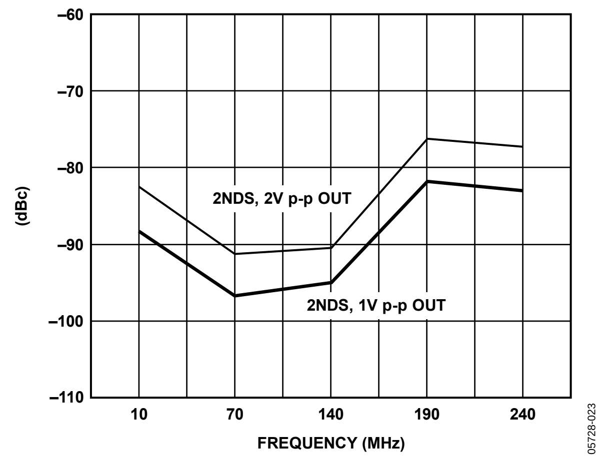

Figure 21. Single-Ended Second-Order Harmonic Distortion 1000 Ω Load

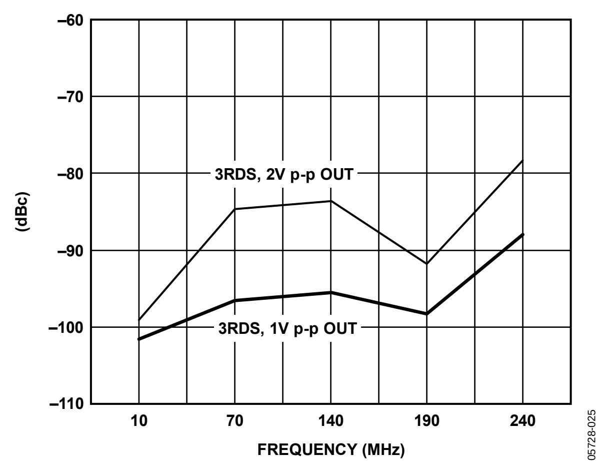

Figure 22. Single-Ended Third-Order Harmonic Distortion 1000 Ω Load

Table 7. Distortion Cancellation Selection Components RD and CD for Required Gain, 200 Ω Load

Gain (dB)	RG (Ω)	CD (pF)	RD (kΩ)
3	4.3 k	0	4.3
6	520	0	4.3
9	200	0.2	4.3
12	100	0.4	4.3
15	62	0.7	4.3
18	43	0.9	4.3

Table 8. Distortion Cancellation Selection Components RD and CD for Required Gain, 1000 kΩ Load

Gain (dB)	RG (Ω)	CD (pF)	RD (kΩ)
6	3 k	0	4.3
9	430	0	4.3
12	190	0.2	4.3
15	100	0.3	4.3
18	62	0.5	4.3

LOADING SCHEMES

The AD8352 is characterized with two loads representing the most common ADC input resistance. The loads chosen are 200 Ω and 1000 Ω. These loads are accomplished using a broad band resistive match. The loading can be changed via R8, R9, and R12 giving the flexibility to characterize the AD8352 for the load in any given application. These loads are inherently lossy and thus must be accounted for in overall gain/loss for the evaluation board. Measure the gain of the AD8352 with an oscilloscope using the following procedure:

1. Measure the peak to peak voltage at the input node (C2 or C3), and
2. Measure the peak to peak voltage at the out put node (C4 or C5), then
3. Compute gain using the formula

   $Gain = 20\log V_{OUT}/V_{IN}$

Table 9. Typical Values Used for 200 Ω and 1000 Ω Loads

Component	200 Ω Load	1000 Ω Load
R8	86.6	487
R9	57.6	51.1
R12	86.6	487

EVALUATION BOARD

An evaluation board is available for experimentation of various parameters such as gain, common mode level, and input and output network configurations can be modified through minor resistor changes. The schematic and evaluation board artwork are presented in Figure 23, Figure 24, and Figure 25.

Table 10. Evaluation Board Circuit Components and Functions

Component	Name	Function	Additional information
Pin 8 to Pin 13	VCC	Supply VCC = +5 V.	
Pin 6, Pin 7, Pin 9, Pin 12	GND	Connect to low impedance GND.	
Pin 14, C9	VCM, Capacitor	Common Mode Offset Pin. Allows for monitoring or adjustment of the output common-mode voltage. C9 is a bypass capacitor.	C9 = 0.1 µF
RD/CD	Distortion Tuning Components	Distortion Adjustment components. Allows for third-order distortion adjustment HD3.	Typically, both are open above 300 MHz. C_D = 0.3 pF, R_D = 4.3 kΩ (size 0402)
Pin 15, C8	ENB, Capacitor	Enable. Apply positive voltage (1.3 V < ENB < VCC) to activate device. Pull down to disable. Can be bypassed and float high (1.8 V) for on state. C8 is a bypass capacitor.	Floats to 1.8 V to maintain device in power-up mode. C8 = 0.1 µF
R1,R2, R3, R4, R5, R6, T2, C2, C3	Resistors, Transformer, Capacitors	Input Interface. R1 and R4 ground one side of the differential drive interface for single-ended applications. T2 is a 1-to-1 impedance ratio balun to transform a single-ended input into a balanced differential signal. R2 and R3 provide a differential 50 Ω input termination. R5 and R6 can be increased to reduce gain peaking when driving from a high source impedance. The 50 Ω termination provides an insertion loss of 6 dB. C2 and C3 provide ac-coupling.	T2 = Macom™ ETC1-1-13 R1 = open, R2 = 25 Ω, R3 = 25 Ω, R4 = 0 Ω, R5 = 0 Ω, R6 = 0 Ω, C2 = 0.1 µF, C3 = 0.1 µF
R7, R8, R9, R10, R11, R12, R13, R14 , R15, T1, C4, C5	Resistors, Transformer, Capacitors	Output Interface. R10, R13, R14, and R15 ground one side of the differential output interface for single-ended applications. T1 is a 1-to-1 impedance ratio balun to transform a balanced differential signal to a single-ended signal. R8, R9, and R12 are provided for generic placement of matching components. R7 and R11 allow additional output series resistance when driving capacitive loads. The evaluation board is configured to provide a 150 Ω to 50 Ω impedance transformation with an insertion loss of 9.9 dB. C4 and C5 provide ac-coupling. R7 and R11 provide additional series resistance when driving capacitive loads.	T2= Macom™ ETC1-1-13 R7 = 0 Ω, R8 = 86.6 Ω, R9 = 57.6 Ω, R10 = open, R11 = 0 Ω R12 = 86.6 Ω, R13 = 0 Ω, R14 = 0 Ω, R15 = 0 Ω C4 = 0.1 µF, C5 = 0.1 µF
RG	Resistor	Gain Setting Resistor. Resistor R_G is used to set the gain of the device. Refer to Table 5 and Table 6 when selecting the gain resistor.	R_G = 100 Ω (Size 0402) for a gain of 10 dB
C1, C6, C7	Capacitors	Power Supply Decoupling. The supply decoupling consists of a 100 nF capacitor to ground. C6 and C7 are bypass capacitors.	C1 = 100 nF C6, C7 = 0.1 µF
Pin 14	VCM	Common Mode Offset Adjustment. Use Pin 14 to trim common-mode input/output levels. By applying a voltage to Pin 14, the input and output common-mode voltage can be directly adjusted.	Typically decoupled to ground using a 0.1 µF capacitor with ac-coupled input/output ports.

EVALUATION BOARD SCHEMATICS

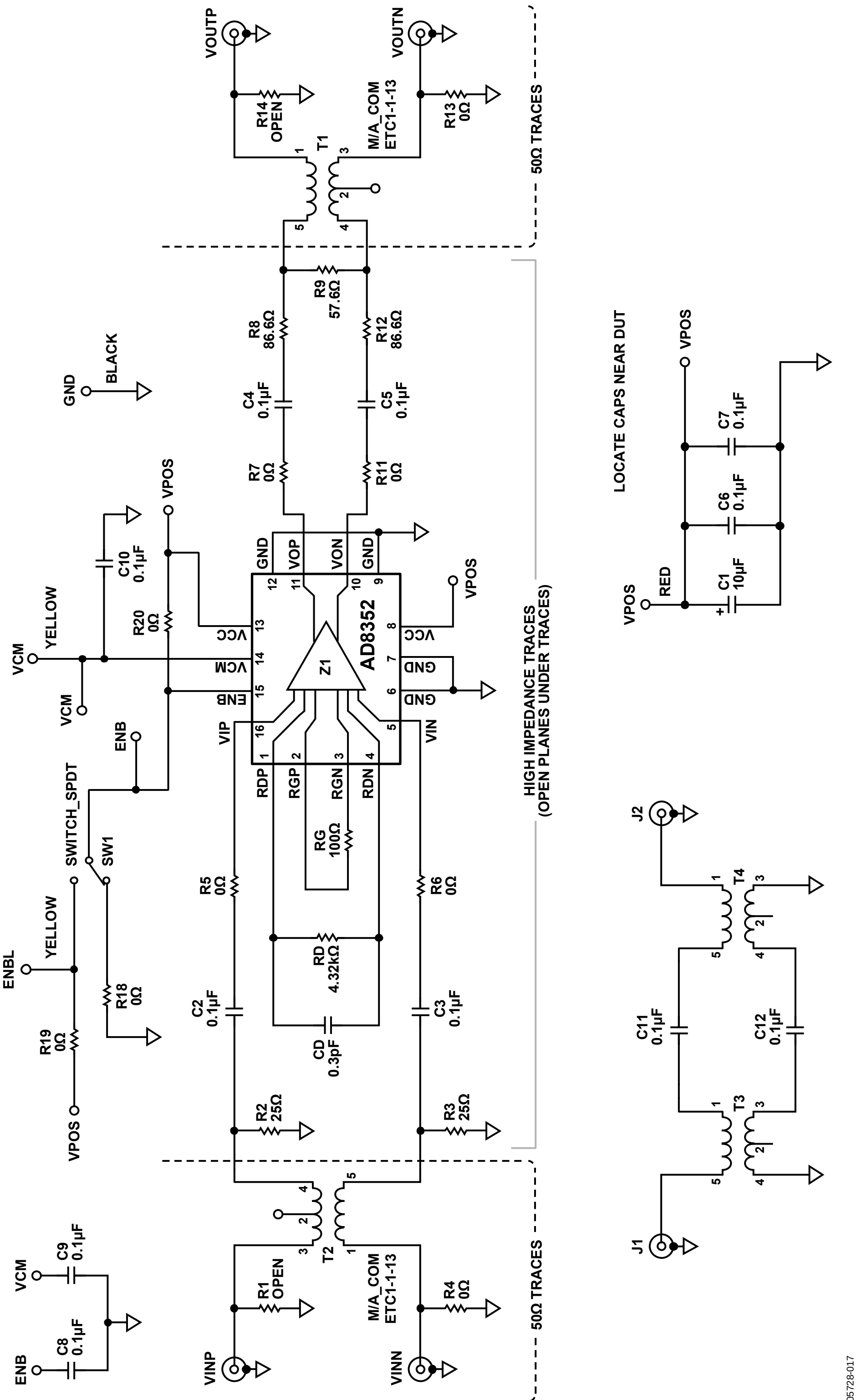

Figure 23. Preliminary Characterization Board v.A01212A

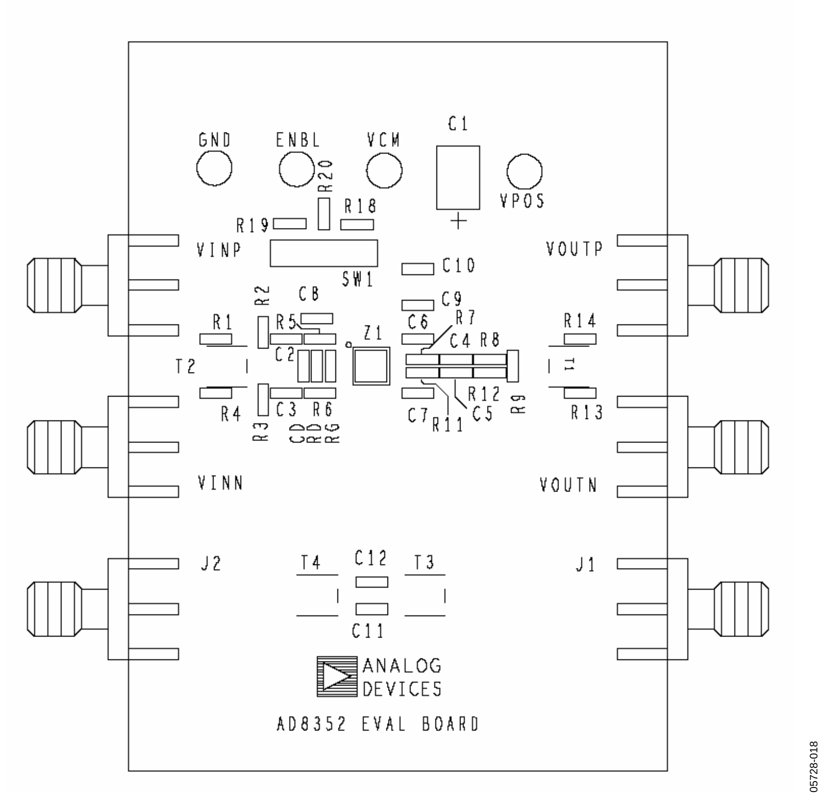

Figure 24. Component Side Silk Screen

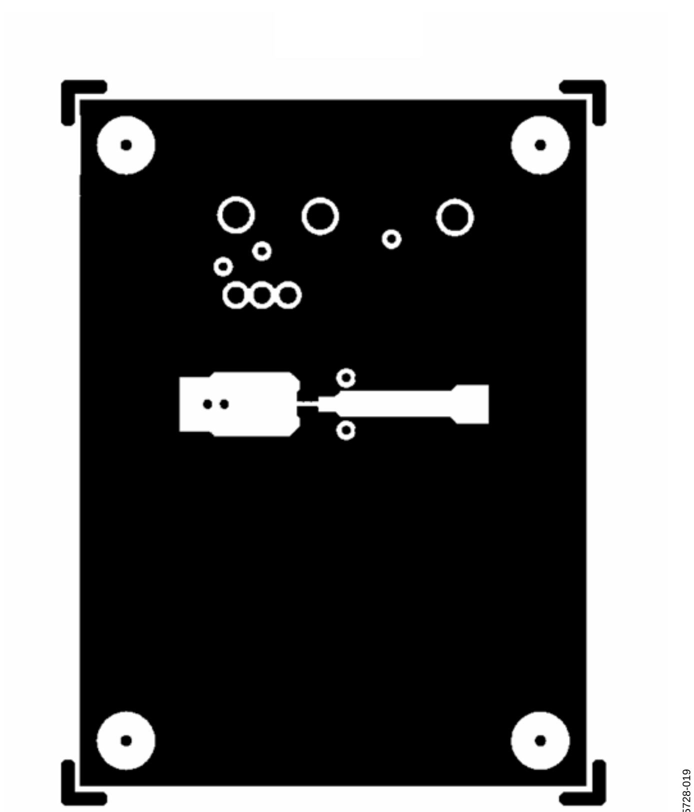

Figure 25. Far Side showing Ground Plane Pull Back around critical features

OUTLINE DIMENSIONS

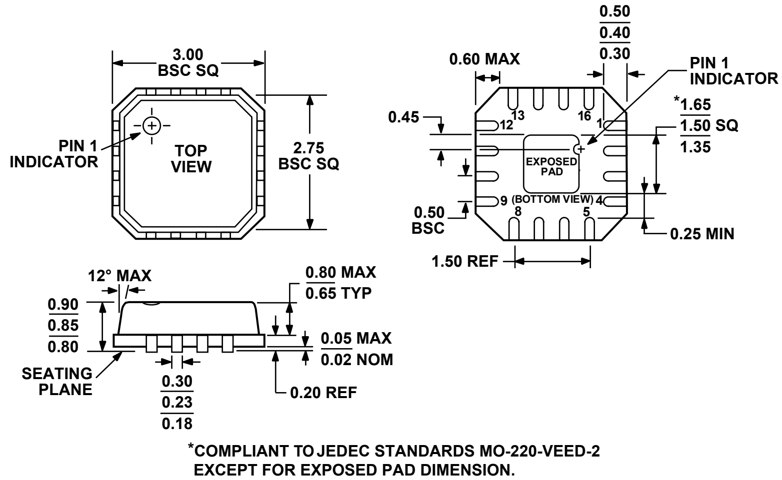

Figure 26. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8352ACPZ-WP[1]	−40°C to +85°C	16-Lead LFCSP, Tube	CP-16-3
AD8352ACPZ-RL7[1]	−40°C to +85°C	16-Lead LFCSP, 7" Tape and Reel	CP-16-3
AD8352-EVAL		Evaluation Board	

[1] Z = Pb-free part.

NOTES

PR05728-0-10/05(PrA)