Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 8-KByte Data Cache, 8-KByte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
- Additional Embedded Memories
  - One 32-KByte Internal ROM, Single-cycle Access At Maximum Matrix Speed
  - Two 4-KByte Internal SRAM, Single-cycle Access At Maximum Matrix Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- USB 2.0 Full Speed (12 Mbits per second) Host Single Port in the 208-lead PQFP Package and Double Port in 217-ball LFBGA Package
  - Single or Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - Six 32-bit-layer Matrix
  - Boot Mode Select Option, Remap Command
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
- Reset Controller (RSTC)
  - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output Control
- Clock Generator (CKGR)
  - Selectable 32,768 Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator, One up to 240 MHz PLL and One up to 130 MHz PLL
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected

AT91 ARM Thumb Microcontrollers

AT91SAM9260

Summary

Preliminary

6221BS–ATARM–12-Jun-06

- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog-to-Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - High-current Drive I/O Lines, Up to 16 mA Each
- Peripheral DMA Controller Channels (PDC)
- One Two-slot MultiMedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- Two 2-wire UARTs
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
  - High-Drive Capability on Outputs TIOA0, TIOA1, TIOA2
- One Two-wire Interface (TWI)
  - Master, Multi-master and Slave Mode Operation
  - General Call Supported in Slave Mode
  - Connection to PDC Channel To Optimize Data Transfers in Master Mode Only
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.65V to 1.95V for VDDBU, VDDCORE, VDDOSC and VDDPLL
  - 3.0V to 3.6V for VDDIOP0, VDDIOP1 (Peripheral I/Os) and VDDANA (Analog to Digital Converter)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 208-lead PQFP and 217-ball LFBGA Package

1. Description

The AT91SAM9260 is based on the integration of an ARM926EJ-S processor with fast ROM and RAM memories and a wide range of peripherals.

The AT91SAM9260 embeds an Ethernet MAC, one USB Device Port, and a USB Host controller. It also integrates several standard peripherals, such as the USART, SPI, TWI, Timer Counters, Synchronous Serial Controller, ADC and MultiMedia Card Interface.

The AT91SAM9260 is architectured on a 6-layer matrix, allowing a maximum internal bandwidth of six 32-bit buses. It also features an External Bus Interface capable of interfacing with a wide range of memory devices.

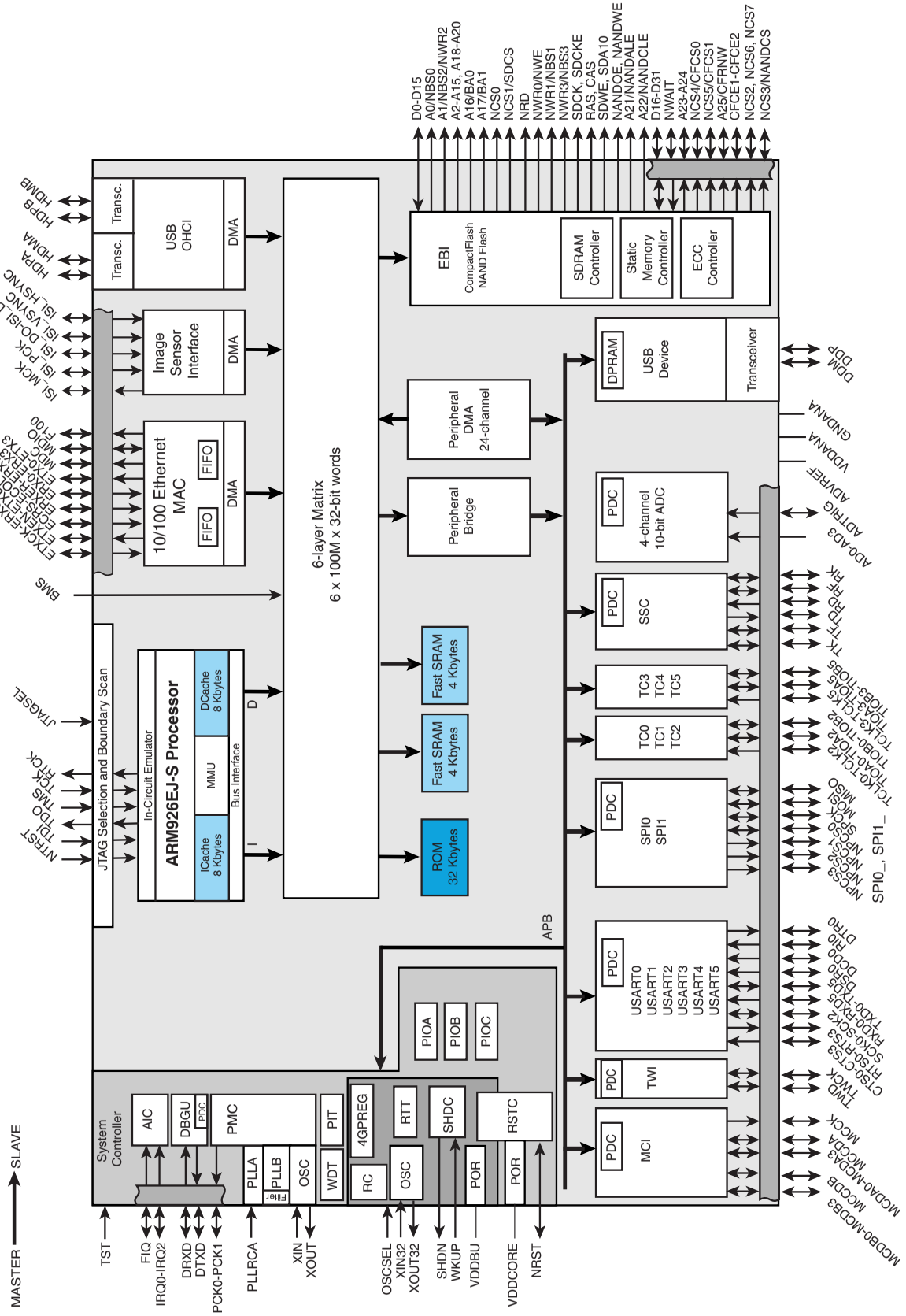
2. AT91SAM9260 Block Diagram

The block diagram shows all the features for the 217-LFBGA package. Some functions are not accessible in the 208-pin PQFP package and the unavailable pins are highlighted in ”Multiplexing on PIO Controller A” on page 34, ”Multiplexing on PIO Controller B” on page 35, ”Multiplexing on PIO Controller C” on page 36. The USB Host Port B is not available in the 208-pin package. Table 2-1 on page 3 defines all the multiplexed and not multiplexed pins not available in the 208-PQFP package.

Table 2-1. Unavailable Signals in 208-lead PQFP Package

PIO	Peripheral A	Peripheral B
-	HDPB	-
-	HDMB	-
PA30	SCK2	RXD4
PA31	SCK0	TXD4
PB12	TXD5	ISI_D10
PB13	RXD5	ISI_D11
PC2	AD2	PCK1
PC3	AD3	SPI1_NPCS3
PC12	IRQ0	NCS7

Figure 2-1. AT91SAM9260 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65V to 1.95V or 3.0V to3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power		3.0V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power		
VDDBU	Backup I/O Lines Power Supply	Power		1.65V to 1.95V
VDDANA	Analog Power Supply	Power		3.0V to 3.6V
VDDPLL	PLL Power Supply	Power		1.65V to 1.95V
VDDOSC	Oscillator Power Supply	Power		1.65V to 1.95V
VDDCORE	Core Chip Power Supply	Power		1.65V to 1.95V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDANA	Analog Ground	Ground		
GNDOSC	Oscillator Ground	Ground		
GNDBU	Backup Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
OSCSEL	Slow Clock Oscillator Selection	Input		
PLLRCA	PLL A Filter	Input		
PCK0 - PCK1	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Driven at 0V only. Do not tie over VDDBU.
WKUP	Wake-up Input	Input		Accepts between 0V and VDDBU.
ICE and JTAG				
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
RTCK	Return Test Clock	Output		
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor
BMS	Boot Mode Select	Input		
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ0 - IRQ2	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA - PIOB - PIOC				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
External Bus Interface - EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset
A0 - A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0 - NCS7	Chip Select Lines	Output	Low	
NWR0 - NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NANDALE	NAND Flash Address Latch Enable	Output	Low	
NANDCLE	NAND Flash Command Latch Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Multimedia Card Interface MCI				
MCCK	Multimedia Card Clock	Output		
MCCDA	Multimedia Card Slot A Command	I/O		
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O		
MCCDB	Multimedia Card Slot B Command	I/O		
MCDB0 - MCDB3	Multimedia Card Slot B Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter USARTx				
SCKx	USARTx Serial Clock	I/O		
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		
CTSx	USARTx Clear To Send	Input		
DTR0	USART0 Data Terminal Ready	Output		
DSR0	USART0 Data Set Ready	Input		
DCD0	USART0 Data Carrier Detect	Input		
RI0	USART0 Ring Indicator	Input		
Synchronous Serial Controller - SSC				
TD	SSC Transmit Data	Output		
RD	SSC Receive Data	Input		
TK	SSC Transmit Clock	I/O		
RK	SSC Receive Clock	I/O		
TF	SSC Transmit Frame Sync	I/O		
RF	SSC Receive Frame Sync	I/O		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Timer/Counter - TCx				
TCLKx	TC Channel x External Clock Input	Input		
TIOAx	TC Channel x I/O Line A	I/O		
TIOBx	TC Channel x I/O Line B	I/O		
Serial Peripheral Interface - SPIx_				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1-SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
USB Host Port				
HDPA	USB Host Port A Data +	Analog		
HDMA	USB Host Port A Data -	Analog		
HDPB	USB Host Port B Data +	Analog		
HDMB	USB Host Port B Data +	Analog		
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
Ethernet 10/100				
ETXCK	Transmit Clock or Reference Clock	Input		MII only, REFCK in RMII
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0-ETX3	Transmit Data	Output		ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		RXDV in MII , CRSDV in RMII
ERX0-ERX3	Receive Data	Input		ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense and Data Valid	Input		MII only
ECOL	Collision Detect	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100Mbit/sec.	Output	High	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Image Sensor Interface				
ISI_D0-ISI_D11	Image Sensor Data	Input		
ISI_MCK	Image Sensor Reference Clock	Output		
ISI_HSYNC	Image Sensor Horizontal Synchro	Input		
ISI_VSYNC	Image Sensor Vertical Synchro	Input		
ISI_PCK	Image Sensor Data clock	Input		
Analog to Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
ADVREFP	Analog Positive Reference	Analog		
ADTRG	ADC Trigger	Input		

4. Package and Pinout

The AT91SAM9260 is available in two packages:

- 208-pin PQFP Green package (0.5mm pitch) (Figure 4-1)
- 217-ball LFBGA RoHS-compliant package (0.8 mm ball pitch) (Figure 4-2).

The marking codes of the AT91SAM9260 as written on the packages are:

- “xxxxxxx”: the lot number
- “YY”: the manufactory year
- “WW”: the manufactory week
- “v”: External revision number

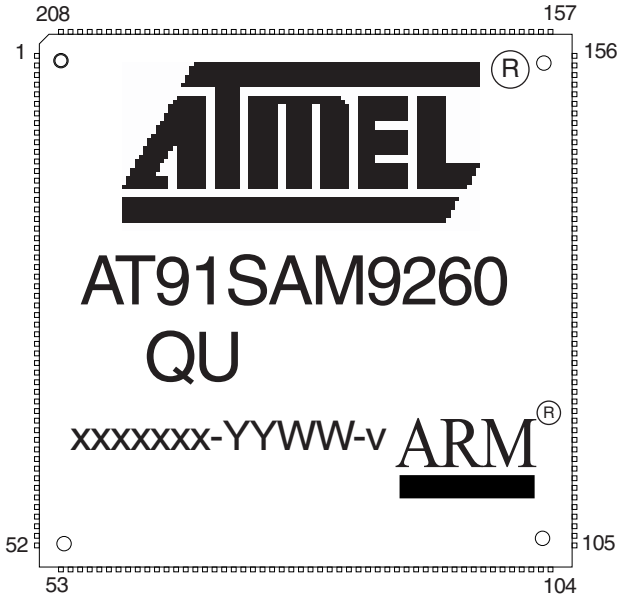
4.1 208-pin PQFP Package

4.1.1 Mechanical Overview

Figure 4-1 shows the orientation of the 208-pin PQFP package.

A detailed mechanical description is given in the section “AT91SAM9260 Mechanical Characteristics” of the product datasheet.

Figure 4-1. 208-pin PQFP Package



4.1.2 Pinout

Table 4-1. Pinout for 208-pin PQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PA24	53	GND	105	RAS	157	ADVREFP
2	PA25	54	DDM	106	D0	158	PC0
3	PA26	55	DDP	107	D1	159	PC1
4	PA27	56	PC13	108	D2	160	VDDANA
5	VDDIOP0	57	PC11	109	D3	161	PB10
6	GND	58	PC10	110	D4	162	PB11
7	PA28	59	PC14	111	D5	163	PB20
8	PA29	60	PC9	112	D6	164	PB21
9	PB0	61	PC8	113	GND	165	PB22
10	PB1	62	PC4	114	VDDIOM	166	PB23
11	PB2	63	PC6	115	SDCK	167	PB24
12	PB3	64	PC7	116	SDWE	168	PB25
13	VDDIOP0	65	VDDIOM	117	SDCKE	169	VDDIOP1
14	GND	66	GND	118	D7	170	GND
15	PB4	67	PC5	119	D8	171	PB26
16	PB5	68	NCS0	120	D9	172	PB27
17	PB6	69	CFOE/NRD	121	D10	173	GND
18	PB7	70	CFWE/NWE/NWR0	122	D11	174	VDDCORE
19	PB8	71	NANDOE	123	D12	175	PB28
20	PB9	72	NANDWE	124	D13	176	PB29
21	PB14	73	A22	125	D14	177	PB30
22	PB15	74	A21	126	D15	178	PB31
23	PB16	75	A20	127	PC15	179	PA0
24	VDDIOP0	76	A19	128	PC16	180	PA1
25	GND	77	VDDCORE	129	PC17	181	PA2
26	PB17	78	GND	130	PC18	182	PA3
27	PB18	79	A18	131	PC19	183	PA4
28	PB19	80	BA1/A17	132	VDDIOM	184	PA5
29	TDO	81	BA0/A16	133	GND	185	PA6
30	TDI	82	A15	134	PC20	186	PA7
31	TMS	83	A14	135	PC21	187	VDDIOP0
32	VDDIOP0	84	A13	136	PC22	188	GND
33	GND	85	A12	137	PC23	189	PA8
34	TCK	86	A11	138	PC24	190	PA9
35	NTRST	87	A10	139	PC25	191	PA10
36	NRST	88	A9	140	PC26	192	PA11
37	RTCK	89	A8	141	PC27	193	PA12
38	VDDCORE	90	VDDIOM	142	PC28	194	PA13
39	GND	91	GND	143	PC29	195	PA14
40	BMS	92	A7	144	PC30	196	PA15
41	OSCSEL	93	A6	145	PC31	197	PA16
42	TST	94	A5	146	GND	198	PA17
43	JTAGSEL	95	A4	147	NC	199	VDDIOP0
44	GNDBU	96	A3	148	VDDPLLB	200	GND
45	XOUT32	97	A2	149	XIN	201	PA18
46	XIN32	98	NWR2/NBS2/A1	150	XOUT	202	PA19
47	VDDBU	99	NBS0/A0	151	GNDPLLB	203	VDDCORE
48	WKUP	100	SDA10	152	NC	204	GND
49	SHDN	101	CFIOW/NBS3/NWR3	153	GNDPLLA	205	PA20
50	HDMA	102	CFIOR/NBS1/NWR1	154	PLLRCA	206	PA21
51	HDPA	103	SDCS/NCS1	155	VDDPLLA	207	PA22
52	VDDIOP0	104	CAS	156	GNDANA	208	PA23

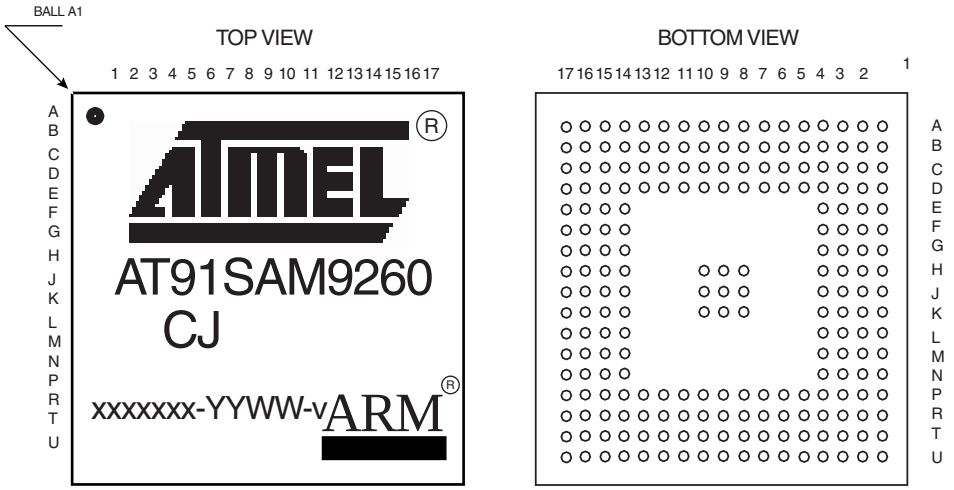
4.2 217-ball LFBGA Package

4.2.1 Mechanical Overview

Figure 4-2 shows the orientation of the 217-ball LFBGA package.

A detailed mechanical description is given in the section “AT91SAM9260 Mechanical Characteristics” of the product datasheet.

Figure 4-2. 217-ball LFBGA Package



4.2.2 Pinout

Table 4-2. Pinout for 217-ball LFBGA Package

Pin	Signal Name
A1	CFIOW/NBS3/NWR3
A2	NBS0/A0
A3	NWR2/NBS2/A1
A4	A6
A5	A8
A6	A11
A7	A13
A8	BA0/A16
A9	A18
A10	A21
A11	A22
A12	CFWE/NWE/NWR0
A13	CFOE/NRD
A14	NCS0
A15	PC5
A16	PC6
A17	PC4
B1	SDCK
B2	CFIOR/NBS1/NWR1
B3	SDCS/NCS1
B4	SDA10
B5	A3
B6	A7
B7	A12
B8	A15
B9	A20
B10	NANDWE
B11	PC7
B12	PC10
B13	PC13
B14	PC11
B15	PC14
B16	PC8
B17	WKUP
C1	D8
C2	D1
C3	CAS
C4	A2
C5	A4
C6	A9
C7	A14
C8	BA1/A17
C9	A19
C10	NANDOE
C11	PC9
C12	PC12
C13	DDP
C14	HDMB
C15	NC
C16	VDDIOP0
C17	SHDN
D1	D9
D2	D2
D3	RAS
D4	D0
D5	A5
D6	GND
D7	A10
D8	GND
D9	VDDCORE
D10	GND
D11	VDDIOM
D12	GND
D13	DDM
D14	HDPB
D15	NC
D16	VDDBU
D17	XIN32
E1	D10
E2	D5
E3	D3
E4	D4
E14	HDPA
E15	HDMA
E16	GNDBU
E17	XOUT32
F1	D13
F2	SDWE
F3	D6
F4	GND
F14	OSCSEL
F15	BMS
F16	JTAGSEL
F17	TST
G1	PC15
G2	D7
G3	SDCKE
G4	VDDIOM
G14	GND
G15	NRST
G16	RTCK
G17	TMS
H1	PC18
H2	D14
H3	D12
H4	D11
H8	GND
H9	GND
H10	GND
H14	VDDCORE
H15	TCK
H16	NTRST
H17	PB18
J1	PC19
J2	PC17
J3	VDDIOM
J4	PC16
J8	GND
J9	GND
J10	GND
J14	TDO
J15	PB19
J16	TDI
J17	PB16
K1	PC24
K2	PC20
K3	D15
K4	PC21
K8	GND
K9	GND
K10	GND
K14	PB4
K15	PB17
K16	GND
K17	PB15
L1	GND
L2	PC26
L3	PC25
L4	VDDIOP0
L14	PA28
L15	PB9
L16	PB8
L17	PB14
M1	VDDCORE
M2	PC31
M3	GND
M4	PC22
M14	PB1
M15	PB2
M16	PB3
M17	PB7
N1	XIN
N2	VDDPLLB
N3	PC23
N4	PC27
N14	PA31
N15	PA30
N16	PB0
N17	PB6
P1	XOUT
P2	VDDPLLA
P3	PC30
P4	PC28
P5	PB11
P6	PB13
P7	PB24
P8	VDDIOP1
P9	PB30
P10	PB31
P11	PA1
P12	PA3
P13	PA7
P14	PA9
P15	PA26
P16	PA25
P17	PB5
R1	NC
R2	GNDANA
R3	PC29
R4	VDDANA
R5	PB12
R6	PB23
R7	GND
R8	PB26
R9	PB28
R10	PA0
R11	PA4
R12	PA5
R13	PA10
R14	PA21
R15	PA23
R16	PA24
R17	PA29
T1	PLLRCA
T2	GNDPLLB
T3	PC0
T4	PC1
T5	PB10
T6	PB22
T7	GND
T8	PB29
T9	PA2
T10	PA6
T11	PA8
T12	PA11
T13	VDDCORE
T14	PA20
T15	GND
T16	PA22
T17	PA27
U1	GNDPLLA
U2	ADVREFP
U3	PC2
U4	PC3
U5	PB20
U6	PB21
U7	PB25
U8	PB27
U9	PA12
U10	PA13
U11	PA14
U12	PA15
U13	PA19
U14	PA17
U15	PA16
U16	PA18
U17	VDDIOP0

5. Power Considerations

5.1 Power Supplies

The AT91SAM9260 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.65V and 1.95V, 1.8V nominal.
- VDDIOM pins: Power the External Bus Interface I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical) or between 3.0V and 3.6V (3.3V nominal). The expected voltage range is selectable by software.
- VDDIOP0 pins: Power the Peripheral I/O lines and the USB transceivers; voltage ranges from 3.0V and 3.6V, 3V or 3.3V nominal.
- VDDIOP1 pins: Power the Peripherals I/O lines involving the Image Sensor Interface; voltage ranges from 1.65V and 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.65V to 1.95V, 1.8V nominal.
- VDDPLL pin: Powers the PLL cells; voltage ranges from 1.65V and 1.95V, 1.8V nominal.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 1.65V and 1.95V, 1.8V nominal.
- VDDANA pin: Powers the Analog to Digital Converter; voltage ranges from 3.0V and 3.6V, 3.3V nominal.

The power supplies VDDIOM, VDDIOP0 and VDDIOP1 are identified in the pinout table and the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDCORE, VDDIOM, VDDIOP0 and VDDIOP1 pins power supplies. Separated ground pins are provided for VDDBU, VDDOSC, VDDPLL and VDDANA. These ground pins are respectively GNDBU, GNDOSC, GNDPLL and GNDANA.

5.2 Power Consumption

The AT91SAM9260 consumes about 500 µA of static current on VDDCORE at 25°C. This static current rises up to 5 mA if the temperature increases to 85°C.

On VDDBU, the current does not exceed 10µA in worst case conditions.

For dynamic power consumption, the AT91SAM9260 consumes a maximum of 100 mA on VDDCORE at maximum conditions (1.8V, 25°C, processor running full-performance algorithm out of high speed memories).

5.3 Programmable I/O Lines Power Supplies

The power supplies pins VDDIOM accept two voltage ranges. This allows the device to reach its maximum speed either out of 1.8V or 3.3V external memories.

The target maximum speed is **100 MHz** on the pin SDCK (SDRAM Clock) loaded with **30 pF** for power supply at 1.8V and **50 pF** for power supply at 3.3V. The other signals (control, address and data signals) do not exceed 50MHz.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. Obviously, the device cannot reach its maximum speed if the voltage supplied to the pins is 1.8V only. The user must program the EBI voltage range before getting the device out of its Slow Clock Mode.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about **15 kΩ** to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 6.3.

All the JTAG signals are supplied with VDDIOP0.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about **15 kΩ** to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of **100 kΩ** minimum to VDDIOP0.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines are managed by the PIO Controllers integrate a programmable pull-up resistor of **100 kΩ** typical. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals and that must be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

6.5 I/O Line Drive Levels

The PIO lines are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

6.6 Shutdown Logic Pins

The SHDN pin is an output only, which is driven by the Shutdown Controller.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

6.7 Slow Clock Selection

The AT91SAM9260 slow clock can be generated either by an external 32,768 Hz crystal or the on-chip RC oscillator.

Table 6-1 on page 16 defines the states for OSCSEL signal.

Table 6-1. Slow Clock Selection

OSCSEL	Slow Clock
0	Internal RC
1	External 32,768 Hz

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 8-Kbyte Data Cache, 8-Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain

- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Bus Matrix

- 6-layer Matrix, handling requests from 6 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

7.2.1 Matrix Masters

The Bus Matrix of the AT91SAM9260 manages six Masters, which means that each master can perform an access concurrently with others, according the slave it accesses is available.

Each Master has its own decoder that can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	ARM926™ Instruction
Master 1	ARM926 Data
Master 2	PDC
Master 3	ISI Controller
Master 4	Ethernet MAC
Master 5	USB Host DMA

7.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing a different arbitration per Slave to be programmed.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM0 4kBytes
Slave 1	Internal SRAM1 4kBytes
Slave 2	Internal ROM
	USB Host User Interface
Slave 3	External Bus Interface
Slave 4	Internal Peripherals

7.2.3 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown "-" in the following table.

Table 7-3. AT91SAM9260 Masters to Slaves Access

Master		0 & 1	2	3	4	5
Slave		ARM926 Instruction & Data	Peripheral DMA Controller	ISI Controller	Ethernet MAC	USB Host Controller
0	Internal SRAM 4 KBytes	X	X	X	X	X
1	Internal SRAM 4 KBytes	X	X	X	X	X
2	Internal ROM	X	X	-	-	X
	UHP User Interface	X	-	-	-	-
3	External Bus Interface	X	X	X	X	X
4	Internal Peripherals	X	X	-	-	X

7.3 Peripheral DMA Controller

- Acting as one Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Twenty-four channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - Two for the Two-wire Interface
  - One for Multimedia Card Interface
  - One for Analog-to-Digital Converter

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

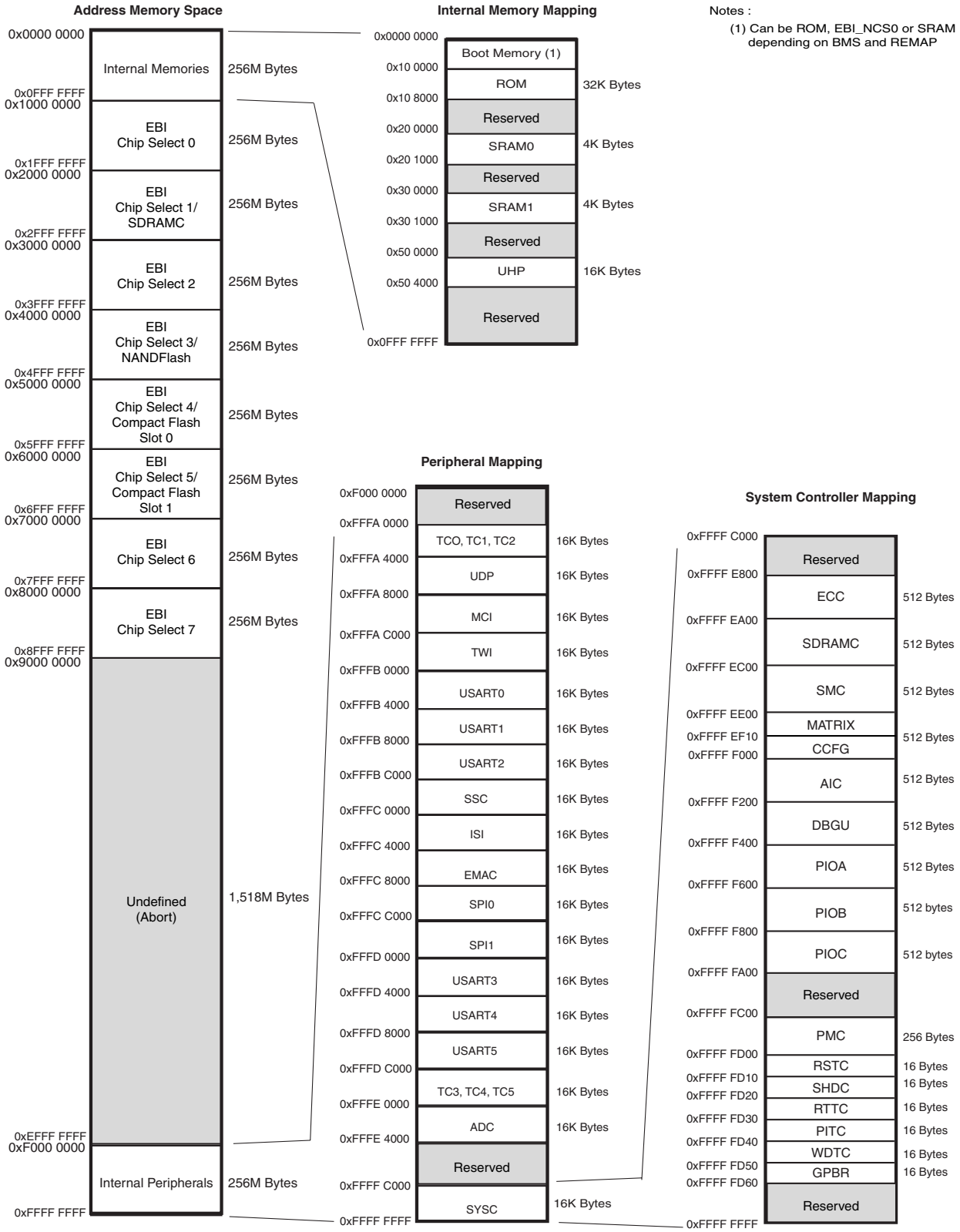
- TWI Transmit Channel
- DBGU Transmit Channel
- USART5 Transmit Channel
- USART4 Transmit Channel
- USART3 Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC Transmit Channel
- TWI Receive Channel
- DBGU Receive Channel
- USART5 Receive Channel
- USART4 Receive Channel
- USART3 Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- ADC Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC Receive Channel
- MCI Transmit/Receive Channel

7.4 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Memories

Figure 8-1. AT91SAM9260 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High Performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4G bytes of address space into 16 banks of 256M bytes. The banks 1 to 7 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS7. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M byte of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926 Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap. Refer to Table 8-1, “Internal Memory Mapping,” on page 22 for details.

A complete memory map is presented in Figure 8-1 on page 21.

8.1 Embedded Memories

- 32-KByte ROM
  - Single Cycle Access at full matrix speed
- Two 4-Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed

8.1.1 Boot Strategies

Table 8-1 summarizes the Internal Memory Mapping for each Master, depending on the Remap status and the BMS state at reset.

Table 8-1. Internal Memory Mapping

Address	REMAP = 0		REMAP = 1
	BMS = 1	BMS = 0	
0x0000 0000	ROM	EBI_NCS0	SRAM0 4K

The system always boots at address 0x0. To ensure a maximum number of possibilities for boot, the memory layout can be configured with two parameters.

REMAP allows the user to lay out the first internal SRAM bank to 0x0 to ease development. This is done by software once the system has booted. When REMAP = 1, BMS is ignored. Refer to the Bus Matrix Section for more details.

When REMAP = 0, BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 21.

The AT91SAM9260 matrix manages a boot memory that depends on the level on the BMS pin at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved for this purpose.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.1.1 BMS = 1, Boot on Embedded ROM

The system boots using Boot Program.

- Boot on slow clock (On-chip RC or 32,768 Hz)
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SPI DataFlash® connected on NPCS0 of the SPI0
  - 8-bit NANDFlash
- SAM-BA™ Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device Port

8.1.1.2 BMS = 0, Boot on External Memory

- Boot on slow clock (On-chip RC or 32,768 Hz)
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI CS0 (BMS=0), the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

8.2 External Memories

The external memories are accessed through the External Bus Interface. Each Chip Select line has a 256-Mbyte memory area assigned.

Refer to the memory map in Figure 8-1 on page 21.

8.2.1 External Bus Interface

- Integrates three External Memory Controllers
  - Static Memory Controller

  - SDRAM Controller
  - ECC Controller
- Additional logic for NANDFlash
- Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64MBytes linear)
- Up to 8 chip selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash support
  - Static Memory Controller on NCS6-NCS7

8.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

8.2.3 SDRAM Controller

- Supported devices
  - Standard and Low-power SDRAM (Mobile SDRAM)
- Numerous configurations supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks
  - SDRAM with 16- or 32-bit Datapath
- Programming facilities
  - Word, half-word, byte access
  - Automatic page break when Memory Boundary has been reached
  - Multibank Ping-pong Access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities

  - Self-refresh, power down and deep power down modes supported
- Error detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- CAS Latency of 1, 2 and 3 supported
- Auto Precharge Command not used

8.2.4 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by trigging on the corresponding chip select
- Single bit error correction and 2-bit Random detection
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-bytes pages

9. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure EBI chip select assignment and voltage range for external memories

The System Controller's peripherals are all mapped within the highest 16K bytes of address space, between addresses 0xFFFF E800 and 0xFFFF FFFF.

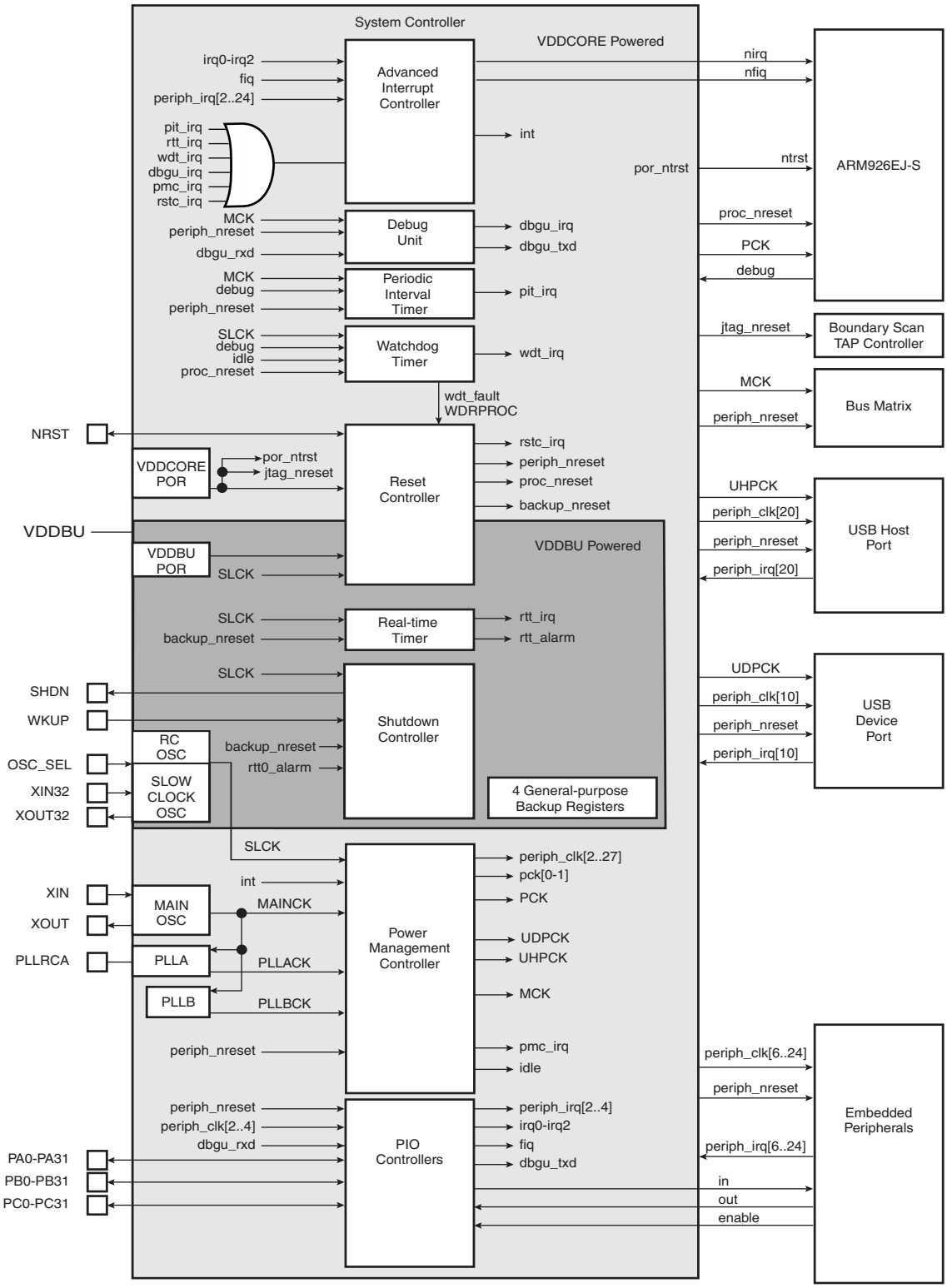
However, all the registers of System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction has an indexing mode of ±4 Kbytes.

Figure 9-1 on page 27 shows the System Controller block diagram.

Figure 8-1 on page 21 shows the mapping of the User Interfaces of the System Controller peripherals.

9.1 Block Diagram

Figure 9-1. AT91SAM9260 System Controller Block Diagram



9.2 Reset Controller

- Based on two Power-on-reset cells
  - One on VDDBU and one on VDDCORE
- Status of the last reset
  - Either general reset (VDDBU rising), wake-up reset (VDDCORE rising), software reset, user reset or watchdog reset
- Controls the internal resets and the NRST pin output
  - Allows shaping a reset signal for the external devices

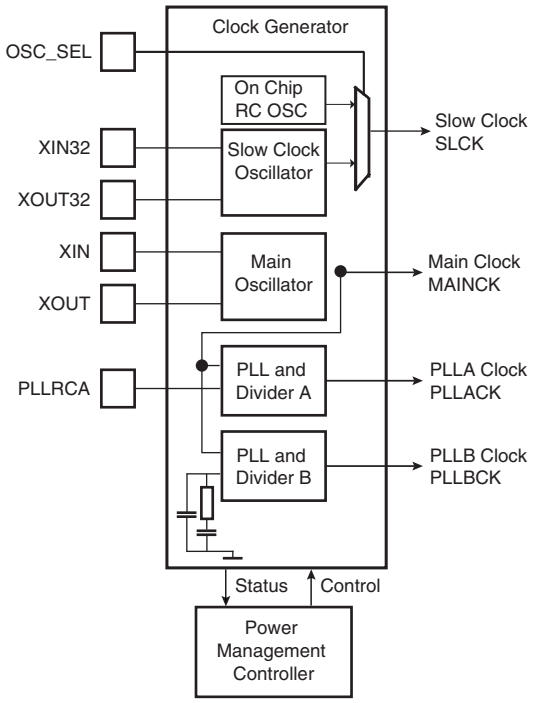
9.3 Shutdown Controller

- Shutdown and Wake-up logic
  - Software programmable assertion of the SHDWN pin
  - Deassertion Programmable on a WKUP pin level change or on alarm

9.4 Clock Generator

- Embeds a Low-power 32,768 Hz Slow Clock Oscillator and a Low-power RC oscillator selectable with OSCSEL signal
  - Provides the permanent Slow Clock SLCK to the system
- Embeds the Main Oscillator
  - Oscillator bypass feature
  - Supports 3 to 20 MHz crystals
- Embeds 2 PLLs
  - PLLA outputs 80 to 240 MHz clock
  - PLLB outputs 70 to 130 MHz clock
  - Both integrate an input divider to increase output accuracy
  - PLLB embeds its own filter

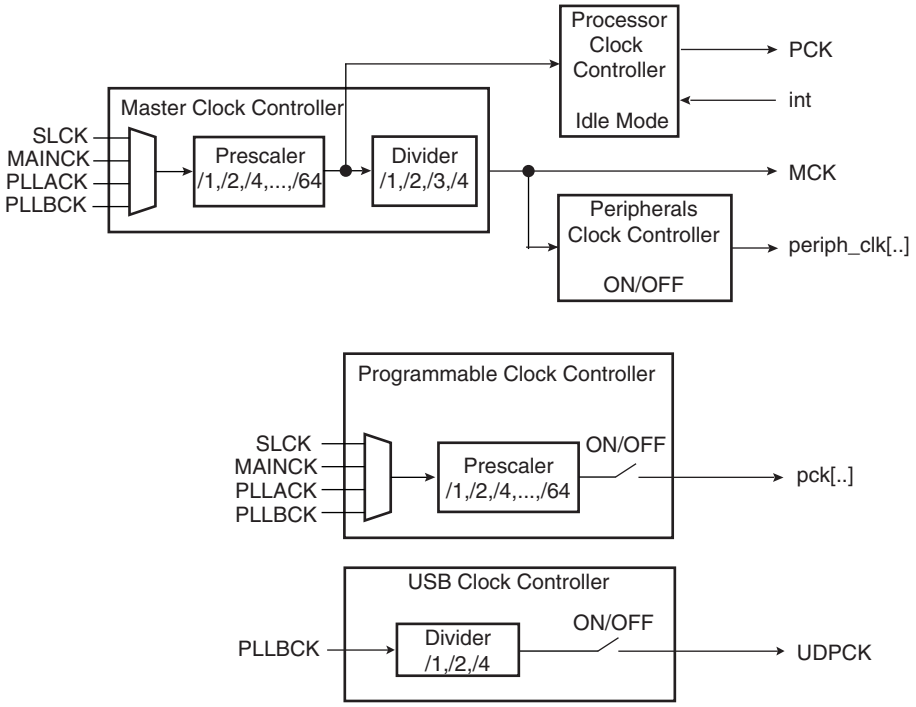
Figure 9-2. Clock Generator Block Diagram



9.5 Power Management Controller

- Provides:
  - the Processor Clock PCK
  - the Master Clock MCK, in particular to the Matrix and the memory interfaces
  - the USB Device Clock UDPCK
  - independent peripheral clocks, typically at the frequency of MCK
  - 2 programmable clock outputs: PCK0, PCK1
- Five flexible operating modes:
  - Normal Mode, processor and peripherals running at a programmable frequency
  - Idle Mode, processor stopped waiting for an interrupt
  - Slow Clock Mode, processor and peripherals running at low frequency
  - Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
  - Backup Mode, Main Power Supplies off, VDDBU powered by a battery

Figure 9-3. AT91SAM9260 Power Management Controller Block Diagram



9.6 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1 µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real Time OS or Linux®/Windows CE® compliant tick generator

9.7 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor being in a dead-lock on the watchdog access

9.8 Real-time Timer

- Real-time Timer 32-bit free-running back-up Counter
- Integrates a 16-bit programmable prescaler running on slow clock
- Alarm Register capable of generating a wake-up of the system through the Shutdown Controller

9.9 General-purpose Back-up Registers

- Four 32-bit backup general-purpose registers

9.10 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)

  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- Three External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect models are enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

9.11 Debug Unit

- Composed of two functions:
  - Two-pin UART
  - Debug Communication Channel (DCC) support
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
  - Offers visibility of and interrupt trigger from COMMRX and COMMTX signals from the ARM Processor's ICE Interface

9.12 Chip Identification

- Chip ID: 0x019803A0
- JTAG ID: 0x05B1303F
- ARM926™ TAP ID: 0x0792603F

10. Peripherals

10.1 User Interface

The peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFFA 0000 and 0xFFFC FFFF. Each User Peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in Figure 8-1 on page 21.

10.2 Identifiers

Table 10-1 defines the Peripheral Identifiers of the AT91SAM9260. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. AT91SAM9260 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC	System Controller Interrupt	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	ADC	Analog to Digital Converter	
6	US0	USART 0	
7	US1	USART 1	
8	US2	USART 2	
9	MCI	Multimedia Card Interface	
10	UDP	USB Device Port	
11	TWI	Two Wire Interface	
12	SPIO	Serial Peripheral 0	
13	SPI1	Serial Peripheral 1	
14	SSC	Serial Peripheral Interface 0	
15	-	Reserved	
16	-	Reserved	
17	TC0	Timer/Counter 0	
18	TC1	Timer/Counter 1	
19	TC2	Timer/Counter 2	
20	UHP	USB Host Port	
21	EMAC	Ethernet MAC	
22	ISI	Image Sensor Interface	
23	US3	USART 3	
24	US4	USART 4	
25	US5	USART 5	
26	TC3	Timer/Counter 3	
27	TC4	Timer/Counter 4	
28	TC5	Timer/Counter 5	
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1
31	AIC	Advanced Interrupt Controller	IRQ2

10.2.1 Peripheral Interrupts and Clock Control

10.2.1.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the SDRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-time Timer
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

10.2.1.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signals IRQ0 to IRQ2, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

10.3 Peripheral Signal Multiplexing on I/O Lines

The AT91SAM9260 features 3 PIO controllers (PIOA, PIOB, PIOC) that multiplex the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. Table 10-2 on page 34, Table 10-3 on page 35 and Table 10-4 on page 36 define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted in this table for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only might be duplicated within both tables.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O appears, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name appears in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

10.3.1 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A					Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PA0	SPI0_MISO	MCDB0		I/O	VDDIOP0		
PA1	SPI0_MOSI	MCCDB		I/O	VDDIOP0		
PA2	SPI0_SPCK			I/O	VDDIOP0		
PA3	SPI0_NPCS0	MCDB3		I/O	VDDIOP0		
PA4	RTS2	MCDB2		I/O	VDDIOP0		
PA5	CTS2	MCDB1		I/O	VDDIOP0		
PA6	MCDA0			I/O	VDDIOP0		
PA7	MCCDA			I/O	VDDIOP0		
PA8	MCCK			I/O	VDDIOP0		
PA9	MCDA1			I/O	VDDIOP0		
PA10	MCDA2	ETX2		I/O	VDDIOP0		
PA11	MCDA3	ETX3		I/O	VDDIOP0		
PA12	ETX0			I/O	VDDIOP0		
PA13	ETX1			I/O	VDDIOP0		
PA14	ERX0			I/O	VDDIOP0		
PA15	ERX1			I/O	VDDIOP0		
PA16	ETXEN			I/O	VDDIOP0		
PA17	ERXDV			I/O	VDDIOP0		
PA18	ERXER			I/O	VDDIOP0		
PA19	ETXCK			I/O	VDDIOP0		
PA20	EMDC			I/O	VDDIOP0		
PA21	EMDIO			I/O	VDDIOP0		
PA22	ADTRG	ETXER		I/O	VDDIOP0		
PA23	TWD	ETX2		I/O	VDDIOP0		
PA24	TWCK	ETX3		I/O	VDDIOP0		
PA25	TCLK0	ERX2		I/O	VDDIOP0		
PA26	TIOA0	ERX3		I/O	VDDIOP0		
PA27	TIOA1	ERXCK		I/O	VDDIOP0		
PA28	TIOA2	ECRS		I/O	VDDIOP0		
PA29	SCK1	ECOL		I/O	VDDIOP0		
PA30[1]	SCK2	RXD4		I/O	VDDIOP0		
PA31[1]	SCK0	TXD4		I/O	VDDIOP0		

Note: 1. Not available in the 208-lead PQFP package.

10.3.2 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B					Application Usage		
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Reset State**	**Power Supply**	**Function**	**Comments**
PB0	SPI1_MISO	TIOA3		I/O	VDDIOP0		
PB1	SPI1_MOSI	TIOB3		I/O	VDDIOP0		
PB2	SPI1_SPCK	TIOA4		I/O	VDDIOP0		
PB3	SPI1_NPCS0	TIOA5		I/O	VDDIOP0		
PB4	TXD0			I/O	VDDIOP0		
PB5	RXD0			I/O	VDDIOP0		
PB6	TXD1	TCLK1		I/O	VDDIOP0		
PB7	RXD1	TCLK2		I/O	VDDIOP0		
PB8	TXD2			I/O	VDDIOP0		
PB9	RXD2			I/O	VDDIOP0		
PB10	TXD3	ISI_D8		I/O	VDDIOP1		
PB11	RXD3	ISI_D9		I/O	VDDIOP1		
PB12[1]	TXD5	ISI_D10		I/O	VDDIOP1		
PB13[1]	RXD5	ISI_D11		I/O	VDDIOP1		
PB14	DRXD			I/O	VDDIOP0		
PB15	DTXD			I/O	VDDIOP0		
PB16	TK0	TCLK3		I/O	VDDIOP0		RDY/BUSY signal for NANDFlash in the ROM boot
PB17	TF0	TCLk4		I/O	VDDIOP0		
PB18	TD0	TIOB4		I/O	VDDIOP0		
PB19	RD0	TIOB5		I/O	VDDIOP0		
PB20	RK0	ISI_D0		I/O	VDDIOP1		
PB21	RF0	ISI_D1		I/O	VDDIOP1		
PB22	DSR0	ISI_D2		I/O	VDDIOP1		
PB23	DCD0	ISI_D3		I/O	VDDIOP1		
PB24	DTR0	ISI_D4		I/O	VDDIOP1		
PB25	RI0	ISI_D5		I/O	VDDIOP1		
PB26	RTS0	ISI_D6		I/O	VDDIOP1		
PB27	CTS0	ISI_D7		I/O	VDDIOP1		
PB28	RTS1	ISI_PCK		I/O	VDDIOP1		
PB29	CTS1	ISI_VSYNC		I/O	VDDIOP1		
PB30	PCK0	ISI_HSYNC		I/O	VDDIOP1		
PB31	PCK1	ISI_MCK		I/O	VDDIOP1		

Note: 1. Not available in the 208-lead PQFP package.

10.3.3 PIO Controller C Multiplexing

Table 10-4. Multiplexing on PIO Controller C

PIO Controller C					Application Usage		
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Reset State**	**Power Supply**	**Function**	**Comments**
PC0		SCK3	AD0	I/O	VDDIOP0		
PC1		PCK0	AD1	I/O	VDDIOP0		
PC2[1]		PCK1	AD2	I/O	VDDIOP0		
PC3[1]		SPI1_NPCS3	AD3	I/O	VDDIOP0		
PC4	A23	SPI1_NPCS2		A23	VDDIOM		
PC5	A24	SPI1_NPCS1		A24	VDDIOM		
PC6	TIOB2	CFCE1		I/O	VDDIOM		
PC7	TIOB1	CFCE2		I/O	VDDIOM		
PC8	NCS4/CFCS0	RTS3		I/O	VDDIOM		
PC9	NCS5/CFCS1	TIOB0		I/O	VDDIOM		
PC10	A25/CFRNW	CTS3		A25	VDDIOM		
PC11	NCS2	SPI0_NPCS1		I/O	VDDIOM		
PC12[1]	IRQ0	NCS7		I/O	VDDIOM		
PC13	FIQ	NCS6		I/O	VDDIOM		
PC14	NCS3/NANDCS	IRQ2		I/O	VDDIOM		
PC15	NWAIT	IRQ1		I/O	VDDIOM		
PC16	D16	SPI0_NPCS2		I/O	VDDIOM		
PC17	D17	SPI0_NPCS3		I/O	VDDIOM		
PC18	D18	SPI1_NPCS1		I/O	VDDIOM		
PC19	D19	SPI1_NPCS2		I/O	VDDIOM		
PC20	D20	SPI1_NPCS3		I/O	VDDIOM		
PC21	D21	EF100		I/O	VDDIOM		
PC22	D22	TCLK5		I/O	VDDIOM		
PC23	D23			I/O	VDDIOM		
PC24	D24			I/O	VDDIOM		
PC25	D25			I/O	VDDIOM		
PC26	D26			I/O	VDDIOM		
PC27	D27			I/O	VDDIOM		
PC28	D28			I/O	VDDIOM		
PC29	D29			I/O	VDDIOM		
PC30	D30			I/O	VDDIOM		
PC31	D31			I/O	VDDIOM		

Note: 1. Not available in the 208-lead PQFP package.

10.4 Embedded Peripherals

10.4.1 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.4.2 Two-wire Interface

- Master mode supported
- One, two or three bytes for slave address
- Sequential read/write operations

10.4.3 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit

- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.4.4 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.4.5 Timer Counter

- Six 16-bit Timer Counter Channels
- Wide range of functions including
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.4.6 Multimedia Card Interface

- One double-channel MultiMedia Card Interface
- Compatibility with MultiMedia Card Specification Version 2.2
- Compatibility with SD Memory Card Specification Version 1.0
- Compatibility with SDIO Specification Version V1.0.
- Card clock rate up to Master Clock divided by 2
- Embedded power management to slow down clock rate when not used
- MCI has two slots, each supporting
  - One slot for one MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
- Support for stream, block and multi-block data read and write

10.4.7 USB Host Port

- Compliance with Open HCI Rev 1.0 Specification
- Compliance with USB V2.0 Full-speed and Low-speed Specification
- Supports both Low-Speed 1.5 Mbps and Full-speed 12 Mbps devices
- Root hub integrated with two downstream USB ports in the 217-LFBGA package
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the Matrix

10.4.8 USB Device Port

- USB V2.0 full-speed compliant, 12 MBits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 2,432-byte dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
  - Endpoint 0 and 3: 64 bytes, no ping-pong mode
  - Endpoint 1 and 2: 64 bytes, ping-pong mode
  - Endpoint 4 and 5: 512 bytes, ping-pong mode
- Embedded pad pull-up

10.4.9 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 MBits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data in

10.4.10 Image Sensor Interface

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats

- Preview scaler to generate smaller size image
- Programmable frame capture rate

10.4.11 Analog-to-Digital Converter

- 4-channel ADC
- 10-bit 100 Ksamples/sec. Successive Approximation Register ADC
- -2/+2 LSB Integral Non Linearity, -1/+2 LSB Differential Non Linearity
- Individual enable and disable of each channel
- External voltage reference for better accuracy on low voltage inputs
- Multiple trigger source – Hardware or software trigger – External trigger pin – Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer – Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four analog inputs shared with digital signals

11. Package Drawings

Figure 11-1. 217-ball LFBGA Package Drawing

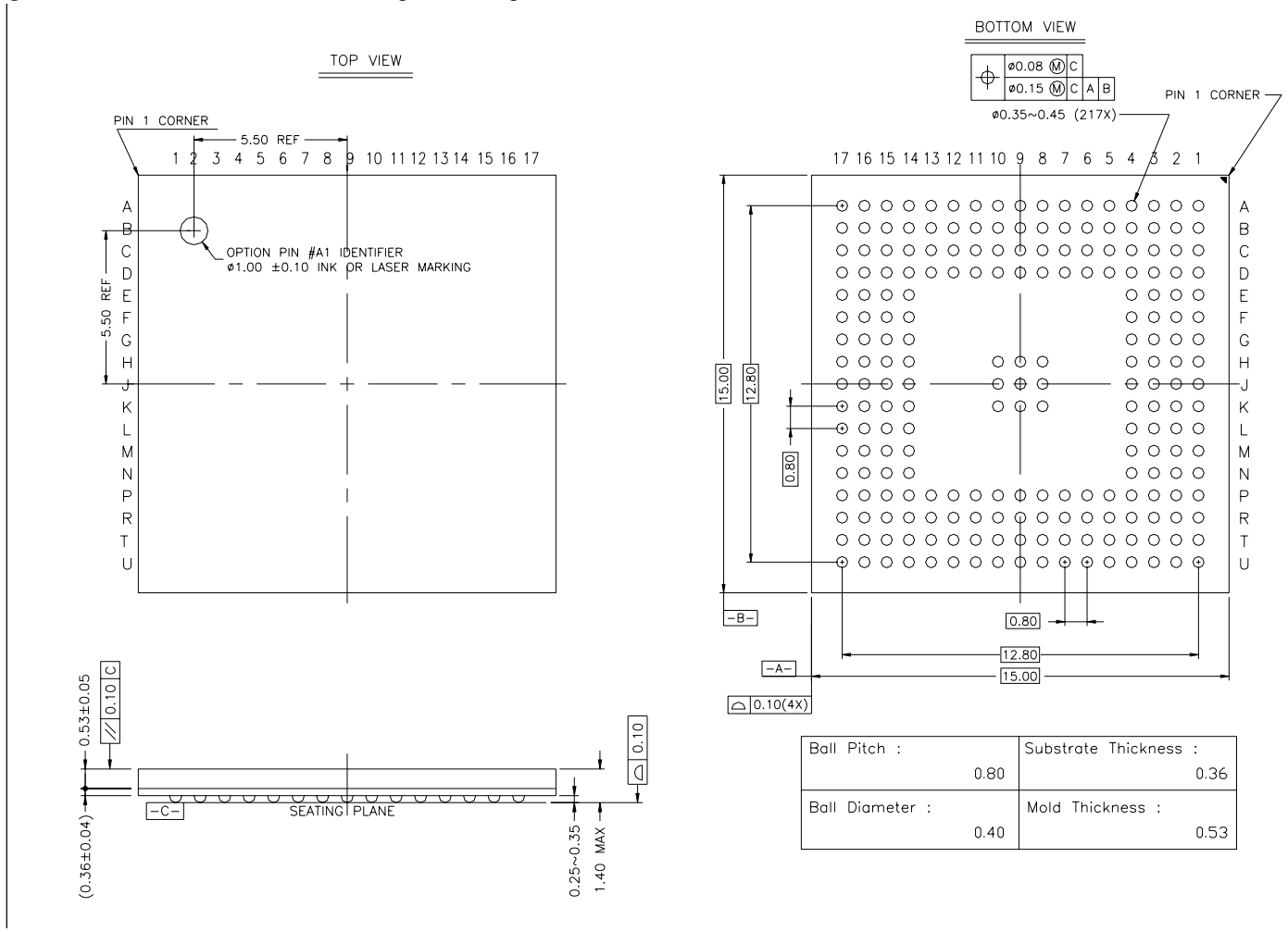
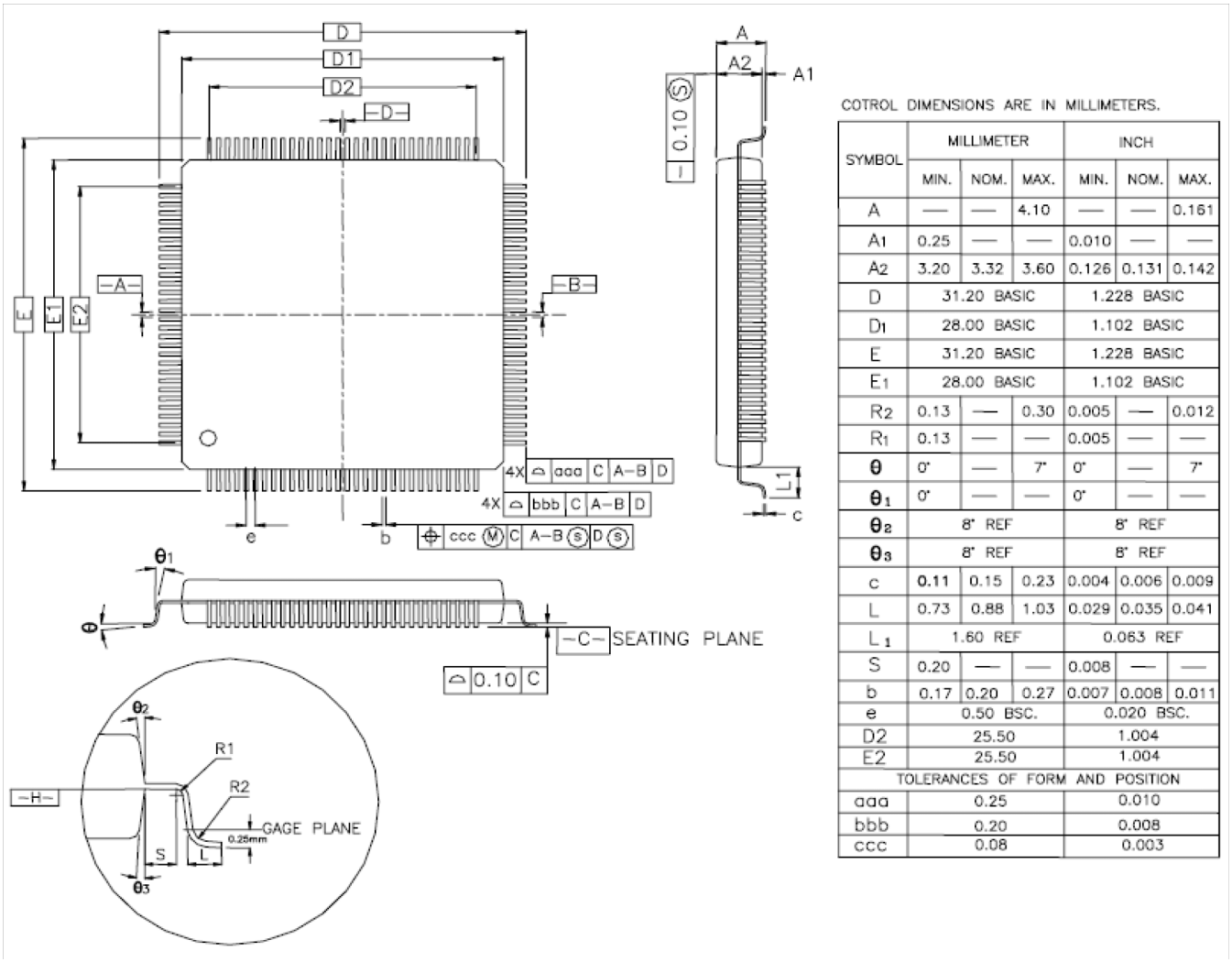


Figure 11-2. 208-lead TQFP Package Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A1	0.25	—	—	0.010	—	—
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E1	28.00 BASIC			1.102 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2	8° REF			8° REF		
θ3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

12. AT91SAM9260 Ordering Information

Table 12-1. AT91SAM9260 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM9260-QU	PQFP208	Green	Industrial -40°C to 85°C
AT91SAM9260-CJ	BGA217	RoHS-compliant	

13. Revision History

Table 13-1. Revision History

Revision	Comments	Change Request Ref.
6221AS	First issue.	
6221BS	Power consumption figures updated with current values in Section 5.2 ”Power Consumption” on page 14. Change to pin 47 in Section 4-1 ”Pinout for 208-pin PQFP Package” on page 11.	2843

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6221BS–ATARM–12-Jun-06