CDB4362

Evaluation Board for CS4362

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 receives S/PDIF & EIAJ-340 compatible digital audio
- Headers for external audio input for either PCM or DSD
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

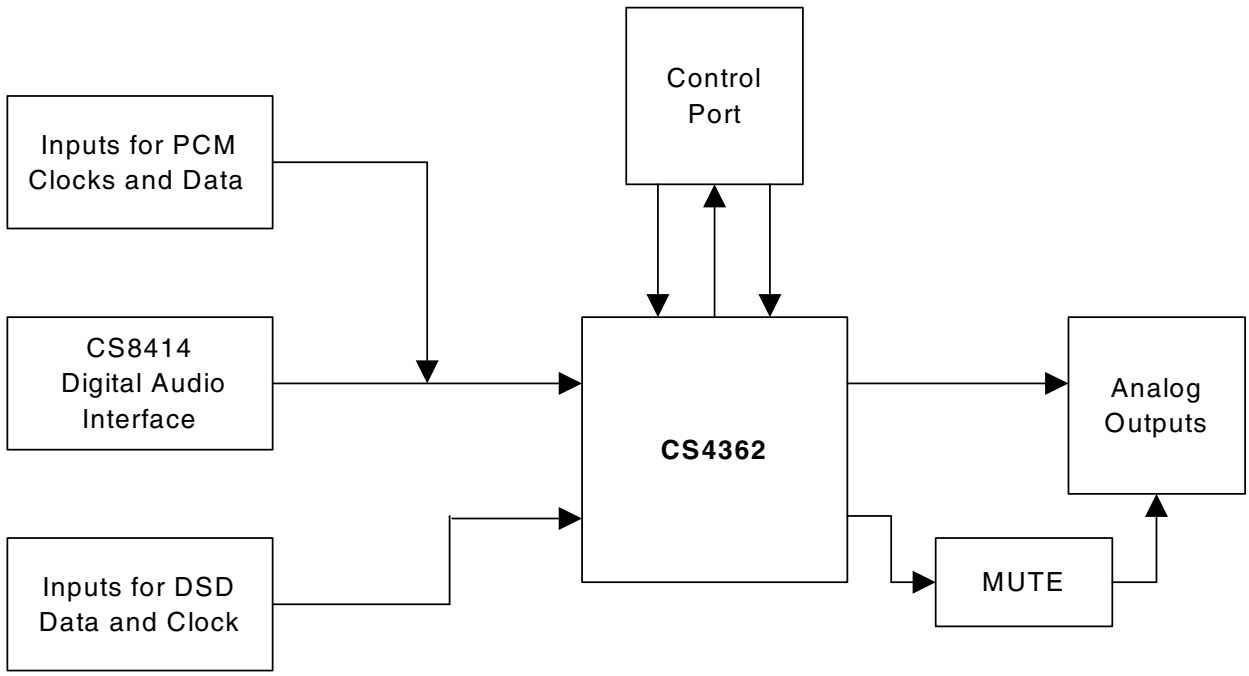
Description

The CDB4362 evaluation board is an excellent means for quickly evaluating the CS4362 24-bit, six channel D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4362 (for control port mode only) and a power supply. Analog line level outputs are provided via RCA phono jacks.

The CS8414 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept S/PDIF and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4362 Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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CDB4362 SYSTEM OVERVIEW

The CDB4362 evaluation board is an excellent means of quickly evaluating the CS4362. The CS8414 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply either PCM or DSD clocks and data through headers for system development.

The CDB4362 schematic has been partitioned into 13 schematics shown in Figures 3 through 15. Each partitioned schematic is represented in the system diagram shown in Figure 2. Notice that the system diagram also includes the interconnections between the partitioned schematics.

1. CS4362 DIGITAL TO ANALOG CONVERTER

A description of the CS4362 is included in the CS4362 datasheet.

2. CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 4. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), and a 256 Fs master clock. The CS8414 data format has been configured for I^2S. The operation of the CS8414 and a discussion of the digital audio interface is included in the CS8414 datasheet.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 4. However, both inputs cannot be driven simultaneously.

3. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 14-pin and 16-pin headers, J14 and J15. Header J15 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 5.

Header J14 allows the evaluation board to accept externally generated DSD data and clock. The schematic for the clock/data input is shown in Figure 6. A synchronous MCLK must still be provided via header J15. Please see the CS4362 datasheet for more information on clocking formats.

4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by seven binding posts (GND, +5V, VLS, VLC, VD, +18V and -18V), see Figure 15. The VLC and VLS supplies can be jumpered to the +5V binding post for ease of use. VD and VA should be set to the recommended voltages stated in the CS4362 datasheet. +18V and -18V supply power to the op-amps and can be +/-5 to +/-18 volts (must be +/-18 V when filter 2 is selected).

WARNING: Refer to the CS4362 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

5. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4362 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 details the connections to the CS4362 and Figures 16, 17, & 18 show the placement and layout. The decoupling capacitors are located as close to the CS4362 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. CONTROL PORT SOFTWARE

The CDB4362 is shipped with Windows 95/98/ME based software for interfacing with the CS4362 control port via the DB25 connector, J1 (Windows NT and 2000 not currently supported). The software can be used to communicate with the CS4362

in either SPI® or I²C mode; however, in SPI mode the CS4362 registers are write-only.

7. DSD OPERATION

The CDB4362 supports Direct Stream Digital (DSD) operation through the header for external clocks and data, J14. The CS4362 must be placed into the DSD mode and headers J6 and J18 must be set accordingly. See Table 2 for more information.

8. ANALOG OUTPUT FILTER

The analog output filter on the CDB4362 has been designed to add flexibility when evaluating the CS4362. The output filter was designed in an optional two stage format, with the first optional stage being an instrumentation amplifier design and the second is a 2-pole butterworth filter.

The 2-pole filter is designed to have the in-band impedance matched between the positive and negative legs. It also provides a balanced to single ended conversion for standard un-balanced outputs.

The instrumentation amplifier is optionally inserted by changing the FILT jumpers to position 2 (selectable per channel by J37 & 38, J34 & 35, etc.). This instrumentation amplifier incorporates a 5x gain (+14dB) which effectively lowers the noise contribution of the 2-pole filter which improves the overall dynamic range of the system. The gain of this stage is determined from the following equation:

$$GAIN = 1 + \frac{2(R)}{R_2}$$

The resistor designated by R_2 (see Figure 1) can be adjusted to change the gain of the instrumentation amp. The feedback resistors on the two sides of the instrumentation amp 'R' must be equal.

A resistor divider has been placed before the RCA jack which brings the signal level back to 2 Vrms (selectable per channel with jumpers J21, J22, etc.).

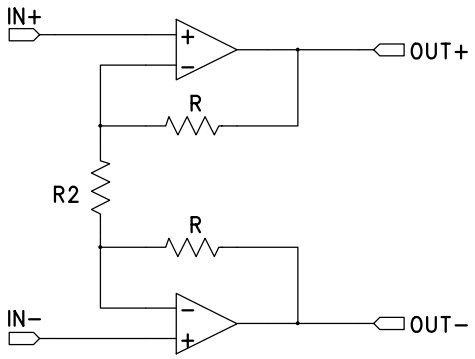

Figure 1. Instrumentation Amplifier Configuration

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 Volt power
VD	Input	+ 2.5 to +5V power for the CS4362 digital supply
VLS	Input	+ 1.8 to +5V power for the CS4362 serial interface
VLC	Input	+ 1.8 to +5V power for the CS4362 control interface
-18V	Input	-18 to -5V negative supply for the op-amps
+18V	Input	+5 to +18V positive supply for the op-amps
GND	Input	Ground connection from power supply
SPDIF INPUT - J2	Input	Digital audio interface input via coax
SPDIF INPUT - OPTO-1	Input	Digital audio interface input via optical
PCM INPUT - J15	Input	Input for master, serial, left/right clocks and serial data
DSD INPUT - J14	Input	Input for DSD data and clock
PC Port	Input/Output	Parallel connection to PC for SPI / I²C control port signals
EXT CTRL I/O	Input/Output	I/O for SPI / I²C control port signals
OUTA1 to OUTB3	Output	Channels 1A to 3B line level analog outputs

Table 1. System Connections

9. ERRATA

CDB4362 Revision A.0

The CDB4362 revision A.0 has the following errata. The silk-screens for Z4 and Z5 are reversed. The cathode band marks on the silkscreen are facing the wrong direction. The zener devices have been placed according to the schematic and not the silkscreen.

The three TST pins of the CS4362 (pins 14, 44, and 45) were left floating. As the CS4362 datasheet says, these three pins should be tied to ground.

CDB4362 Revision B.0

The CDB4362 revision B.0 has the following errata. The three TST pins of the CS4362 (pins 14, 44, and 45) were left floating. As the CS4362 datasheet says, these three pins should be tied to ground.

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
J3	Selects source of voltage for the VLC supplies	VLC *+5V	Voltage source is VLC binding post Voltage source is +5V binding post
J7	Selects source of voltage for the VLS supplies	VLS *+5V	Voltage source is VLS binding post Voltage source is +5V binding post
J47	Selects source of voltage for the VD supply	*VD +5V	Voltage source is VD binding post Voltage source is +5V binding post
J6	Clock Source Select	*CS8414 External	CS8414 provides PCM inputs to CS4362 PCM or DSD inputs are provided externally
J18	Input Mode Select	*PCM DSD	Selects PCM input mode Selects DSD input mode (via J16)
J4	Stand-Alone/Control Port Select	SA *CP	Stand-Alone Mode (No PC required) Control Port Mode (PC required)
J9	M0/AD0/CS	HI *LO	See CS4362 datasheet for details
J10	M1/SDA/CDIN	*HI LO	See CS4362 datasheet for details
J11	M2/SCL/CCLK	*HI LO	See CS4362 datasheet for details
J12	M3/DSD_CLK	HI *LO	See CS4362 datasheet for details
FILT	Filter select	1 *2	Selects standard 2-pole filter Inserts instrumentation-amp
J20	MUTEC routing	MUTEC1 MUTEC1,2,3 *INDV MUTE	MUTEC1 signal is routed to all channels MUTEC1,2,3 is routed per channel pair MUTEC signals are routed for individual mutes
0 Ohm after Q1 to Q6	Mute Enables	*SHUNTED OPEN	Enables the external mute circuit for each channel when 0 Ohm is present (default)

Table 2. CDB4362 Jumper Settings

*Default Factory Settings

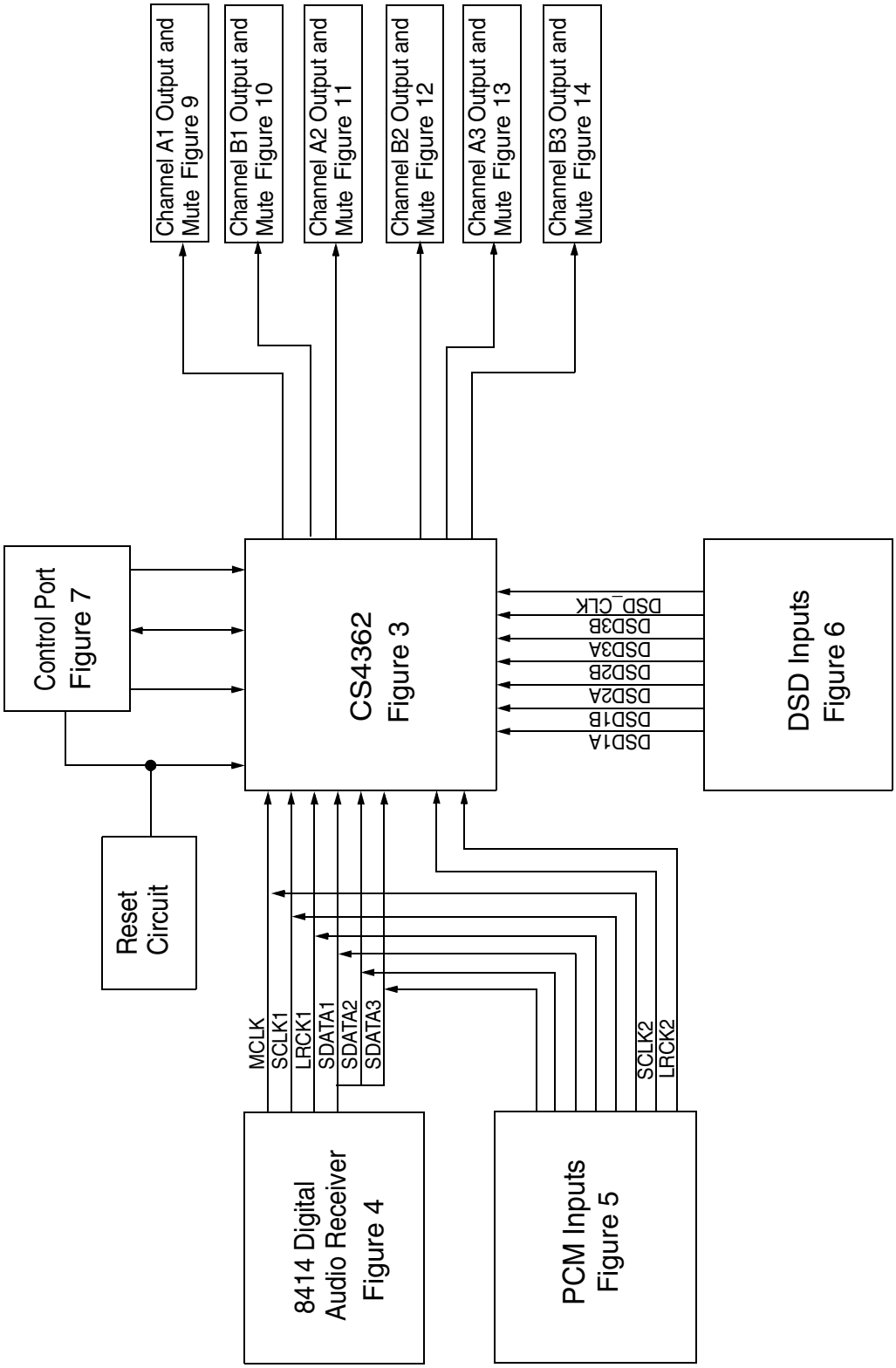

Figure 2. System Block Diagram and Signal Flow

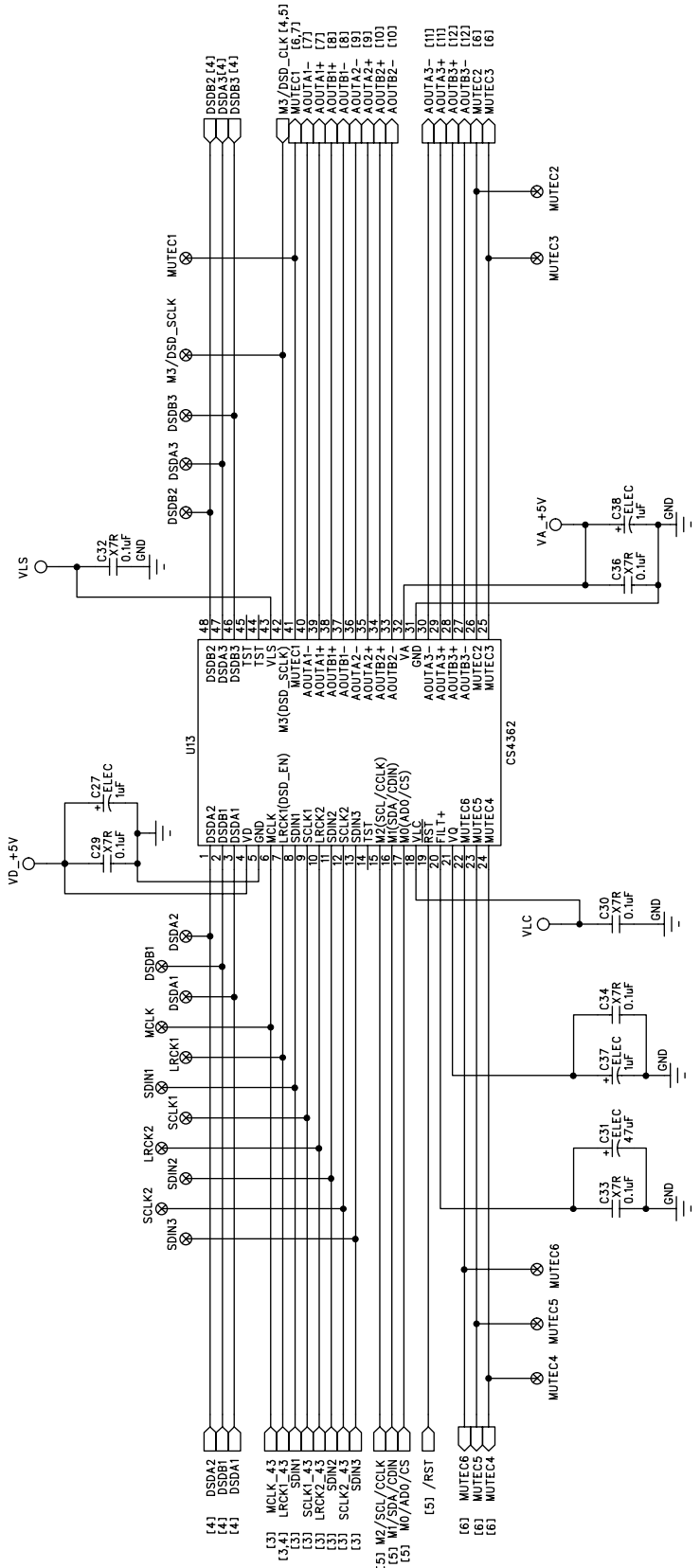

Figure 3. CS4362

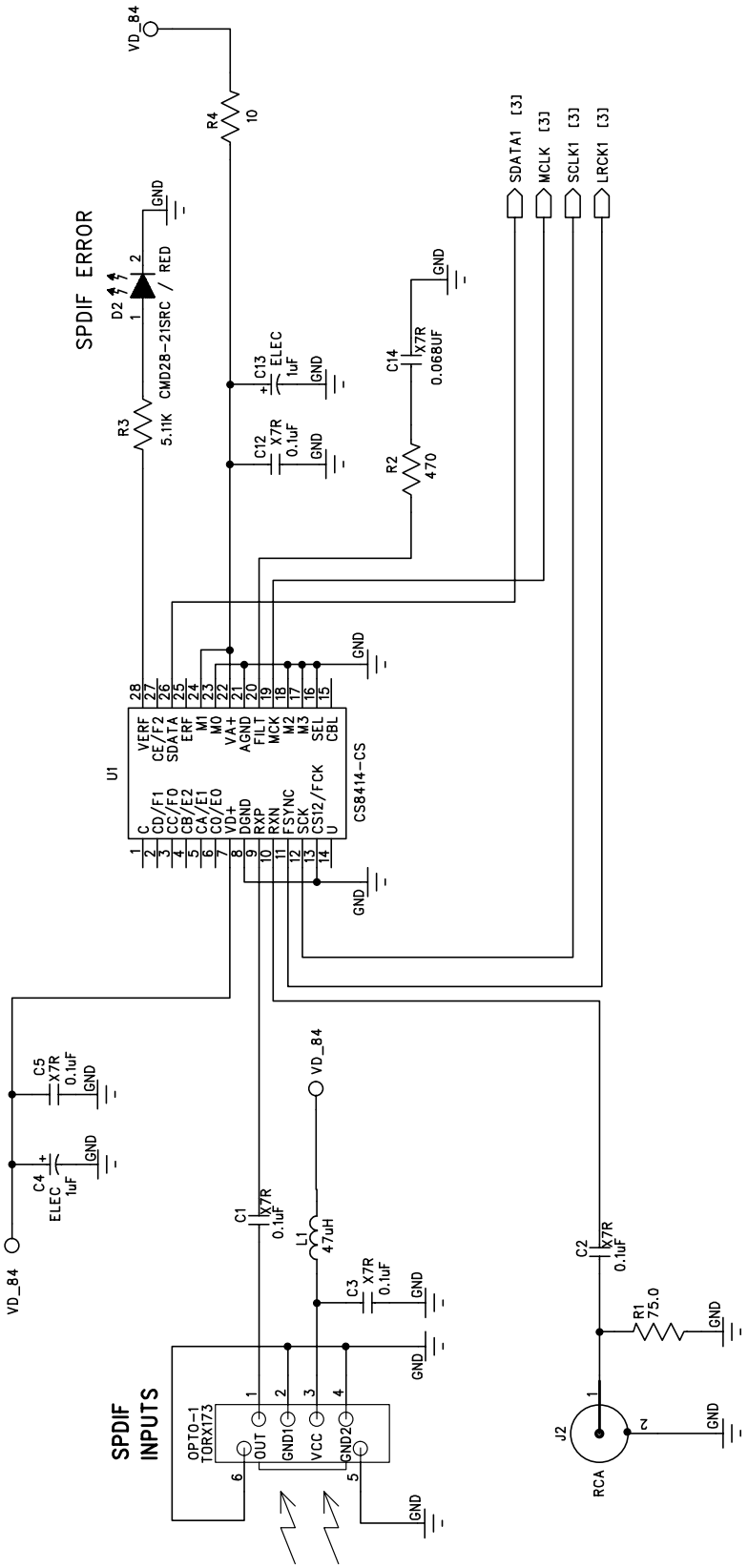

Figure 4. CS8414 Digital Audio Receiver

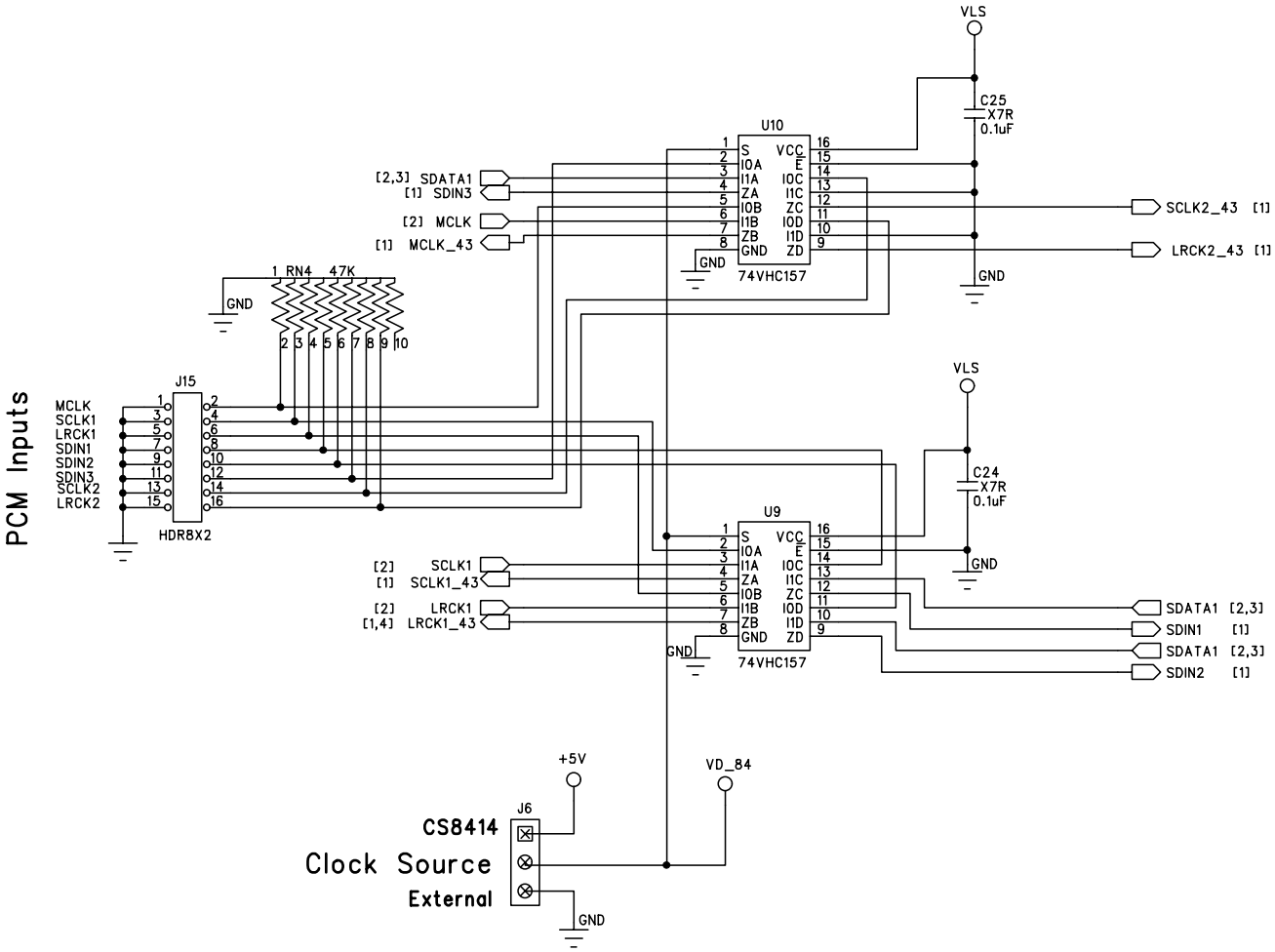

Figure 5. PCM Input Header

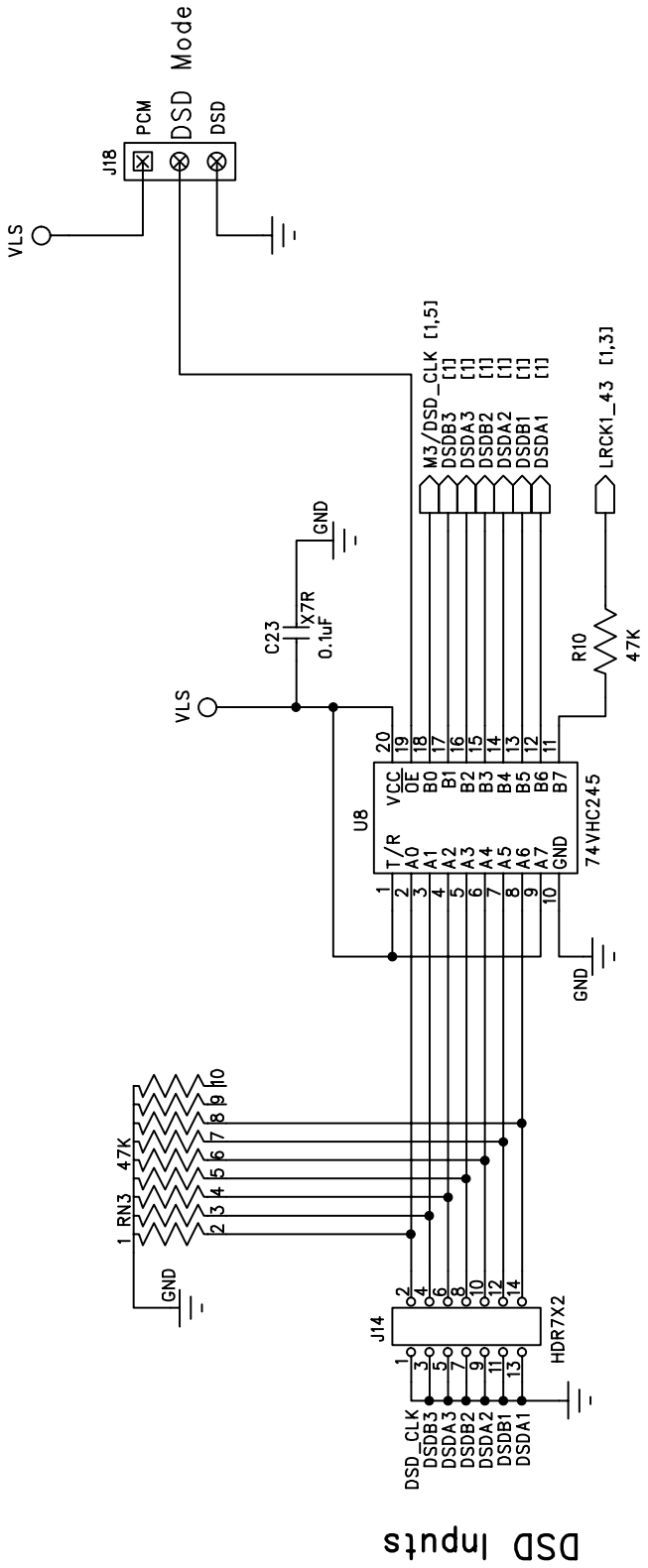

Figure 6. DSD Input Header

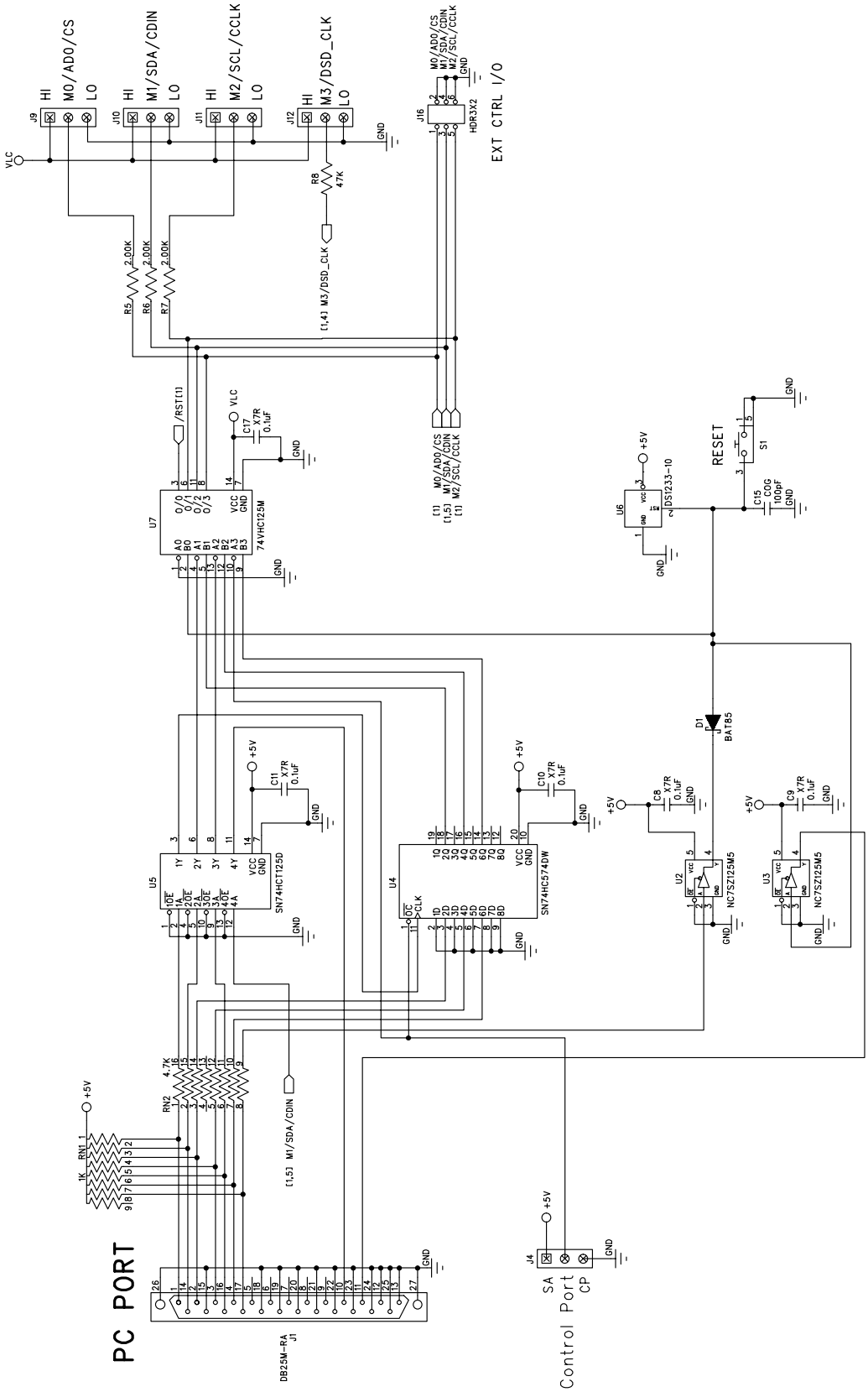

Figure 7. Control Port Interface

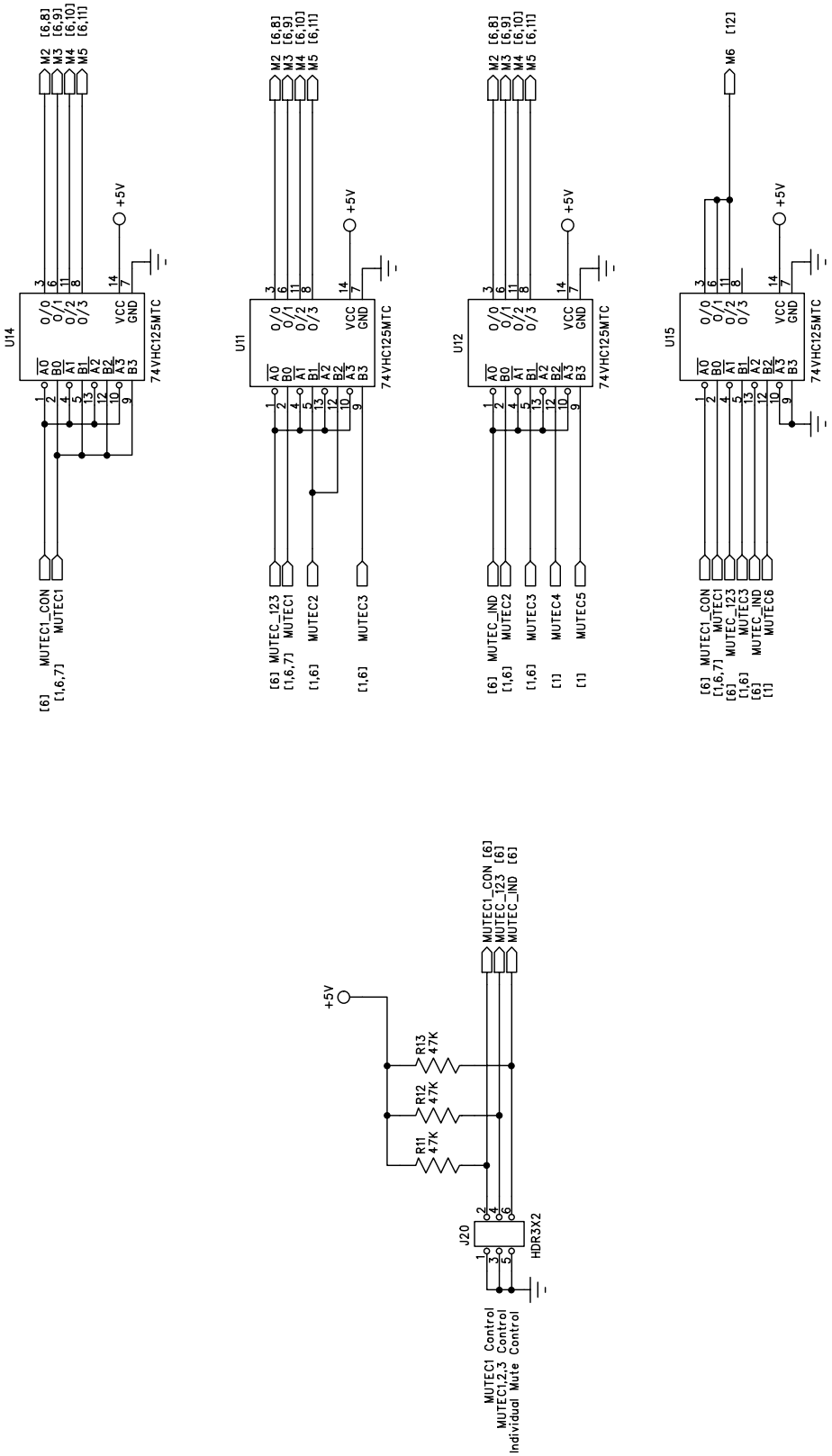

Figure 8. CDB Mute Control Selection and Routing

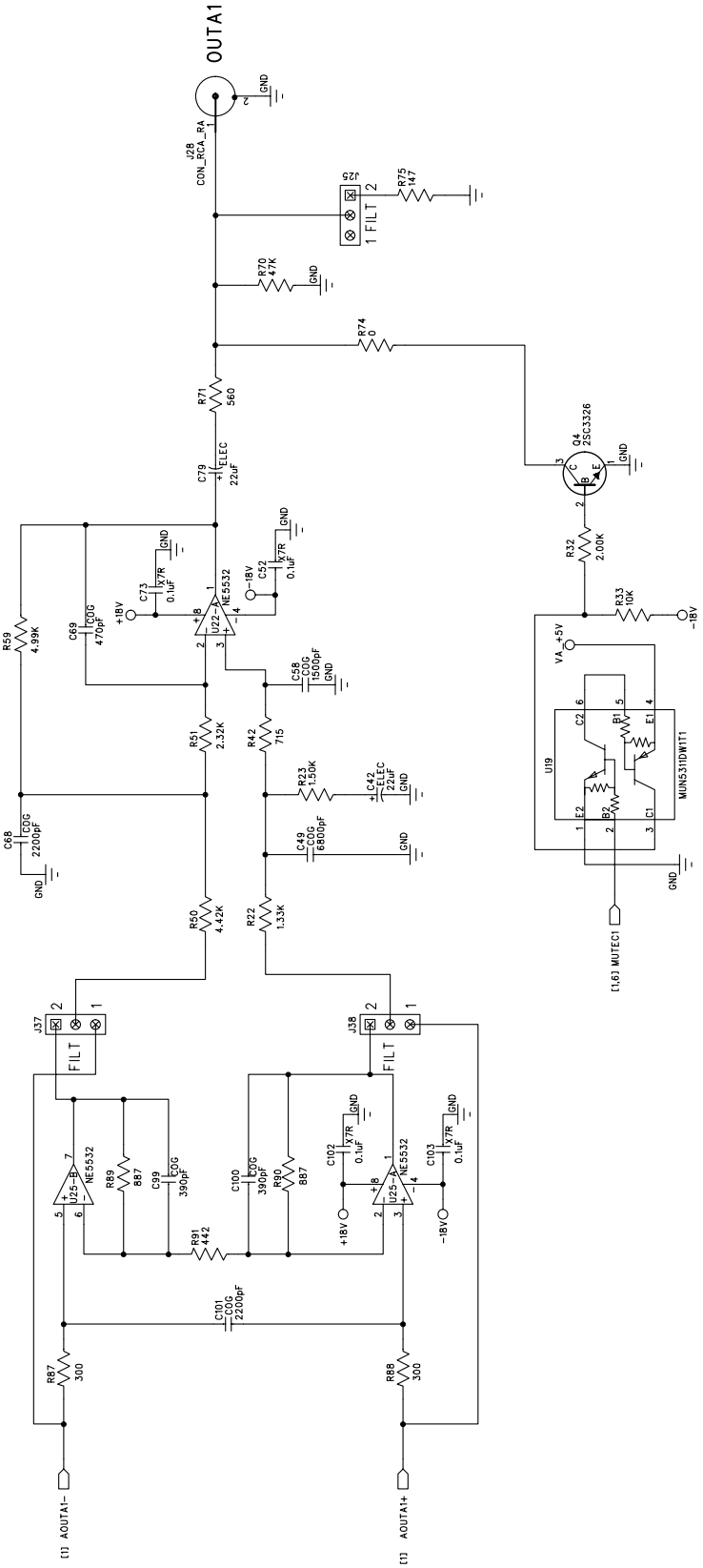

Figure 9. Channel A1 Output and Mute

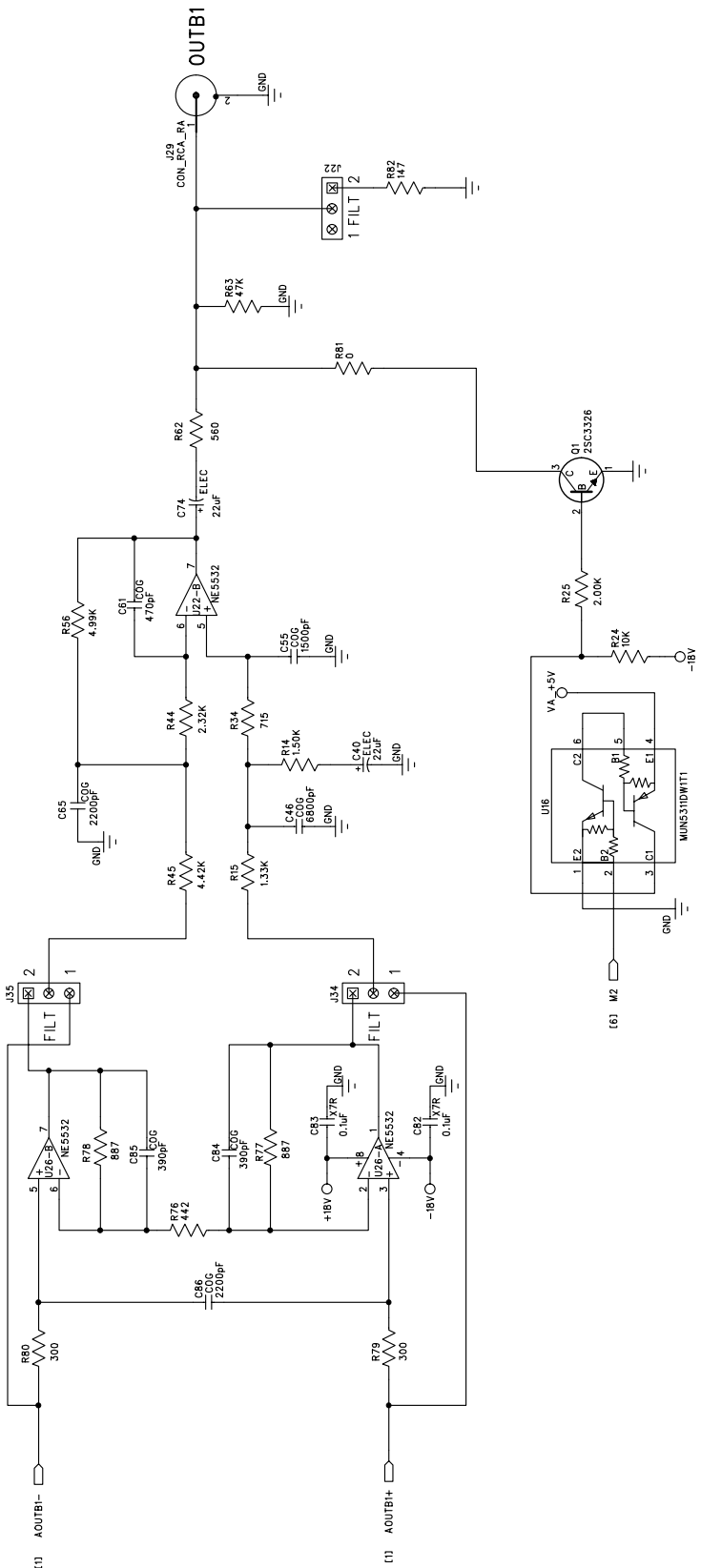

Figure 10. Channel B1 Output and Mute

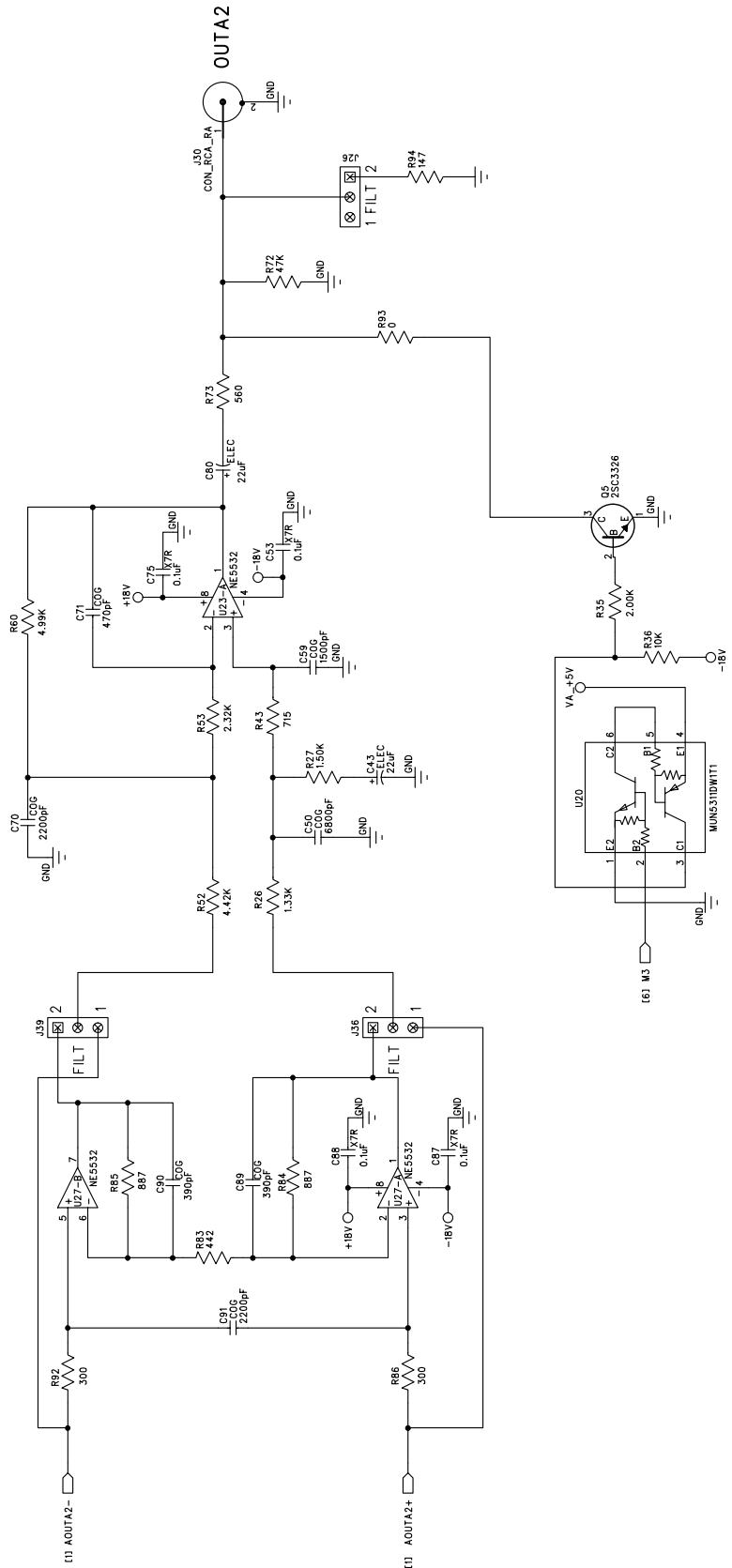

Figure 11. Channel A2 Output and Mute

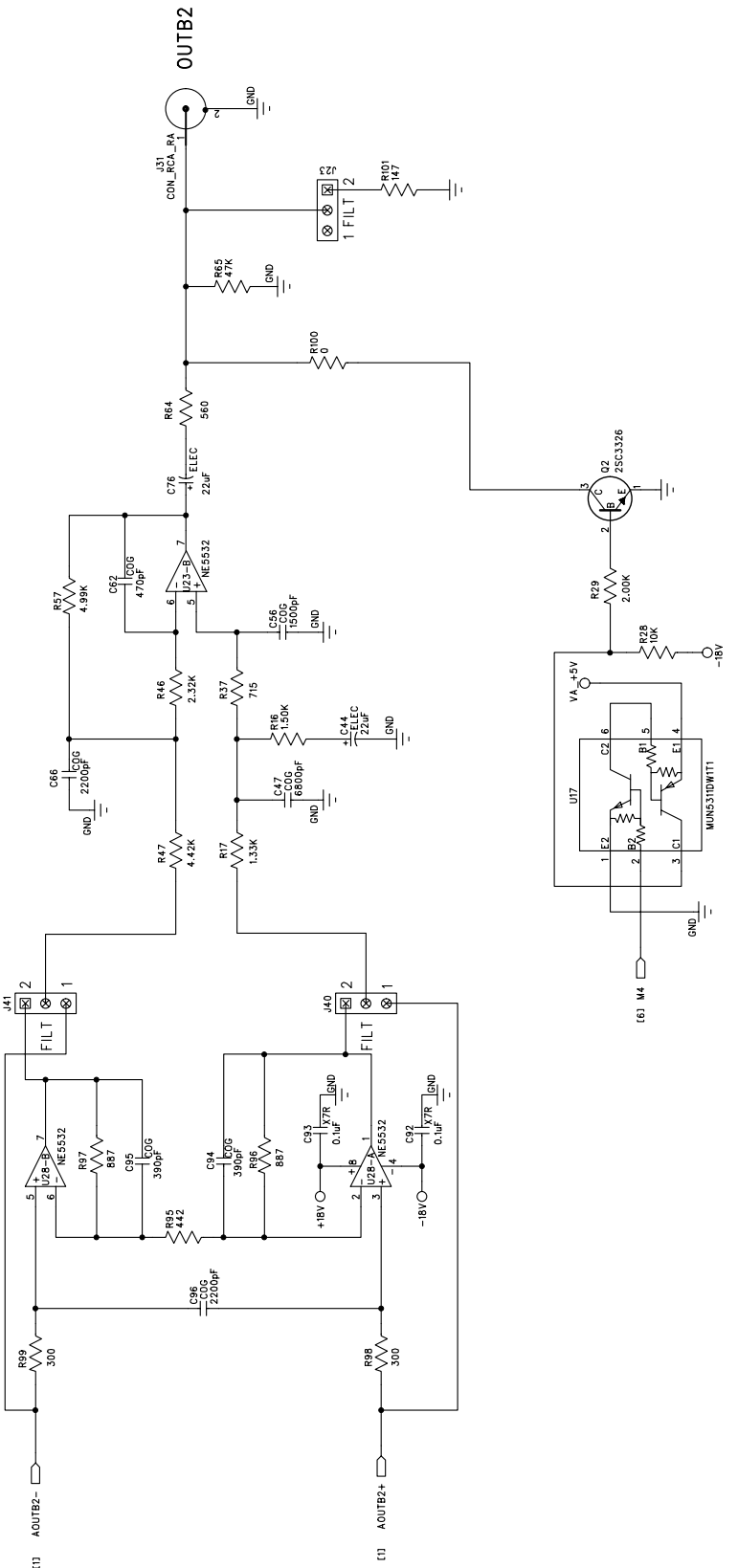

Figure 12. Channel B2 Output and Mute

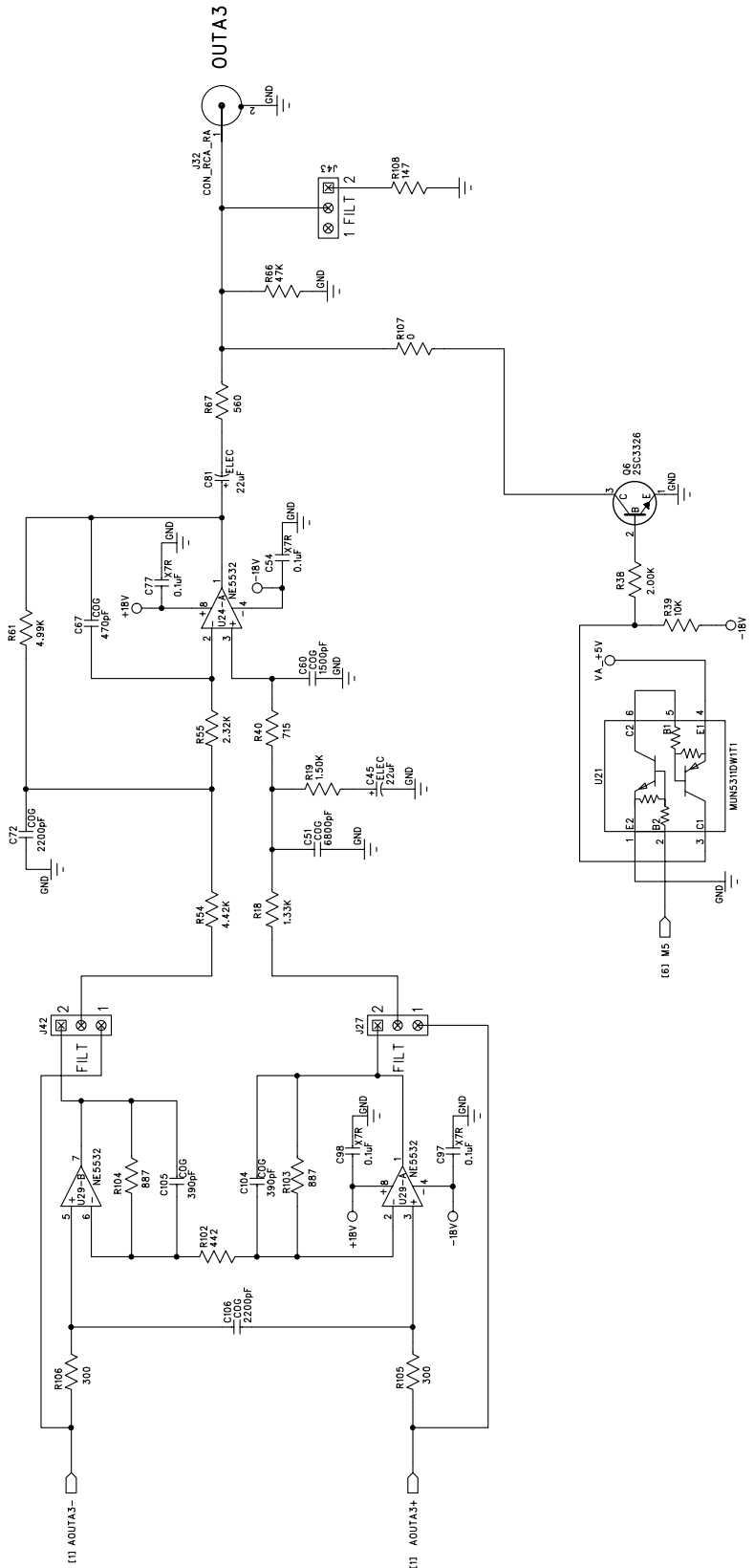

Figure 13. Channel A3 Output and Mute

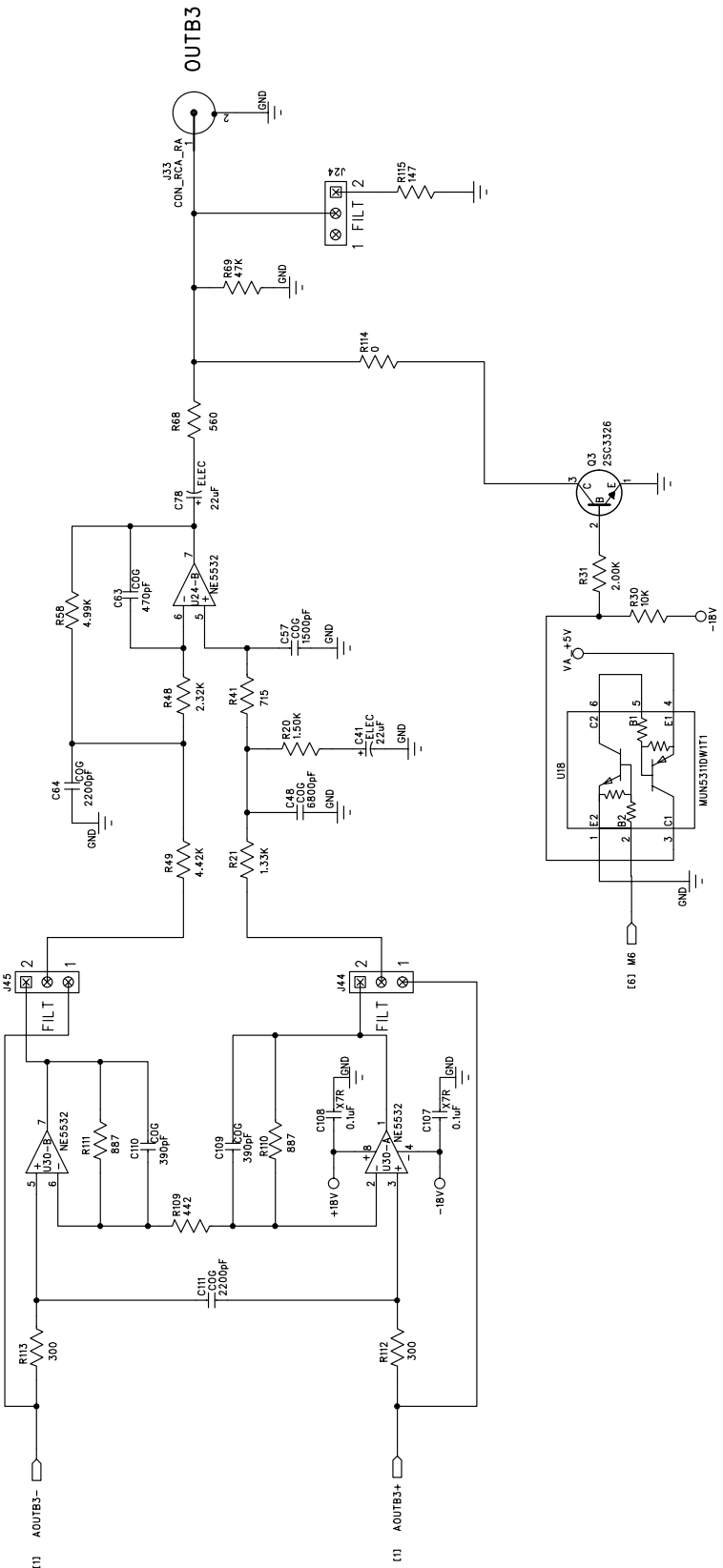

Figure 14. Channel B3 Output and Mute

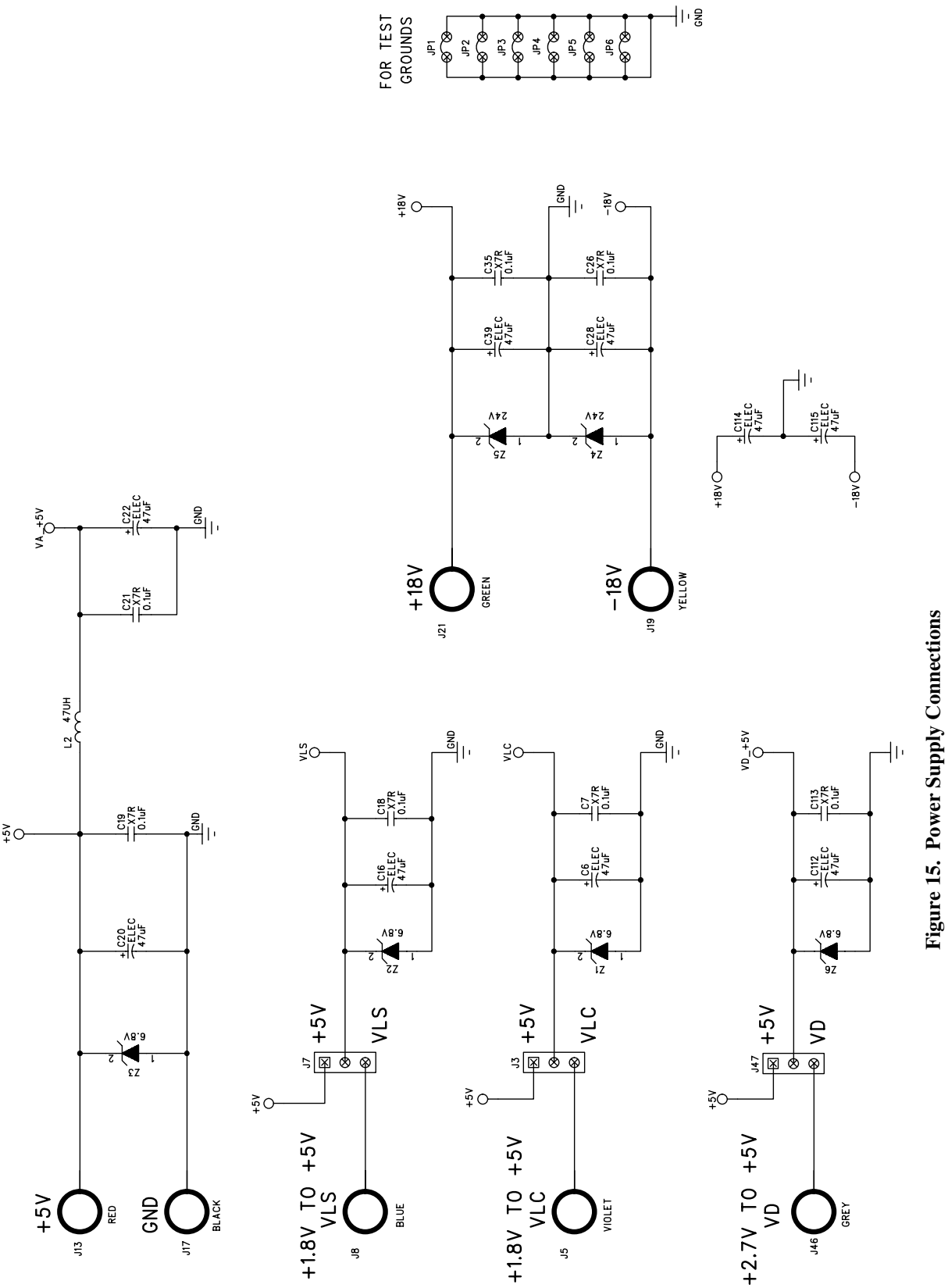

Figure 15. Power Supply Connections

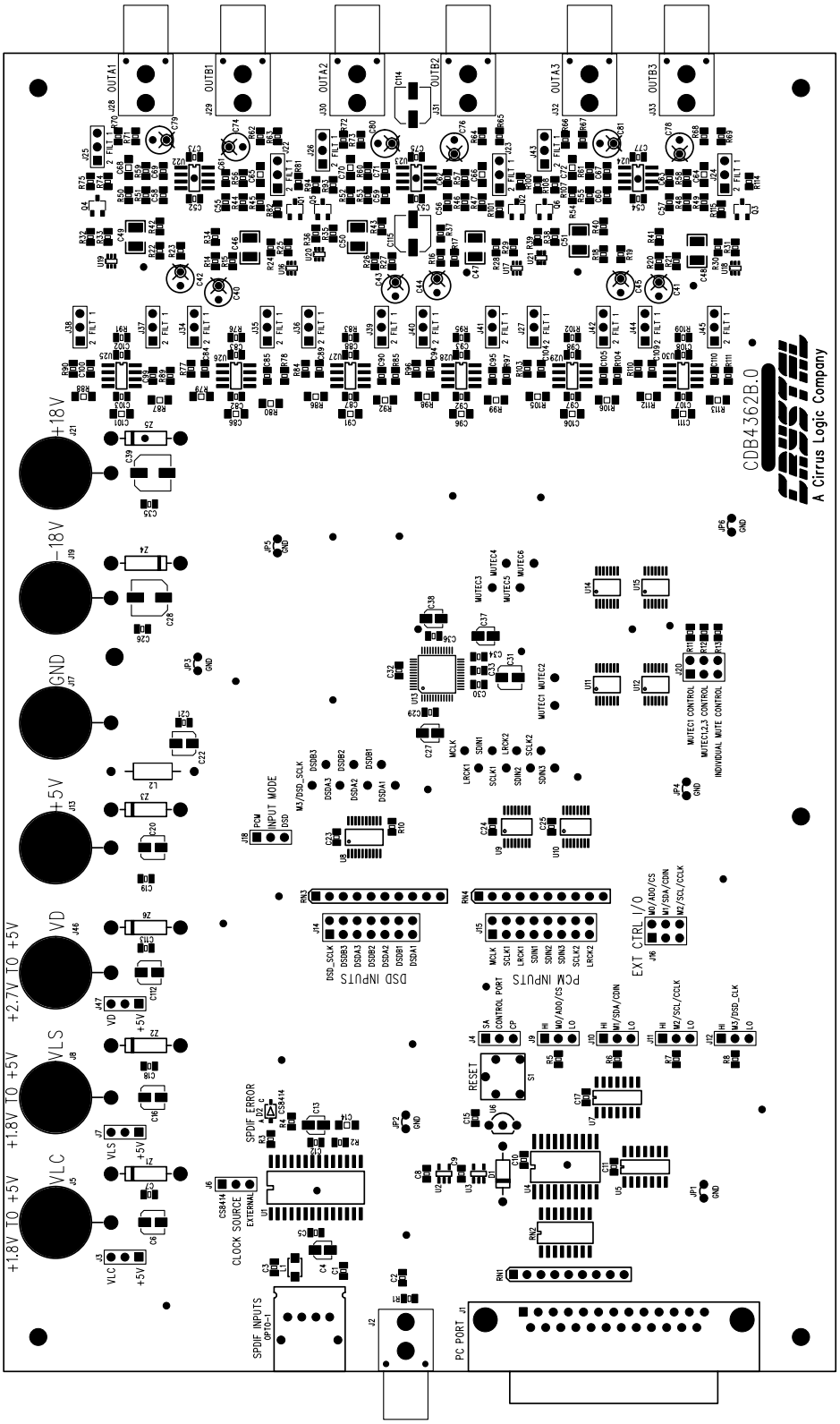

Figure 16. Silkscreen Top

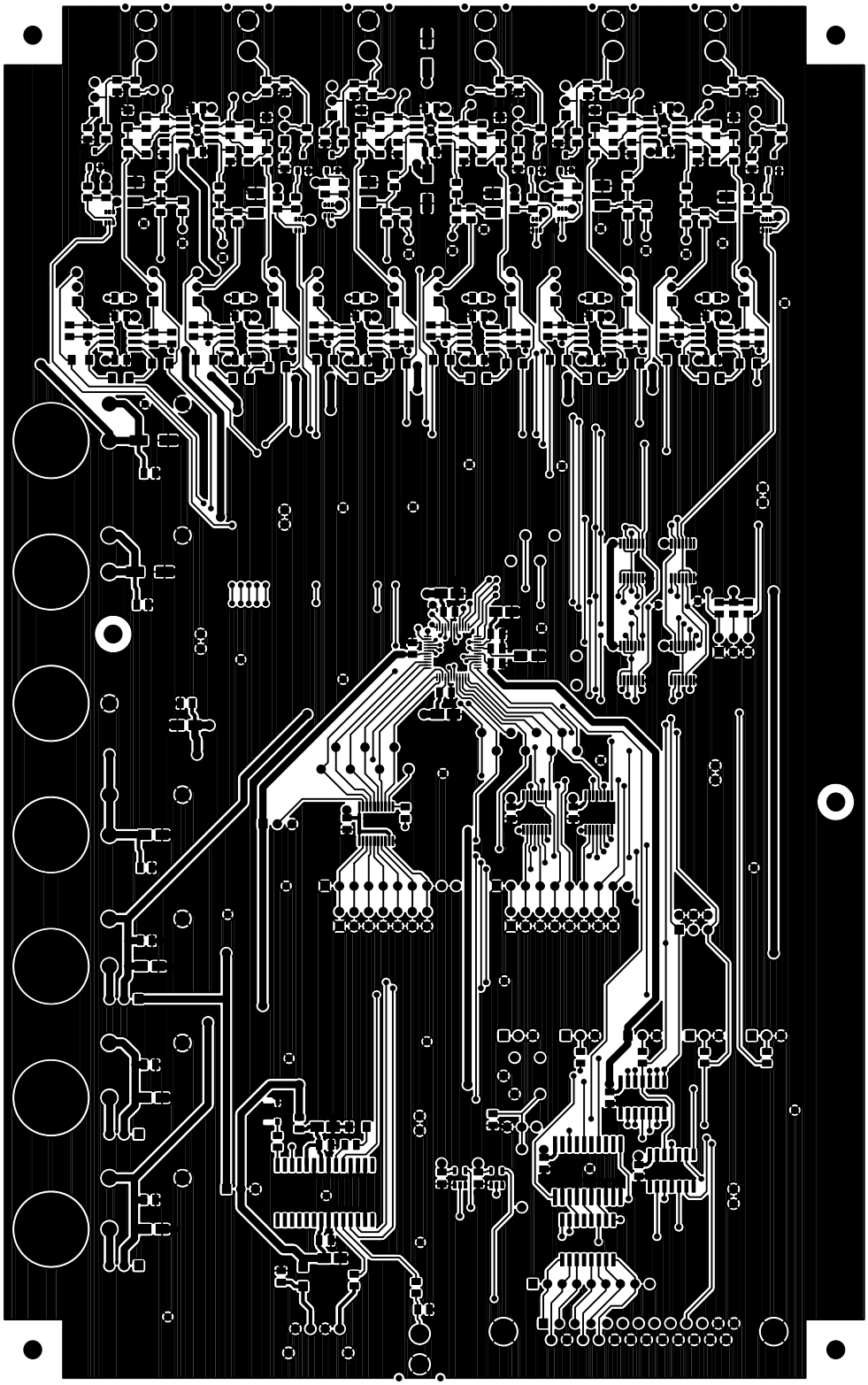

Figure 17. Top Side

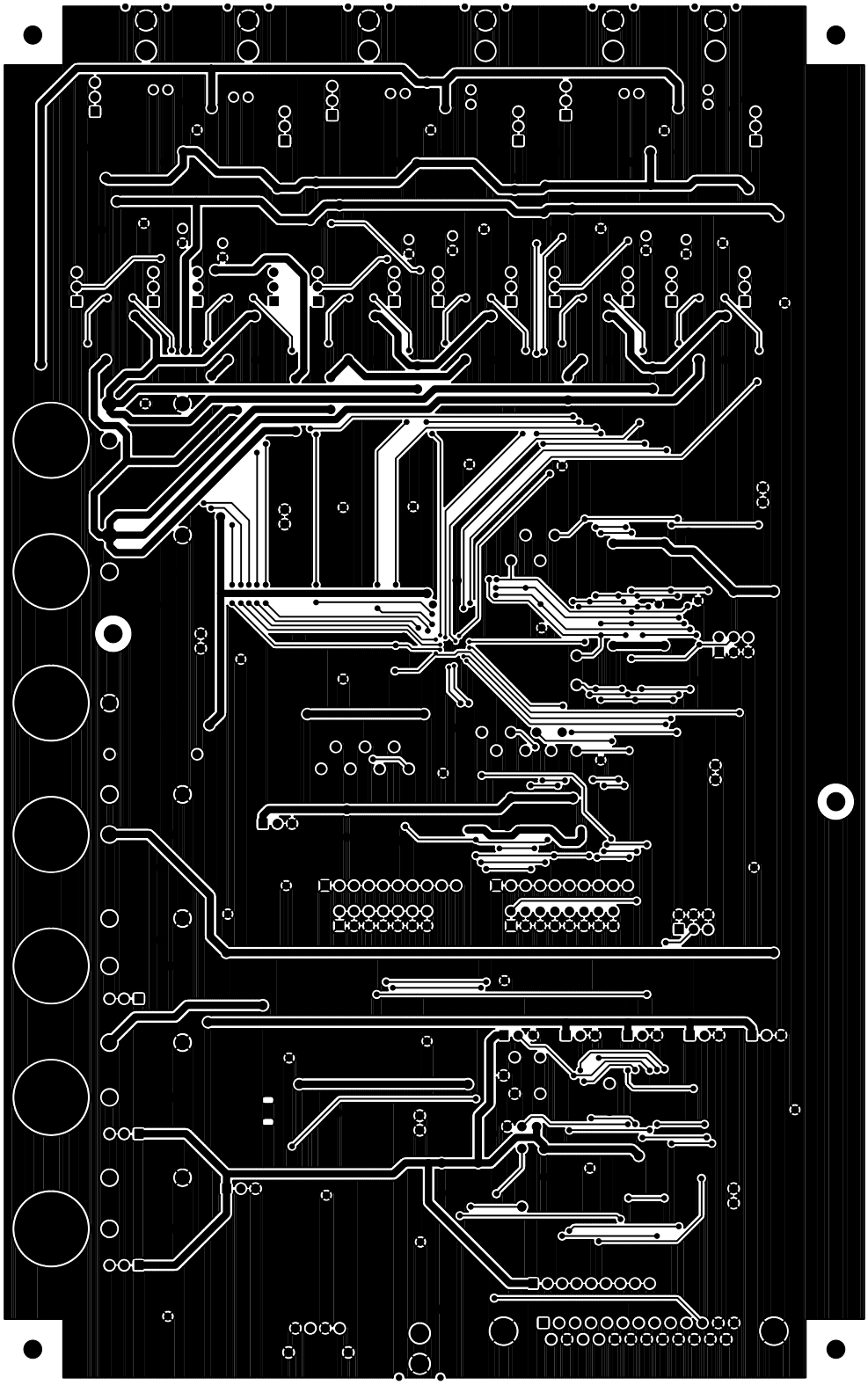

Figure 18. Bottom Side

• Notes •


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