FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-13508-2E

Linear IC Converter

CMOS

D/A Converter for Digital Tuning

(24-channel, 8-bit, on-chip OP amp)

MB88345

■ DESCRIPTION

The MB88345 incorporates twenty-four 8-bit D/A converter modules.

It also contains an output amplifier, allowing driving at large current.

Since the inputs data in serial mode, it requires only three control lines for data input and can be cascaded.

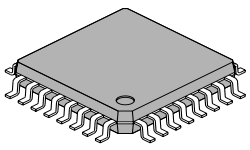
The MB88345 is suitable for applications such as electronic volume controls and replacement of semi-fixed resistors in tuning systems.

■ FEATURES

- Ultra-low power consumption (1.1 mW/ch : typical)
- Compact space-saving package (QFP-32)
- Contains 24-channel R-2R type 8-bit D/A converter
- On-chip analog output amps (sink current max. 1.0 mA, source current max. 1.0 mA)
- Analog output range : 0 V to V_{CC}
- Two separate power supply/ground lines for MCU interface block/operational amplifier output buffer block and D/A converter block
- Serial data input : maximum operating speed 2.5 MHz
- CMOS process

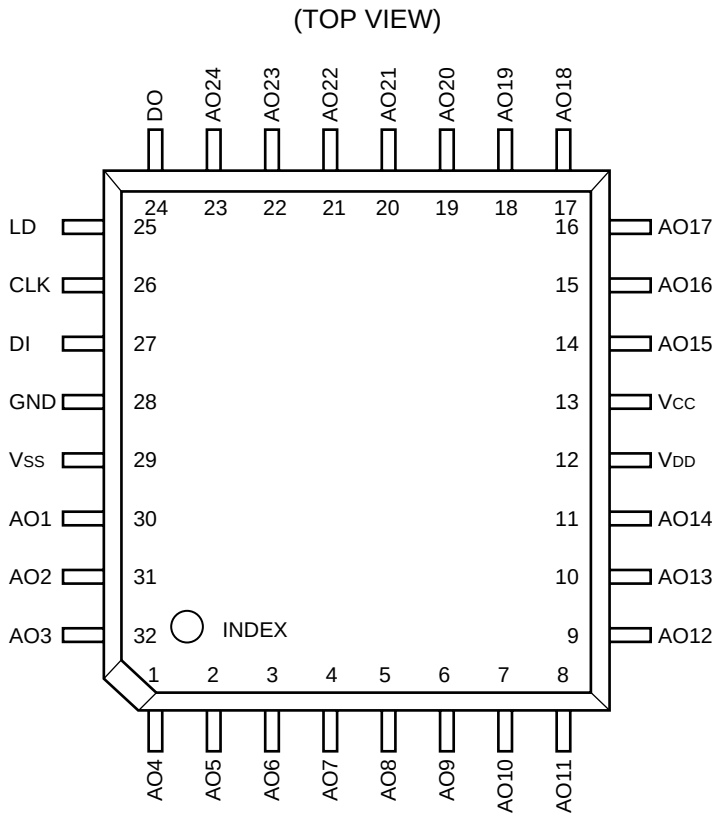
■ PACKAGE

32-pin Plastic QFP



(FPT-32P-M21)

■ PIN ASSIGNMENT

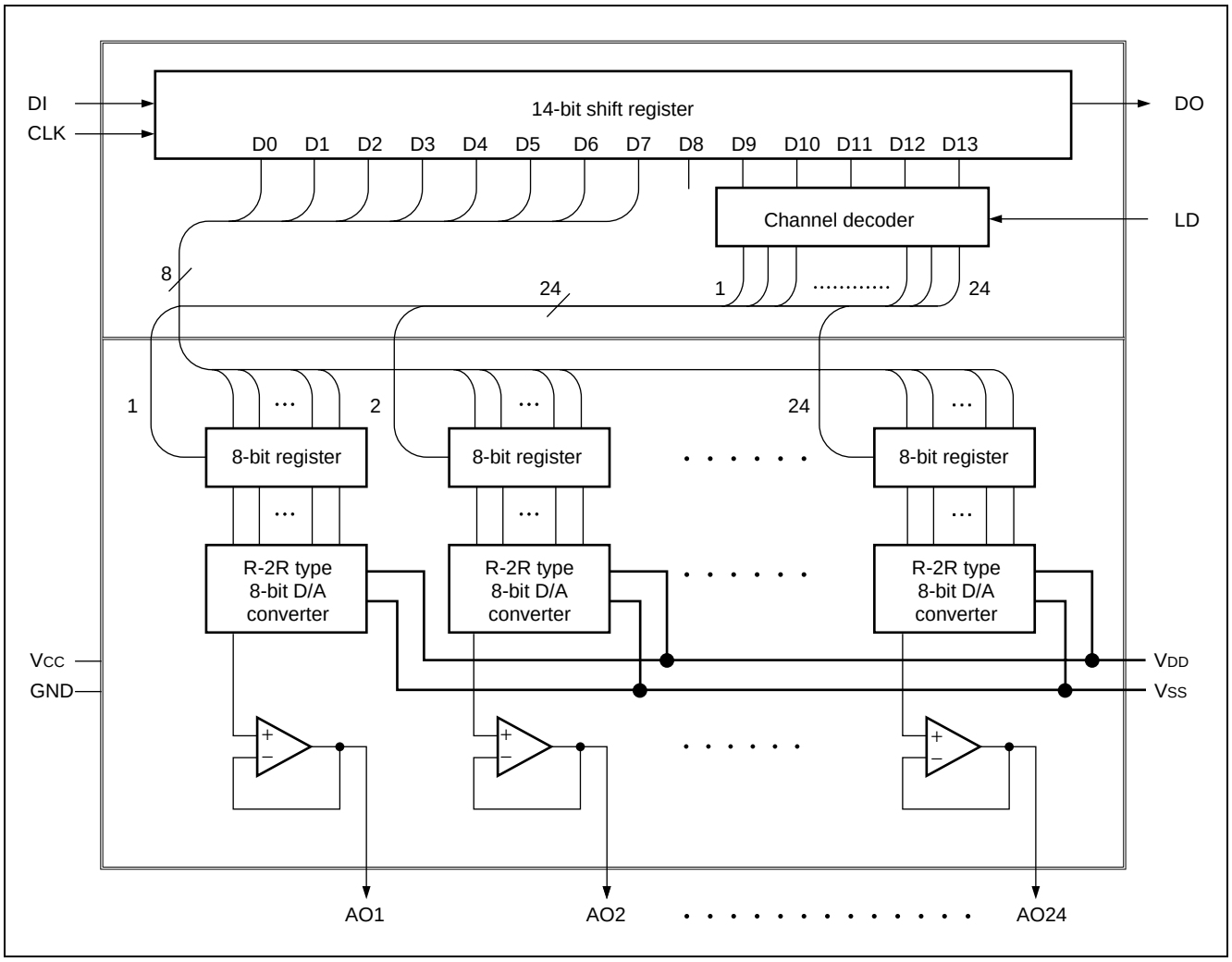


■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
27	DI*	I	Serial data input pin. This pin inputs serial data with a data length of 14 bits.
24	DO	O	This pin outputs the MSB data in the 14-bit shift register.
26	CLK*	I	Shift clock input pin. The input signal from the DI pin enters the 14-bit shift register at the rising edge of the shift clock pulse.
25	LD*	I	When the LD pin inputs the High-level signal, shift register value is loaded to the decoder and the D/A output register.
30 to 32 1 to 11 14 to 23	AO1 to AO3 AO4 to AO14 AO15 to AO24	O	8-bit D/A output with OP-amp.
13	V_{CC}	—	MCU interface and OP-amp power-supply pin
28	GND	—	MCU interface and OP-amp GND pin
12	V_{DD}	—	D/A converter power-supply pin
29	V_{SS}	—	D/A converter GND pin

* : DI, CLK, LD pins should be fixed with “Low”level while no data are transferred.

■ BLOCK DIAGRAM

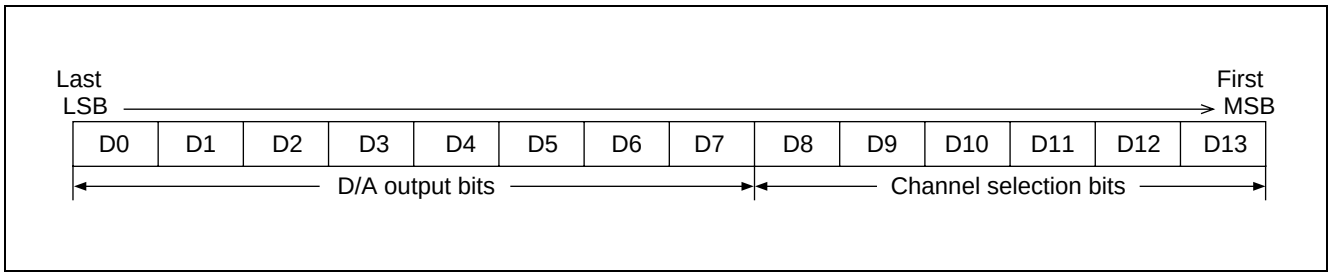


■ DATA CONFIGURATION

The MB88345 has a 14-bit shift register for chip control.

The 14-bit shift register must be used to set up data in the configuration shown below.

Note : The data configuration has a total of 14 bits, six for channel selection and eight for D/A data output.



• D/A converter control signals

Input data signal								D/A converter output voltage
D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	0	0	0	0	0	≒ V_{SS}
1	0	0	0	0	0	0	0	≒ V_{REF} / 255 × 1 + V_{SS}
≀	≀	≀	≀	≀	≀	≀	≀	≀
0	1	1	1	1	1	1	1	≒ V_{REF} / 255 × 254 + V_{SS}
1	1	1	1	1	1	1	1	≒ V_{DD}

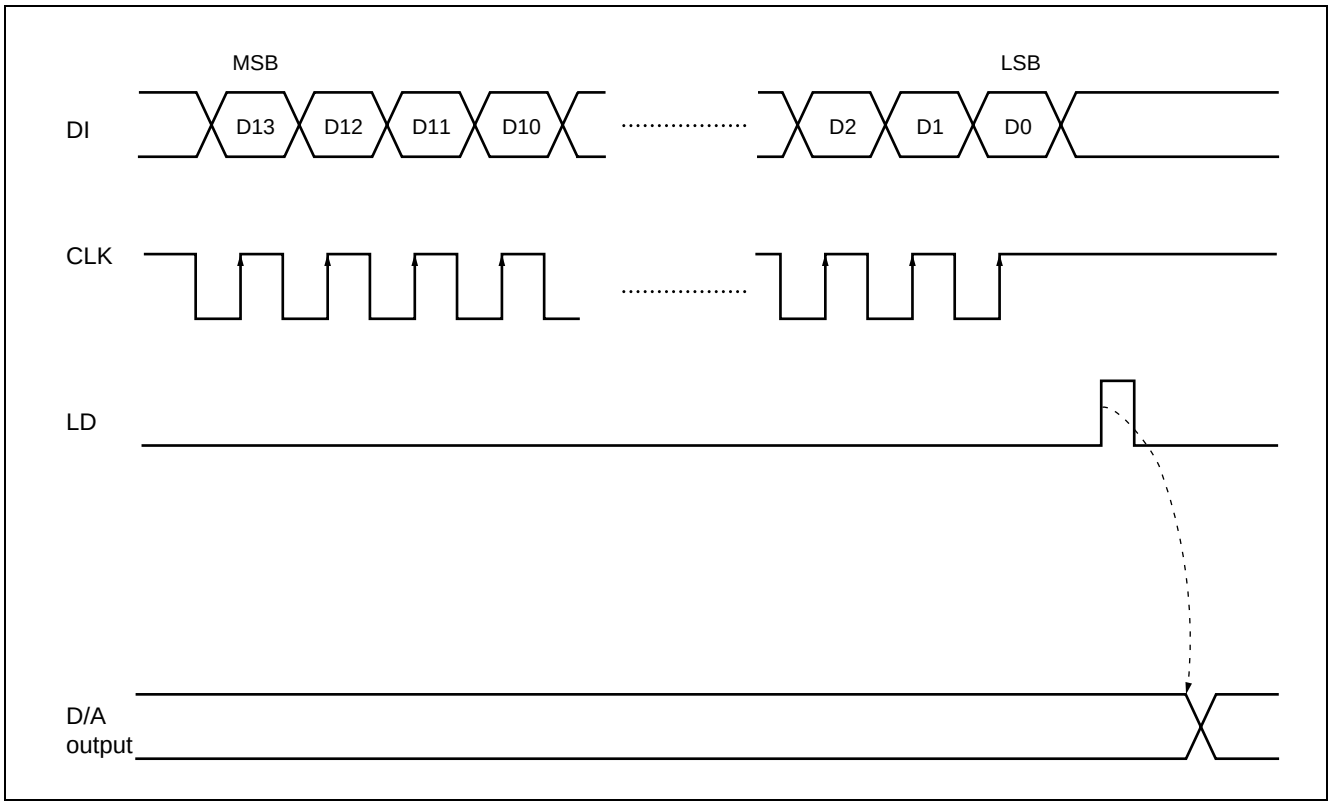
$V_{REF} = V_{DD} - V_{SS}$

• Channel selection signals

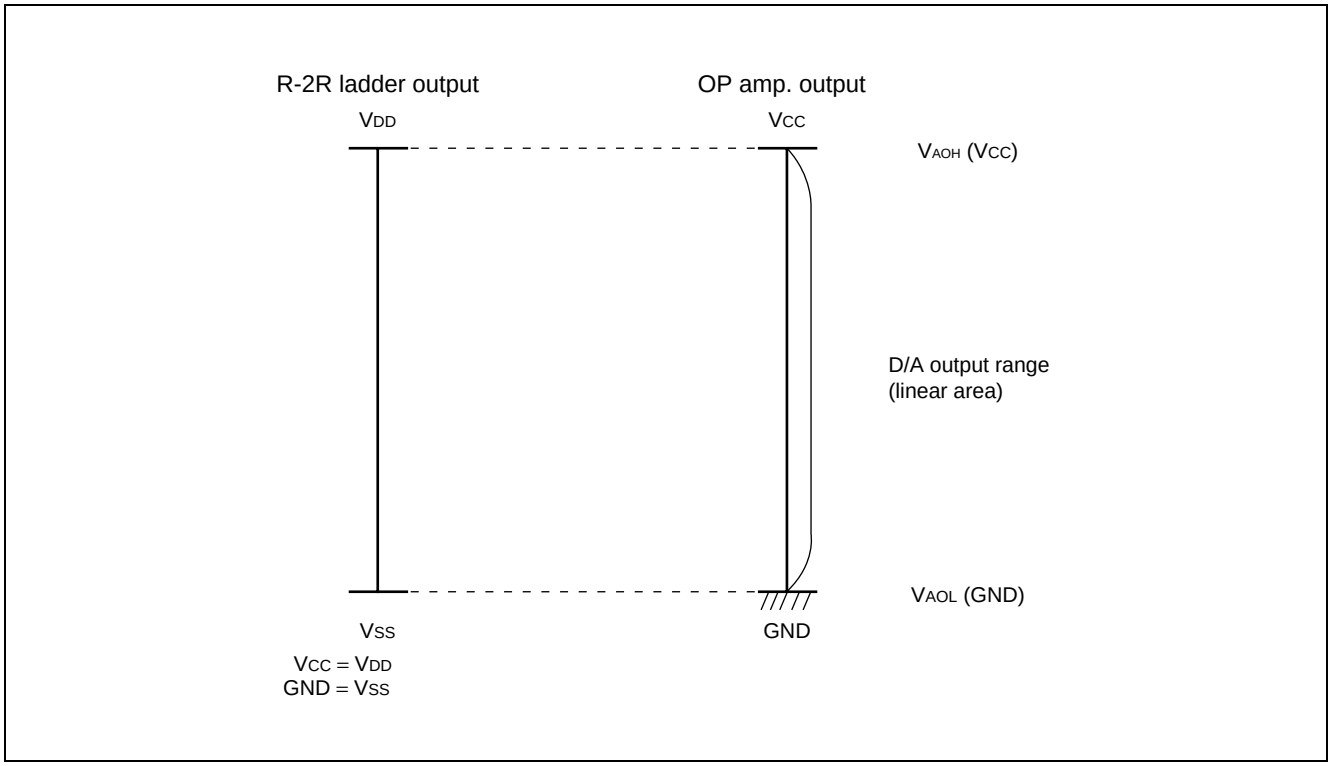
Input data signal						Channel selection
D8	D9	D10	D11	D12	D13	
×	0	0	0	0	0	Deselected
×	0	0	0	0	1	AO1 Selection
×	0	0	0	1	0	AO2 Selection
≀	≀	≀	≀	≀	≀	≀
×	1	0	1	1	1	AO23 Selection
×	1	1	0	0	0	AO24 Selection
×	1	1	0	0	1	Deselected
×	1	1	0	1	0	
≀	≀	≀	≀	≀	≀	
×	1	1	1	1	0	
×	1	1	1	1	1	

× : Don't Care

■ TIMING CHART



■ ANALOG OUTPUT VOLTAGE RANGE



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	Based on GND Ta = +25 °C	–0.3	+7.0	V
	V_{DD}		–0.3*	+7.0*	V
Input voltage	V_{IN}		–0.3	V_{CC} + 0.3	V
Output voltage	V_{OUT}		–0.3	V_{CC} + 0.3	V
Power consumption	P_D	—	—	250	mW
Operating temperature	Ta		–20	+85	°C
Storage temperature	Tstg		–55	+150	°C

* : $V_{CC} \geq V_{DD}$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage 1	V_{CC}	—	5 V ± 10 %	V
	GND		0	V
Power supply voltage 2	V_{DD}	$V_{DD} - V_{SS} \geq 2.0$ V	2.0 to V_{CC}	V
	V_{SS}		GND to V_{CC} – 2.0	V
Analog output source current	I_{AL}	—	max. 1.0	mA
Analog output sink current	I_{AH}		max. 1.0	mA
Oscillation limit output capacity	C_{OL}		max. 1.0	µF
Digital data value range	—		#00 to #FF	—
Operating temperature	Ta		–20 to +85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(1) Digital block

(V_{DD}, V_{CC} = +5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	V_{CC}	V_{CC}	—	4.5	5.0	5.5	V
Power supply current	I_{CC}		Operation at CLK = 1 MHz (No load)	—	2.4	5.4	mA
Input leak current	I_{ILK}	CLK DI LD	V_{IN} = 0 to V_{CC}	–10	—	10	µA
"L" level input voltage	V_{IL}		—	—	—	0.2 V_{CC}	V
"H" level input voltage	V_{IH}			0.5 V_{CC}	—	—	V
"L" level output voltage	V_{OL}	DO	I_{OL} = 2.5 mA	—	—	0.4	V
"H" level output voltage	V_{OH}		I_{OH} = –400 µA	V_{CC} – 0.4	—	—	V

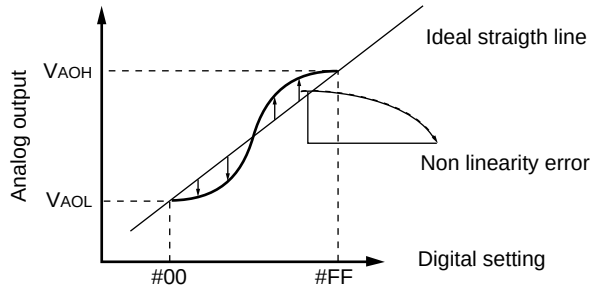
(2) Analog block (1)

(V_{DD}, V_{CC} = +5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power consumption	I_{DD}	V_{DD}	No load	—	3.0	4.5	mA
Analog Voltage	V_{DD}		$V_{DD} – V_{SS} \geq 2.0$ V	2.0	—	V_{CC}	V
	V_{SS}	V_{SS}		GND	—	V_{CC} – 2.0	V
Resolution	Res	AO1 to AO24	—	—	8	—	bit
Monotonic increase	Rem		No load $V_{DD} \leq V_{CC} – 0.1$V $V_{SS} \geq 0.1$ V	—	8	—	bit
Non-linearity error	LE			–1.5	—	1.5	LSB
Differential linearity error	D_{LE}			–1.0	—	1.0	LSB

Nonlinearity error : Deviation (error) in input/output curves with respect to an ideal straight line connecting output voltage at "00" and output voltage at "FF."

Differential linearity error : Deviation (error) in amplification with respect to theoretical increase in amplification per 1-bit increase in digital value.



Note : The value of V_{AOH} and V_{DD}, and the value of V_{AOL} and V_{SS} are not necessarily equivalent.

(3) Analog block (2)

(V_{DD}, V_{CC} = +5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = –20 °C to +85 °C)

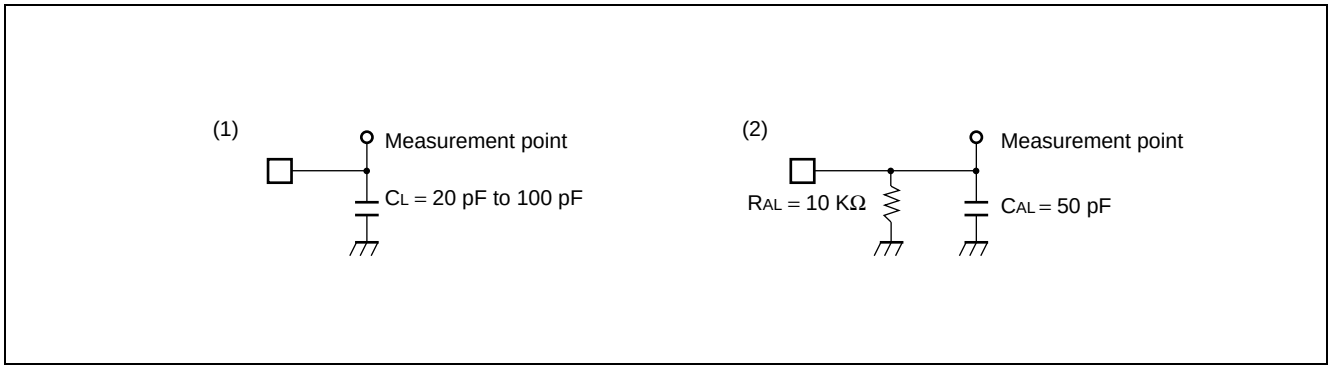
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Output minimum voltage 1	V_{AOL1}	AO1 to AO24	V_{DD} = V_{CC} V_{SS} = GND = 0 V I_{AL} = 0 µA Digital data = #00	V_{SS}	—	V_{SS} + 0.1	V
Output minimum voltage 2	V_{AOL2}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AL} = 500 µA Digital data = #00	V_{SS} – 0.2	V_{SS}	V_{SS} + 0.2	V
Output minimum voltage 3	V_{AOL3}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AH} = 500 µA Digital data = #00	V_{SS}	—	V_{SS} + 0.2	V
Output minimum voltage 4	V_{AOL4}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AL} = 1.0 mA Digital data = #00	V_{SS} – 0.3	V_{SS}	V_{SS} + 0.3	V
Output minimum voltage 5	V_{AOL5}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AH} = 1.0 mA Digital data = #00	V_{SS}	—	V_{SS} + 0.3	V
Output maximum voltage 1	V_{AOH1}		V_{DD} = V_{CC} V_{SS} = GND = 0 V I_{AL} = 0 µA Digital data = #FF	V_{DD} – 0.1	—	V_{DD}	V
Output maximum voltage 2	V_{AOH2}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AL} = 500 µA Digital data = #FF	V_{DD} – 0.2	—	V_{DD}	V
Output maximum voltage 3	V_{AOH3}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AH} = 500 µA Digital data = #FF	V_{DD} – 0.2	V_{DD}	V_{DD} + 0.2	V
Output maximum voltage 4	V_{AOH4}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AL} = 1.0 mA Digital data = #FF	V_{DD} – 0.3	—	V_{DD}	V
Output maximum voltage 5	V_{AOH5}		V_{DD} = V_{CC} = 5.0 V V_{SS} = GND = 0 V I_{AH} = 1.0 mA Digital data = #FF	V_{DD} – 0.3	V_{DD}	V_{DD} + 0.3	V

2. AC Characteristics

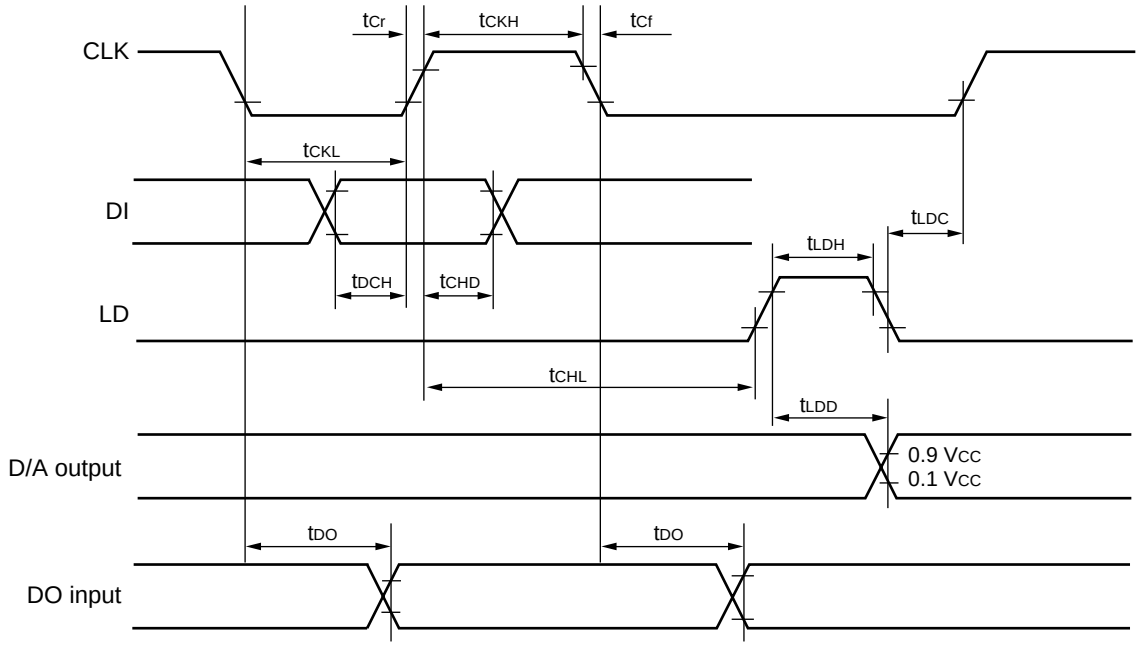
(V_{DD}, V_{CC} = +5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
“L” level clock pulse width	t_{CKL}	—	200	—	ns
“H” level clock pulse width	t_{CKH}		200	—	ns
Clock rise time Clock fall time	t_{Cr} t_{Cf}		—	200	ns
Data setup time	t_{DCH}		30	—	ns
Data hold time	t_{CHD}		60	—	ns
Load setup time	t_{CHL}		200	—	ns
Load hold time	t_{LDC}		100	—	ns
“H” level load pulse width	t_{LDH}		100	—	ns
Data output delay time	t_{DO}	See “Load conditions (1) ”	—	150	ns
D/A output setting time	t_{LDD}	See “Load conditions (2) ”	—	100	µs

- Load conditions

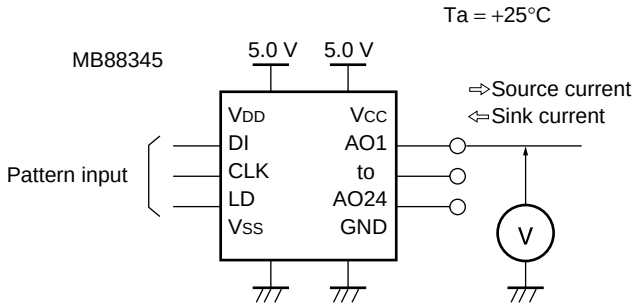


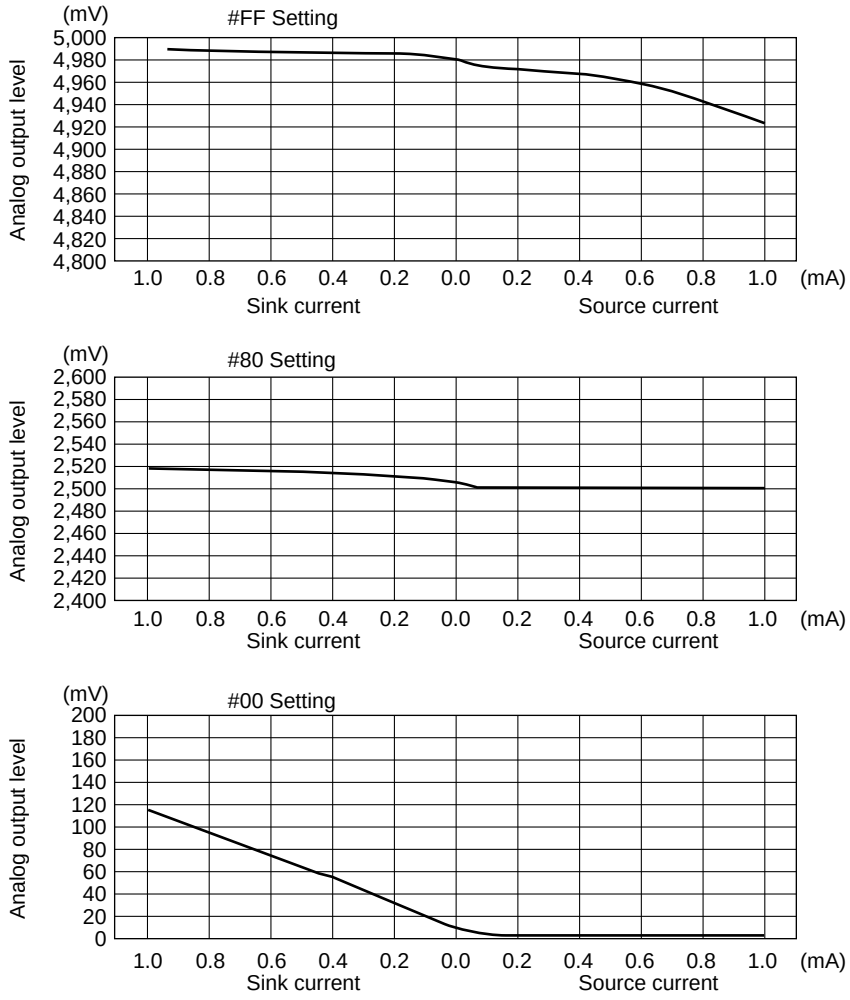
- Input/output timing



Note : Digital input decision level : 50% and 20% of V_{CC}.
Digital output decision level : 80% and 20% of V_{CC}.
Analog output decision level : 90% and 10% of V_{CC}.

■ V_{AO} vs. I_{AO} CHARACTERISTICS EXAMPLE



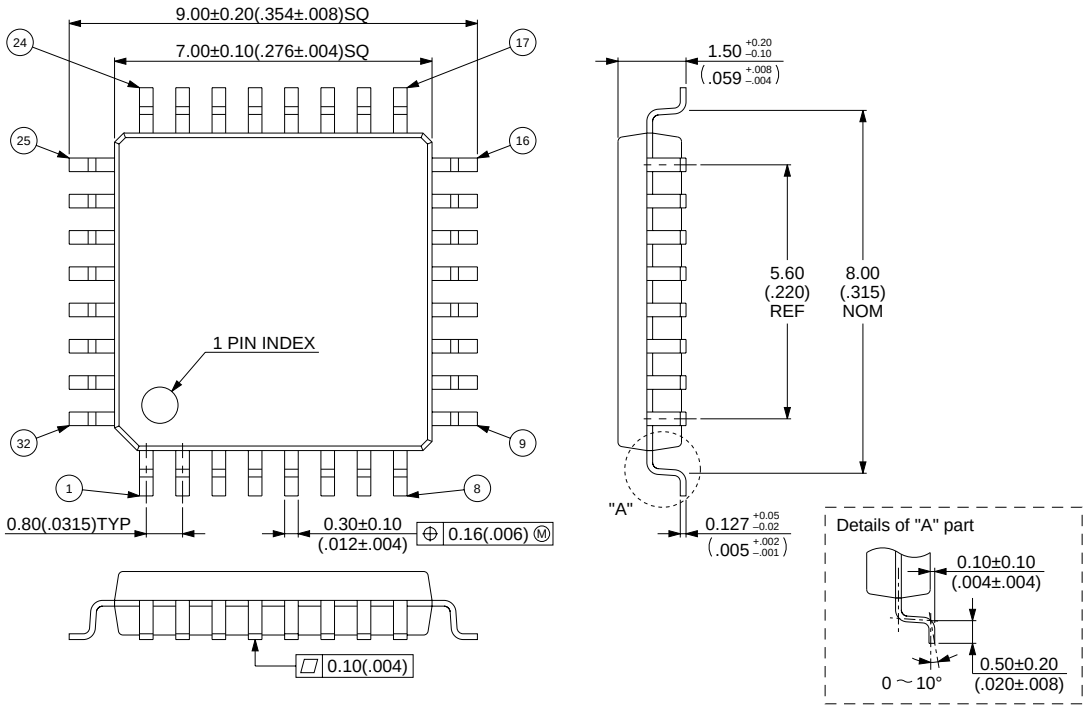


■ ORDERING INFORMATION

Part number	Package	Remarks
MB88345PF	32 pin Plastic QFP (FPT-32P-M21)	

■ PACKAGE DIMENSION

32-pin, Plastic QFP
(FPT-32P-M21)



Dimensions in mm (inches)

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0002