FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13608-1E

16-bit Proprietary Microcontroller

CMOS

F²MC-16L MB90640A Series

MB90641A/P641A

■ DESCRIPTION

MB90640A series includes 16-bit microcontrollers optimally suitable for process control in a wide variety of industrial and OA equipment. The series uses the F²MC*-16L CPU which is based on the F²MC-16 but with enhanced high-level language and task switching instructions and additional addressing modes.

The internal peripheral resources consist of a 2-channel serial port incorporating a UART function (and supporting I/O expansion serial mode), 8/16-bit 2-channel PPG, 5-channel 16-bit reload timer, 8-channel chip select function, and 8-channel DTP/external interrupts.

Also, multiplexed or non-multiplexed operation can be selected for the address/data bus.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

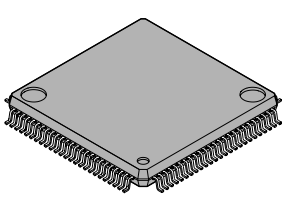
F²MC-16L CPU

- Minimum instruction execution time: 58.8 ns/4.25 MHz oscillation (Uses PLL clock multiplication), maximum multiplier = 4
- Instruction set optimized for controller applications
  Upward object code compatibility with F²MC-16 (H)
  Wide range of data types (bit/byte/word/long word)
  Improved instruction cycles provide increased speed
  Additional addressing modes: 23 modes

(Continued)

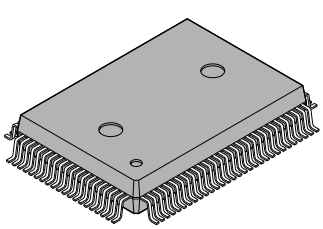
■ PACKAGE

100-pin Plastic LQFP



(FPT-100P-M05)

100-pin Plastic QFP



(FPT-100P-M06)

MB90640A Series

(Continued)

High code efficiency
Access methods (bank access/linear pointer)
Enhanced multiplication and division instructions (signed instructions added)
High precision operations are enhanced by use of a 32-bit accumulator
Extended intelligent I/O service (access area extended to 64 Kbytes)
Maximum memory space: 16 Mbytes

- Enhanced high level language (C)/multitasking support instructions
  Use of a system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
  Stack check function
- Improved execution speed: Four byte instruction queue
- Powerful interrupt function
- Automatic data transfer function (does not use instructions)

Internal peripherals

- RAM: 2 Kbytes
- General purpose ports Data bus, multiplexed mode: 56 ports max.
  Non-multiplexed mode: 48 ports max.
  Single-chip mode: 75 ports max.
- UART0, 1 (SCI): 2 channels
  For either asynchronous or clocked serial transfer (I/O expansion serial)
- 8/16-bit PPG (programmable pulse generator): 2 channels
- 16-bit reload timer: 5 channels
- Chip select function: 8 channels
- DTP/external interrupts: 8 channels
- Timebase timer/watchdog timer
- PLL clock multiplier function
- CPU intermittent operation function
- Various standby modes
- Packages: LQFP-100 and QFP-100
- CMOS technology

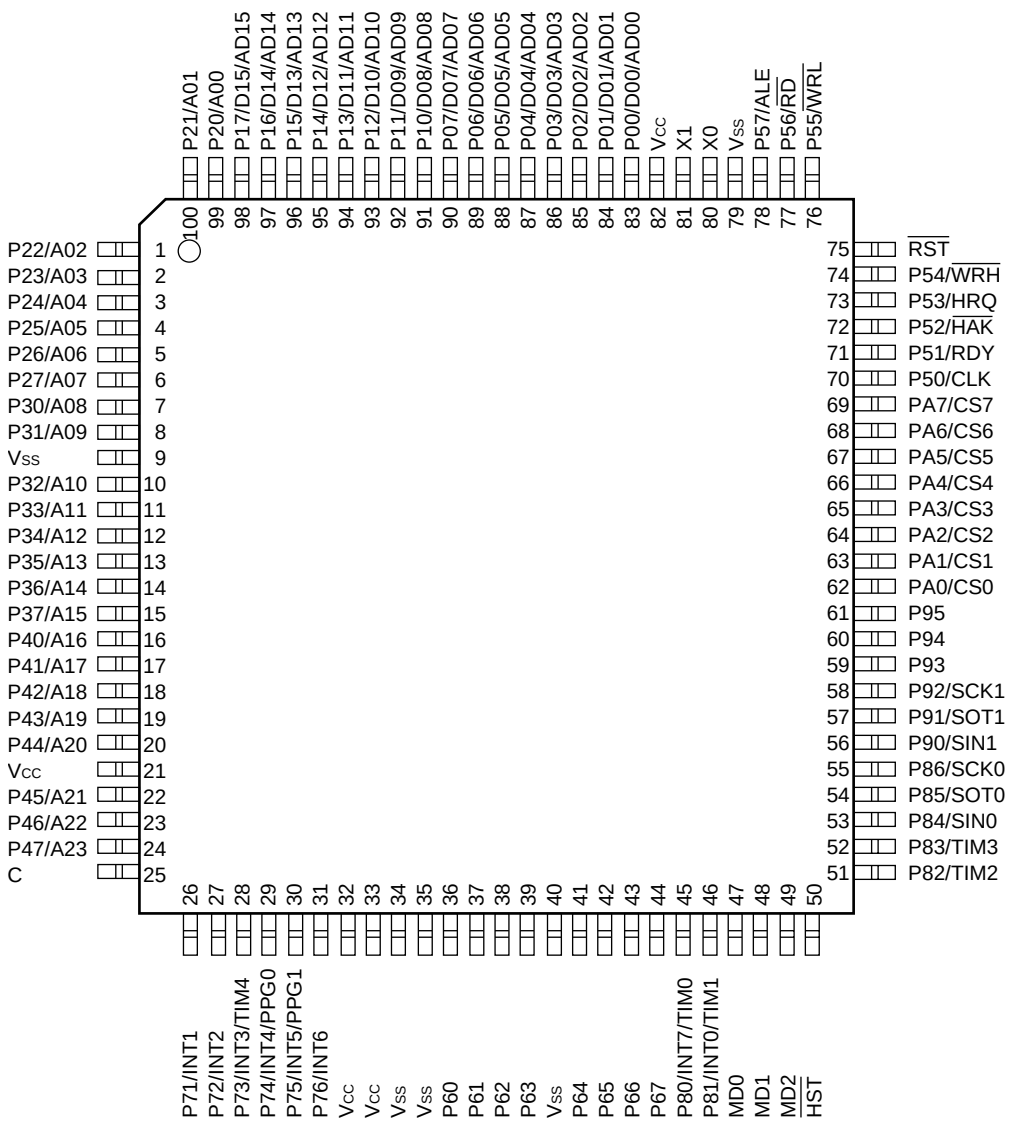
■ PRODUCT LINEUP

Item \ Part number	MB90641A	MB90P641A
Classification	Mask ROM	One-time PROM
ROM size	64 Kbytes	64 Kbytes
RAM size	2 Kbytes	2 Kbytes
CPU functions	The number of instructions: 340 Instruction bit length: 8/16 bits Instruction length: 1 to 7 bytes Data bit length: 1/4/8/16/32 bits Minimum execution time: 58.8 ns at 4.25 MHz (PLL multiplier = 4) Interrupt processing time: 941 ns at 17 MHz (minimum)	
Ports	8/16-bit data bus, multiplexed mode: 56 ports (max) 8-bit non-multiplexed mode: 48 ports (max) Single-chip mode: 75 ports (max)	
Packages	FPT-100P-M05 FPT-100P-M06	
UART0, 1 (SCI)	Two internal UARTs Full-duplex, double-buffered Selectable clock synchronous or asynchronous operation Built-in dedicated baud rate generator	
8/16-bit PPG	2 × 8-bit PPG outputs (1 channel PPG output in 16-bit mode)	
16-bit reload timer	16-bit reload timer operation (selectable toggle output, one-shot output) (Selectable count clock: 0.125 µs, 0.5 µs, or 2.0 µs for a 16 MHz machine cycle) Selectable event count function, 5 internal channels	
Chip select function	8 outputs	
DTP/external interrupts	8 inputs External interrupt mode (Interrupts can be generated from four different types of request signal)	
PLL function	Selectable multiplier: 1/2/3/4 (Set a multiplier that does not exceed the assured operation frequency range.)	
External bus terminal control circuit	Multiplex and non-multiplex between the adress pin and the data pin is selectable.	

MB90640A Series

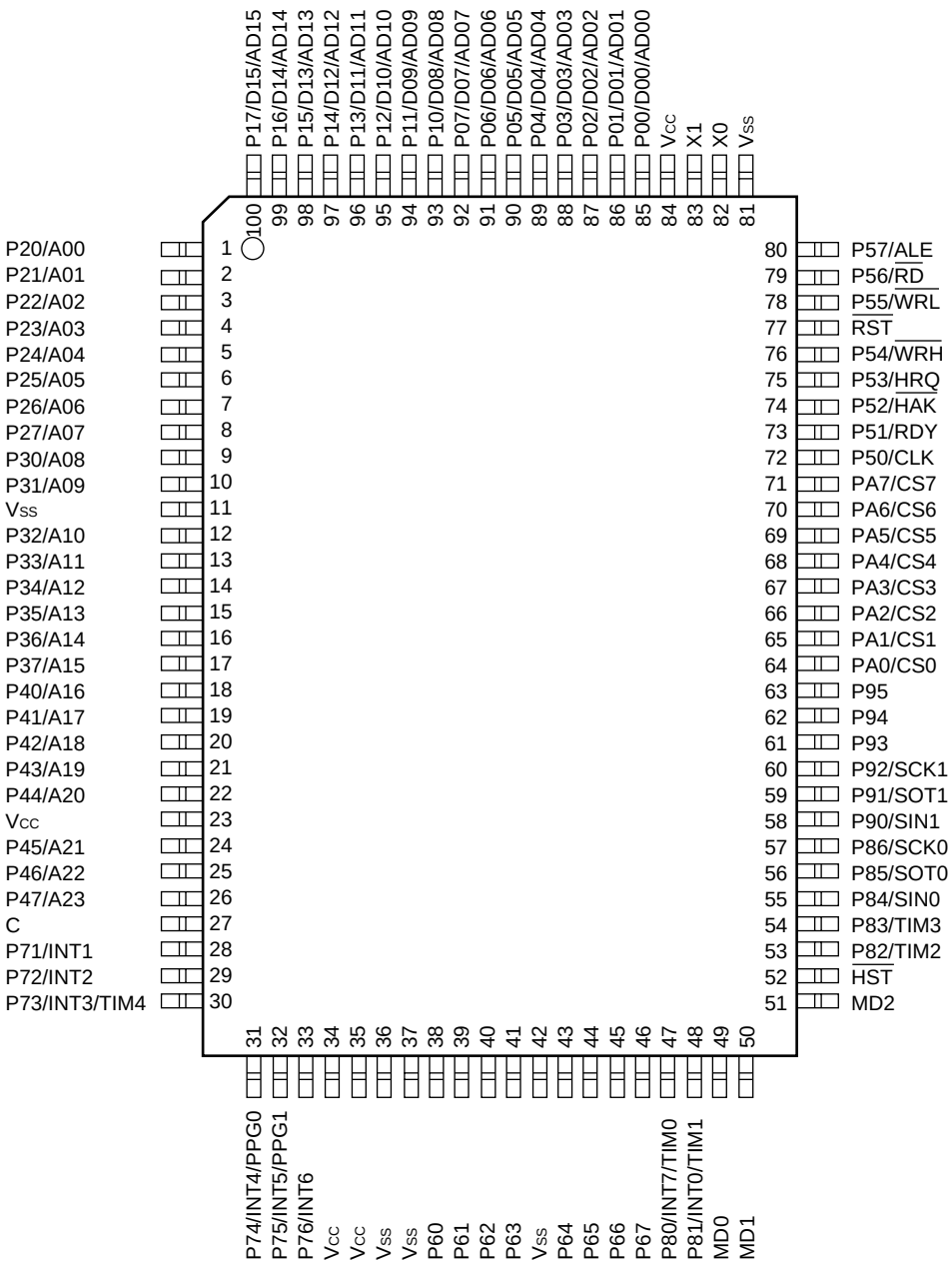
■ PIN ASSIGNMENT

(Top view)



(FPT-100P-M05)

(Top view)



(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
80, 81	82, 83	X0, X1	A	Crystal oscillator pins
47 to 49	49 to 51	MD0 to MD2	E (CMOS)	Input pins for specifying an opration mode. Use these pins by directly connecting V_{CC} or V_{SS}.
75	77	$\overline{RST}$	G (CMOS/H)	External reset request input pin
50	52	$\overline{HST}$	F (CMOS/H)	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	J (TTL)	General purpose I/O ports This applies in single-chip mode with an external data bus in 8-bit mode.
		D00 to D07		In non-multiplex mode, the I/O pins for the lower 8 bits of the external data bus.
		AD00 to AD07		In multiplexed mode, the I/O pins for the lower 8 bits of the external address/data bus.
91 to 98	93 to 100	P10 to P17	J (TTL)	General purpose I/O ports This applies in non-multiplexed mode with an 8-bit external data bus and in single-chip mode.
		P08 to D15		In non-multiplexed mode with a 16-bit external data bus, the I/O pins for the upper 8 bits of the external data bus.
		AD08 to AD15		In multiplexed mode, the I/O pins for the upper 8 bits of the external address/data bus.
99, 100, 1 to 6	1, 2, 3 to 8	P20, P21, P22 to P27	B (CMOS)	General purpose I/O ports This applies in multiplexed mode.
		A00, A01, A02 to A07		In non-multiplexed mode, the output pins for the lower 8 bits of the external address bus.
7, 8, 10 to 15	9, 10, 12 to 17	P30, P31, P32 to P37	B (CMOS)	General purpose I/O ports This applies in multiplexed mode.
		A08, A09, A10 to A15		In non-multiplexed mode, the output pins for the upper 8 bits of the external address bus.
16 to 20, 22 to 24	18 to 22, 24 to 26	P40 to P44, P45 to P47	B (CMOS)	General purpose I/O ports This applies when the upper address control register specifies port operation.
		A16 to A20, A21 to A23		Output pins for A16 to A23 of the external address bus This applies when the upper address control register specifies address operation.

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
70	72	P50	I (CMOS)	General purpose I/O port This applies when CLK output is disabled.
		CLK		CLK output pin This applies when CLK output is enabled.
71	73	P51	K (TTL)	General purpose I/O port This applies when the external ready function is disabled.
		RDY		Ready input pin This applies when the external ready function is enabled.
72	74	P52	I (CMOS)	General purpose I/O port This applies when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin This applies when the hold function is enabled.
73	75	P53	K (TTL)	General purpose I/O port This applies when the hold function is disabled.
		HRQ		Hold request input pin This applies when the hold function is enabled.
74	76	P54	I (CMOS)	General purpose I/O port This applies in 8-bit external bus mode or when output is disabled for the $\overline{\text{WRH}}$ pin.
		$\overline{\text{WRH}}$		Write strobe output pin for the upper 8 bits of the data bus This applies in 16-bit external bus mode and when output is enabled for the $\overline{\text{WRH}}$ pin.
76	78	P55	I (CMOS)	General purpose I/O port This applies when output is disabled for the $\overline{\text{WRL}}$ pin.
		$\overline{\text{WRL}}$		Write strobe output pin for the lower 8 bits of the data bus This applies when output is enabled for the $\overline{\text{WRL}}$ pin.
77	79	P56	I (CMOS)	General-purpose I/O port This port is available in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus
78	80	P57	I (CMOS)	General-purpose I/O port This port is available in the single-chip mode.
		ALE		Address latch enable output pin
36 to 39, 41 to 44	38 to 41, 43 to 46	P60 to P67	C	Open-drain output ports

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
26, 27	28, 29	P71, P72	H (CMOS/H)	General purpose I/O ports This applies in all cases.
		INT1, INT2		External interrupt request input pins As the inputs operate continuously when external interrupts are enabled, output to the pins from other functions must be stopped unless done intentionally.
28	30	P73	H (CMOS/H)	General purpose I/O ports This applies when output is disabled for reload timers.
		INT3		External interrupt request input pins As the inputs operate continuously when external interrupts are enabled, output to the pins from other functions must be stopped unless done intentionally.
		TIM4		I/O pins for reload timers Input is used only as necessary while serving as input for the reload timer. It is therefore necessary to stop output beforehand using other functions unless intentionally used otherwise. Their function as output terminals for the reload timer is activated when the output specification is enabled.
29, 30	31, 32	P74, P75	H (CMOS/H)	General purpose I/O ports This applies when the waveform outputs for PPG timers 0, 1 are disabled.
		INT4, INT5		External interrupt request input pin As the input operates continuously when the external interrupt is enabled, output to the pin from other functions must be stopped unless done intentionally.
		PPG0, PPG1		Output pins for PPG timers This applies when the waveform outputs for PPG timers 0, 1 are enabled.
31	33	P76	H (CMOS/H)	General purpose I/O port This applies in all cases.
		INT6		External interrupt request input pin As the input operates continuously when the external interrupt is enabled, output to the pin from other functions must be stopped unless done intentionally.

(Continued)

*1: FPT-100P-M05
*2: FPT-100P-M06

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
45, 46	47, 48	P80, P81	H (CMOS/H)	General purpose I/O ports This applies when output is disabled for reload timers.
		INT7, INT0		External interrupt request input pin As the input operates continuously when the external interrupt is enabled, output to the pin from other functions must be stopped unless done intentionally.
		TIM0, TIM1		I/O pins for reload timers Input is used only as necessary while serving as input for the reload timer. It is therefore necessary to stop output beforehand using other functions unless intentionally used otherwise. Their function as output terminals for the reload timer is activated when the output specification is enabled.
51, 52	53, 54	P82, P83	D (CMOS/H)	General purpose I/O ports This applies when output is disabled for reload timers.
		TIM2, TIM3		I/O pins for reload timers Input is used only as necessary while serving as input for the reload timer. It is therefore necessary to stop output beforehand using other functions unless intentionally used otherwise. Their function as output terminals for the reload timer is activated when the output specification is enabled.
53	55	P84	D (CMOS/H)	General purpose I/O port This applies in all cases.
		SIN0		Serial data input pin for UART0 As the input operates continuously when UART0 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
54	56	P85	D (CMOS/H)	General purpose I/O port This applies when serial data output is disabled for UART0.
		SOT0		Serial data output pin for UART0 This applies when serial data output is enabled for UART0.
55	57	P86	D (CMOS/H)	General purpose I/O port This applies when the UART0 clock output is disabled.
		SCK0		Clock I/O pin for UART0 This applies when the UART0 clock output is enabled. As the input operates continuously when UART0 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
56	58	P90	D (CMOS/H)	General purpose I/O port This applies in all cases.
		SIN1		Serial data input pin for UART1 As the input operates continuously when UART1 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.

*1: FPT-100P-M05
*2: FPT-100P-M06

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MB90640A Series

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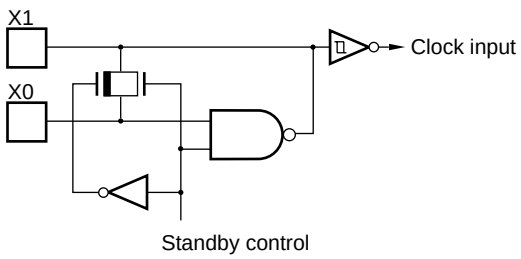
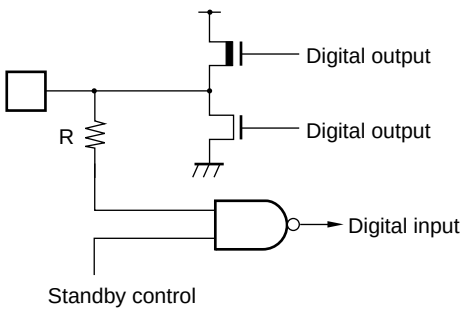
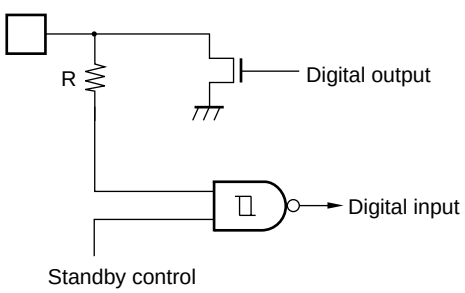
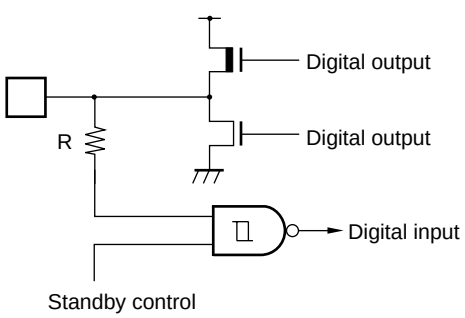
Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
57	59	P91	D (CMOS/H)	General purpose I/O port This applies when serial data output is disabled for UART1.
		SOT1		Serial data output pin for UART1 This applies when serial data output is enabled for UART1.
58	60	P92	D (CMOS/H)	General purpose I/O port This applies when the UART1 clock output is disabled.
		SCK1		Clock I/O pin for UART1 This applies when the UART1 clock output is enabled. As the input operates continuously when UART1 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
59 to 61	61 to 63	P93 to P95	D (CMOS/H)	General purpose I/O port
25	27	C	—	Capacitor pin for stabilizing power supply Connect about 0.1 µF ceramic capacitor outside ROM. MB90P641 doesn't need to be connected the capacitor. It isn't problem even the capacitor is connected to MB90P641A.
62 to 69	64 to 71	PA0 to PA7	I (CMOS/H)	General purpose I/O ports This applies for pins with chip select output disabled by the chip select control register.
		CS0 to CS7		Output pins for the chip select function This applies for pins with chip select output enabled by the chip select control register.
21, 32, 33, 82	23, 34, 35, 84	V_{CC}	Power supply	Power supply for the digital circuits
9, 34, 35, 40, 79	11, 36, 37, 42, 81	V_{SS}	Power supply	Ground level for the digital circuits

*1: FPT-100P-M05
*2: FPT-100P-M06

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Max. 3 to 34 MHz • Oscillation feedback resistance: approximately 1 MΩ
B		• CMOS level I/O With standby control • Pull-up resistor option
C		• N-channel open-drain output • CMOS level hysteresis input • Pull-up resistor option
D		• CMOS level output • CMOS level hysteresis input With standby control • Pull-up resistor option

Note: For pins with pull-up resistors, the resistance is disconnected when the pin outputs the “L” level or when in the standby state.

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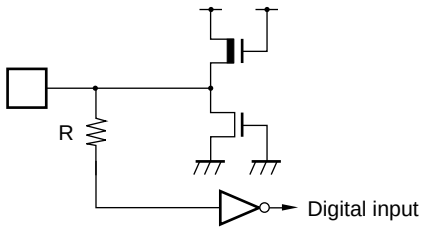
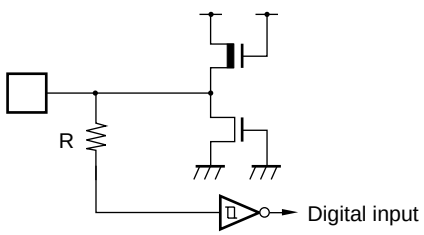
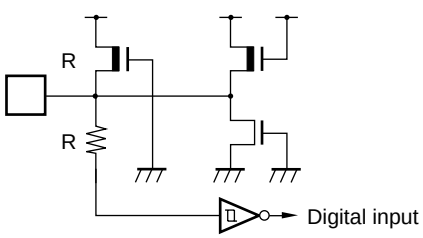
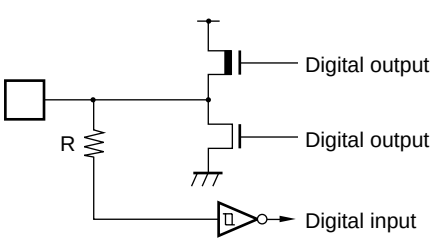
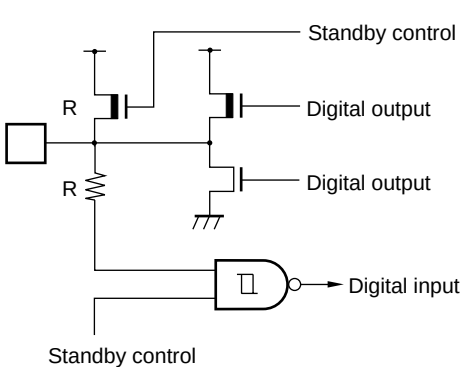
MB90640A Series

Type	Circuit	Remarks
E		• CMOS level input No standby control • Pull-up resistor option
F		• CMOS level hysteresis input No standby control • Pull-up resistor option
G		• CMOS level hysteresis input No standby control • With pull-up resistor
H		• CMOS level output • CMOS level hysteresis input No standby control • Pull-up resistor option
I		• CMOS level output • CMOS level hysteresis input • Pull-up resistor approximately 50 kΩ • Pin goes to high impedance during stop mode.

Note: For pins with pull-up resistors, the resistance is disconnected when the pin outputs the “L” level or when in the standby state.

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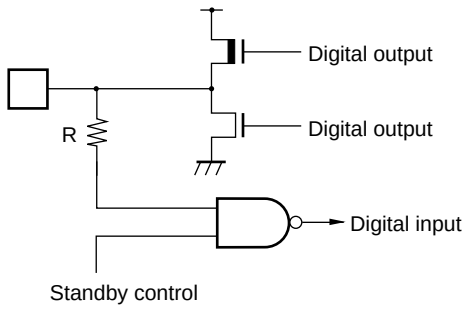
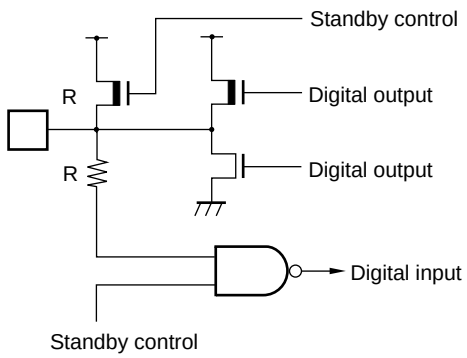
Type	Circuit	Remarks
J		• CMOS level output • TTL level input With standby control • Pull-up resistor option
K		• CMOS level output • TTL level input • Pull-up resistor approximately 50 kΩ • Pin goes to high impedance during stop mode.

Note: For pins with pull-up resistors, the resistance is disconnected when the pin outputs the “L” level or when in the standby state.

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or less than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidlly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the anaolg power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is truned on and off.

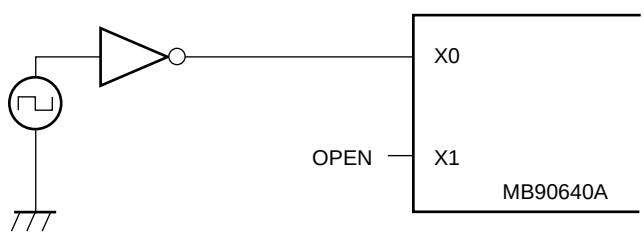
2. Treatment of Unused Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resister.

3. Cautions when Using an External Clock

Drive the X0 pin only when using an external clock.

- **Using an external clock**



4. Power Supply Pins

When there are several V_{CC} and V_{SS} pins, those pins that should have the same electric potential are connected within the device when the device is designed in order to prevent misoperation, such as latchup. However, all of those pins must be connected to the power supply and ground externally in order to reduce unnecessary emissions, prevent misoperation of strobe signals due to an increase in the ground level, and to observe the total output current standards.

In addition, give a due consideration to the connection in that current supply be connected to V_{CC} and V_{SS} with the lowest possible impedance.

Finally, it is recommended to connect a ceramic capacitor of about 0.1 µF between V_{CC} and V_{SS} near this device as a bypass capacitor.

5. Crystal Oscillation Circuit

Noise in the vicinity of the X0 and X1 pins will cause this device to operate incorrectly. Design the printed circuit board so that the bypass capacitor connecting X0, X1 and the crystal oscillator (or ceramic oscillator) to ground is located as close to the device as possible, and possibly take care not to cross over the other wiring with this wiring.

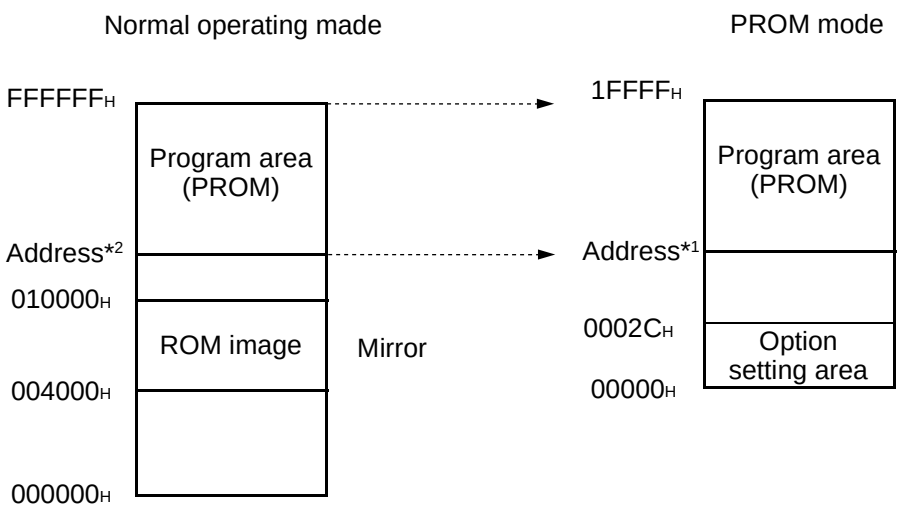
In addition, because printed circuit board artwork in which the area around the X0 and X1 pins is surrounded by ground provides stable operation, such an arrangement is strongly recommended.

■ PROGRAMMING TO THE ONE-TIME PROM ON THE MB90P641A

MB90P641A has a function PROM mode function equivalent to MBM27C1000/1000A, so it can be written by general ROM writer using special adapter. But take attention it doesn't corsespond to the elctronic signature (the device identification code) mode.

1. Programming Procedure

Memory map in the PROM mode is as below. Write option data to the option setting erea refering to the 6 PROM option bit map.



Product	Address*1	Address*2	Number of bytes
MB90P641A	10000H	FF0000H	64 Kbytes

Note: The 00 bank ROM image is 48 Kbyes. (This is a ROM image for FF4000H to FFFFFFH. Only when the ROM mirror function selecting resister is enable.)

Porocedure of the programing to the one-time PROM microcomputer is as below.

(1) Set the EPROM programmer for the MBM27C1000/1000A.
(2) Load the program data into the EPROM programmer at address*1 to 1FFFFH. When specify the PROM option, load the option data to 00000H to 00002CH to refering to "6. PROM Option Bitmap".
(3) Insert the device in the socket adapter, and mount the socket adapter on the EPROM programmer. Pay attention to the orientation of the device and of the socket adapter when doing so.
(4) Program to 00000H to 1FFFFH.

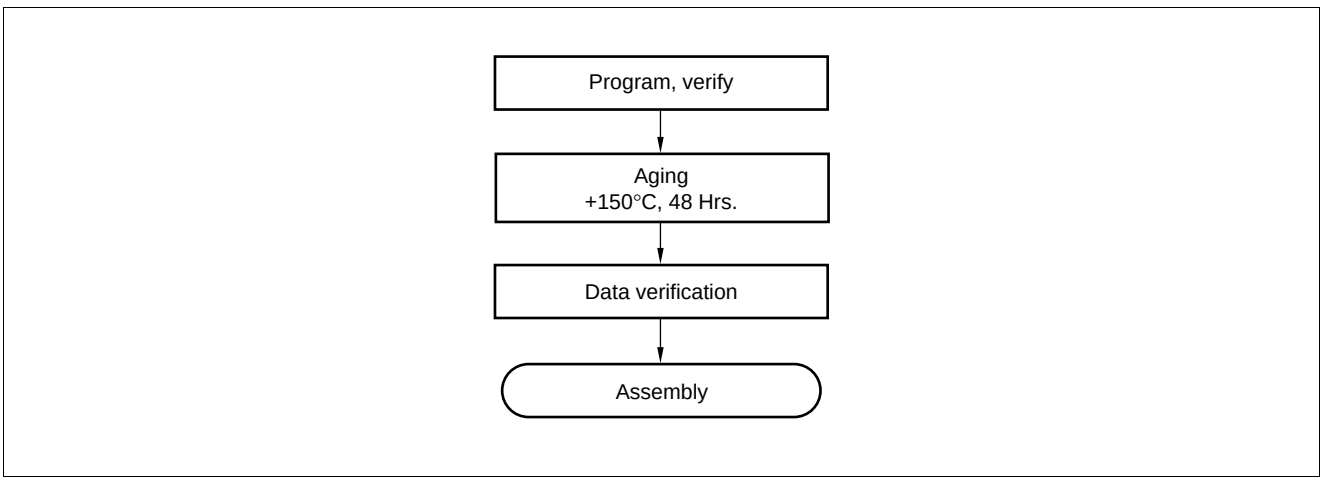
Notes: • Because the mask ROM products do not have a PROM mode, they cannot read date from the EPROM programmer.
• Contact the sales department when purchasing an EPROM programmer.

2. Program Mode

In the MB90P641A, all of the bits are set to "1" when the IC is shipped from Fujitsu and after erasure. To input data, program the IC by selectively setting the desired bits to "0". Bits cannot be set to "1" electrically.

3. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked one-time PROM with microcontroller program.



4. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked one-time PROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

5. EPROM Programmer Socket Adapter and Recommended Programmer Manuffacturer

Part no.			MB90P641APF	MB90P641APFV
Package			QFP-100	LQFP-100
Compatible socket adapter Sun Hayato Co., Ltd.			ROM-100QF-32DP -FFMC-16L	ROM-100SQF-32DP -FFMC-16L
Recommended programmer manufacturer and programmer name	**Minato Electronics Inc.**	**1890A**	Recommended	Recommended
		1891	Recommended	Recommended
		1930	Recommended	Recommended

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106
Minato Electronics Inc.: TEL: USA (1)-916-348-6066
JAPAN (81)-45-591-5611

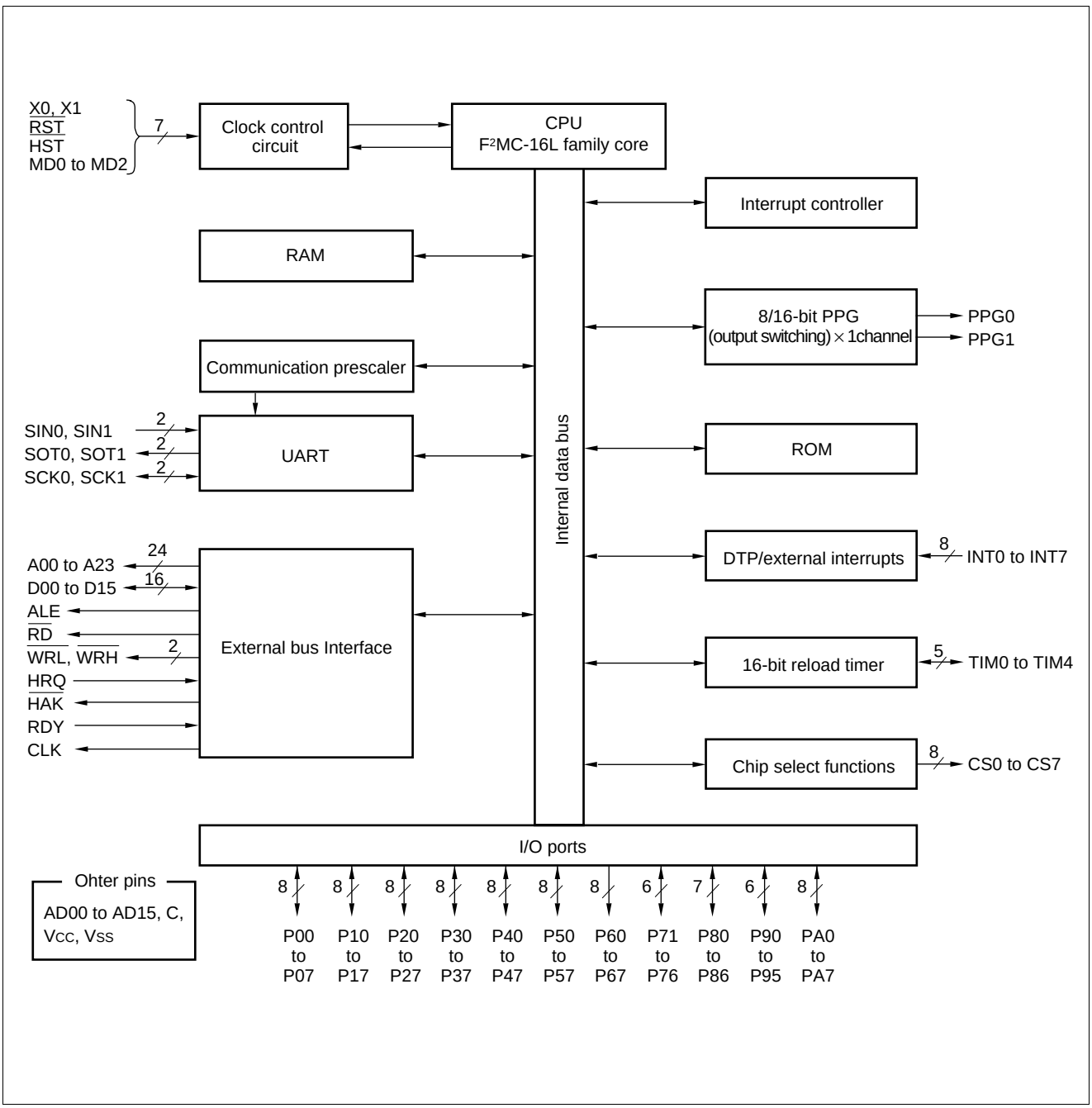
6. PROM Option Bitmap

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00000H	Vacancy	$\overline{\text{RST}}$ Pull-up 1: No 0: Yes	Vacancy	MD 1 Pull-up 1: No 0: Yes	MD 1 Pull-down 1: No 0: Yes	MD 0 Pull-up 1: No 0: Yes	MD 0 Pull-down 1: No 0: Yes	Vacancy
00004H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
00008H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0000CH	P27 Pull-up 1: No 0: Yes	P26 Pull-up 1: No 0: Yes	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P23 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
00010H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
00014H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0001CH	P57 Pull-up 1: No 0: Yes	P56 Pull-up 1: No 0: Yes	P55 Pull-up 1: No 0: Yes	P54 Pull-up 1: No 0: Yes	P53 Pull-up 1: No 0: Yes	P52 Pull-up 1: No 0: Yes	P51 Pull-up 1: No 0: Yes	P50 Pull-up 1: No 0: Yes
00020H	Vacancy	P76 Pull-up 1: No 0: Yes	P75 Pull-up 1: No 0: Yes	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	Vacancy
00024H	Vacancy	P86 Pull-up 1: No 0: Yes	P85 Pull-up 1: No 0: Yes	P84 Pull-up 1: No 0: Yes	P83 Pull-up 1: No 0: Yes	P82 Pull-up 1: No 0: Yes	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes
00028H	Vacancy	Vacancy	P95 Pull-up 1: No 0: Yes	P94 Pull-up 1: No 0: Yes	P93 Pull-up 1: No 0: Yes	P92 Pull-up 1: No 0: Yes	P91 Pull-up 1: No 0: Yes	P90 Pull-up 1: No 0: Yes
0002CH	PA7 Pull-up 1: No 0: Yes	PA6 Pull-up 1: No 0: Yes	PA5 Pull-up 1: No 0: Yes	PA4 Pull-up 1: No 0: Yes	PA3 Pull-up 1: No 0: Yes	PA2 Pull-up 1: No 0: Yes	PA1 Pull-up 1: No 0: Yes	PA0 Pull-up 1: No 0: Yes

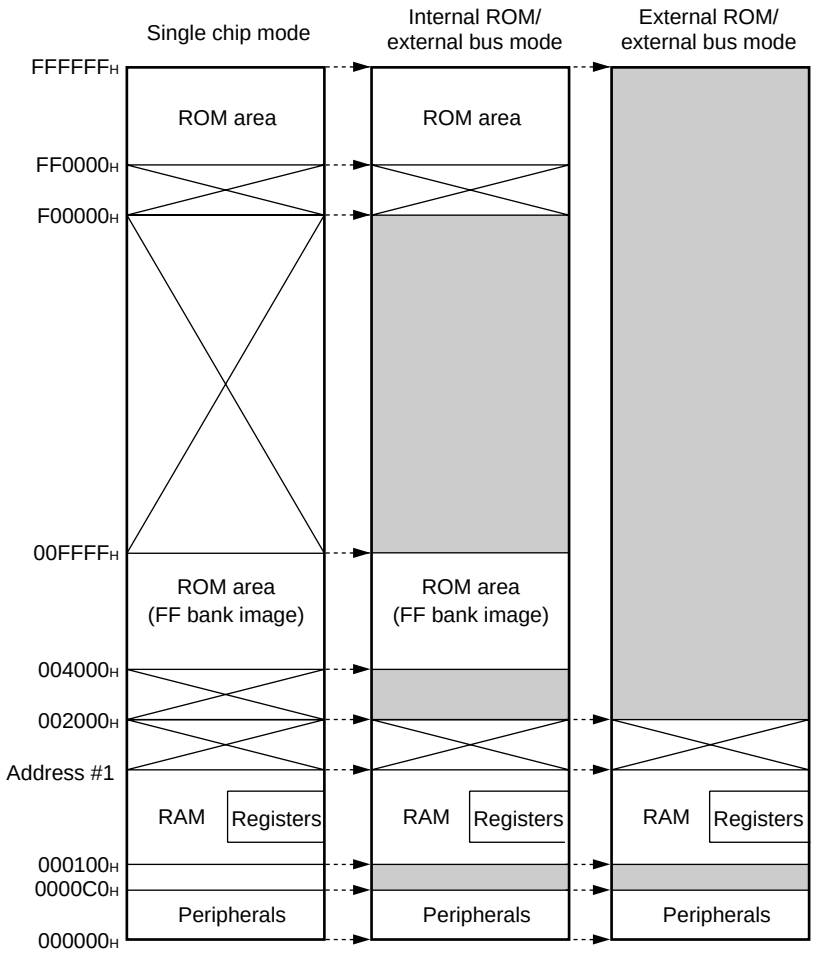
Note: Write data “1” to the vacant bit and the adress other than above.

MB90640A Series

■ BLOCK DIAGRAM



■ MEMORY MAP



Type	Address #1
MB90641A	000900H
MB90P641A	000900H

: Internal access memory

: External access memory

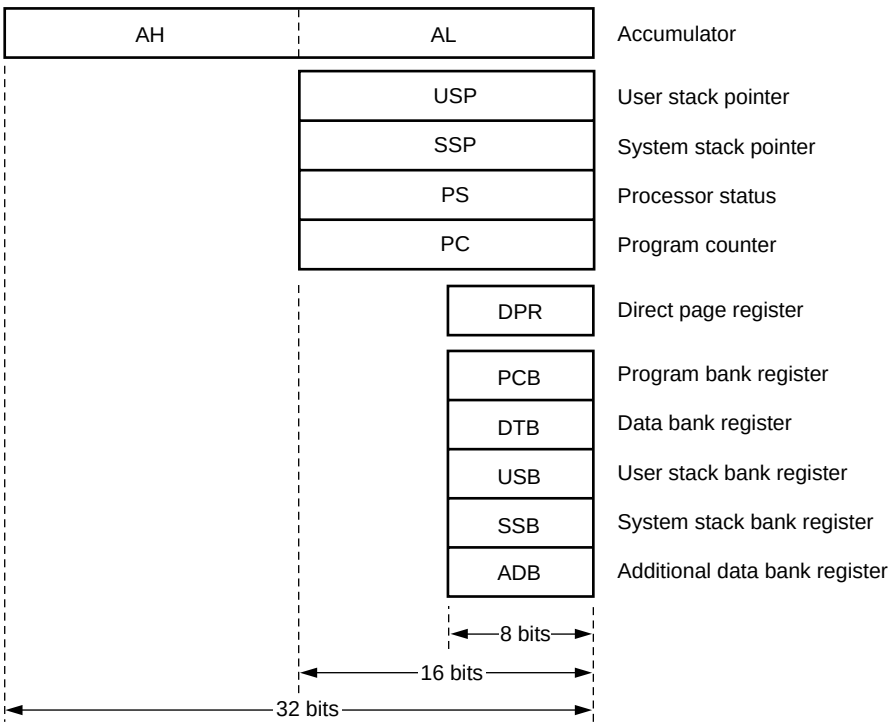
: No access

Note: When disable output upper address A23 to A16 of MB90640A series, the maximum acceptable size becomes 64 Kbytes.

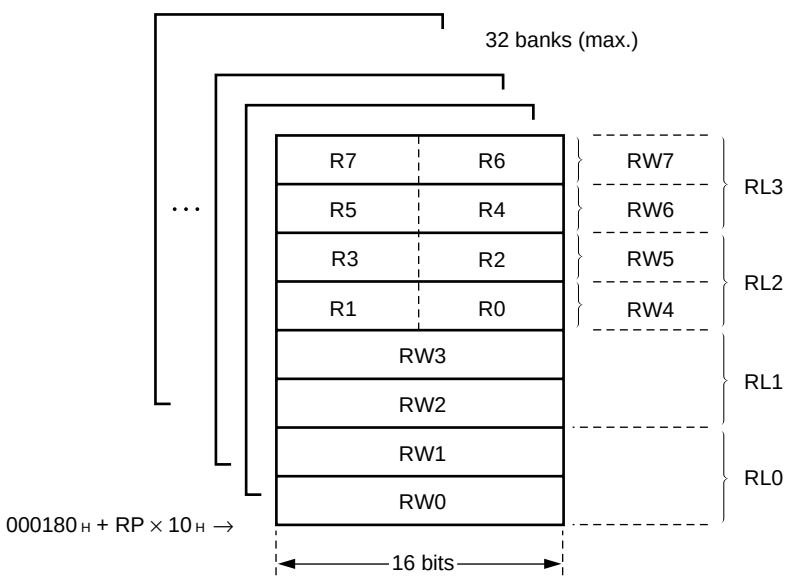
MB90640A Series

■ F²MC-16L CPU PROGRAMMING MODEL

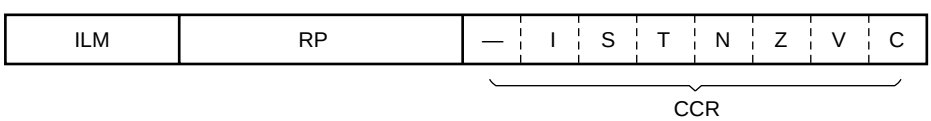
- **Dedicated registers**



- **General-purpose registers**



- **Processor status (PS)**



■ I/O MAP

Address	Name	Register	Read/ write*4,*5	Resource name	Initial value
000000H	PDR0	Port 0 data register	R/W*	Port 0*8	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W*	Port 1*7	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W*	Port 2*6	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W*	Port 3*6	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5*8	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	Port 6	11111111B
000007H	PDR7	Port 7 data register	R/W	Port 7	–XXXXXXXB
000008H	PDR8	Port 8 data register	R/W	Port 8	–XXXXXXXB
000009H	PDR9	Port 9 data register	R/W	Port 9	––XXXXXXB
00000AH	PDRA	Port A data register	R/W	Port A*8	XXXXXXX–B
00000BH to 0FH	—	Vacancy	*3	—	—
000010H	DDR0	Port 0 direction register	R/W*	Port 0*8	00000000B
000011H	DDR1	Port 1 direction register	R/W*	Port 1*7	00000000B
000012H	DDR2	Port 2 direction register	R/W*	Port 2*6	00000000B
000013H	DDR3	Port 3 direction register	R/W*	Port 3*6	00000000B
000014H	DDR4	Port 4 direction register	R/W	Port 4	00000000B
000015H	DDR5	Port 5 direction register	R/W	Port 5*8	00000000B
000016H	DDR6	Port 6 direction register	R/W	Port 6	11111111B
000017H	DDR7	Port 7 direction register	R/W	Port 7	–000000–B
000018H	DDR8	Port 8 direction register	R/W	Port 8	–0000000B
000019H	DDR9	Port 9 direction register	R/W	Port 9	––000000B
00001AH	DDRA	Port A direction register	R/W	Port A*8	00000000B
00001BH to 1FH	—	Vacancy	*3	—	—
000020H	SMR0	Serial mode register 0	R/W!	UART0 (SCI)	00000000B
000021H	SCR0	Serial control register 0	R/W!		00000100B
000022H	SIDR0/ SODR0	Input data register 0/ output data register 0	R/W		XXXXXXXXB
000023H	SSR0	Serial status register 0	R/W!		00001–00B
000024H	SMR1	Serial mode register 1	R/W!	UART1 (SCI)	00000000B
000025H	SCR1	Serial control register 1	R/W!		00000100B
000026H	SIDR1/ SODR1	Input data register 1/ output data register 1	R/W		XXXXXXXXB
000027H	SSR1	Serial status register 1	R/W!		00001–00B

(Continued)

Address	Name	Register	Read/ write*4,*5	Resource name	Initial value
000028H	ENIR	Interrupt/DTP enable register	R/W	DTP/external interrupt	0 0 0 0 0 0 0 0 B
000029H	EIRR	Interrupt/DTP request register	R/W		X X X X X X X X B
00002AH	ELVR	Interrupt level setting register	R/W		0 0 0 0 0 0 0 0 B
00002BH					0 0 0 0 0 0 0 0 B
00002CH to 2FH	—	Vacancy	*3	—	—
000030H	PPGC0	PPG0 operation mode control register	R/W	8/16-bit PPG0	0 – 0 0 0 0 0 1 B
000031H	PPGC1	PPG1 operation mode control register	R/W	8/16-bit PPG1	0 0 0 0 0 0 0 1 B
000032H, 33H	—	Vacancy	*3	—	—
000034H	PRLL0/ PRLH0	PPG0 reload register	R/W	8/16-bit PPG0	X X X X X X X X B
000035H					X X X X X X X X B
000036H	PRLL1/ PRLH1	PPG1 reload register	R/W	8/16-bit PPG1	X X X X X X X X B
000037H					X X X X X X X X B
000038H	TMCSR0	Timer control status register	R/W!	16-bit reload timer 0	0 0 0 0 0 0 0 0 B
000039H					– – – – 0 0 0 0 B
00003AH	TMR0/ TMRLR0	16-bit timer register/ 16-bit reload register	R/W		X X X X X X X X B
00003BH					X X X X X X X X B
00003CH	TMCSR1	Timer control status register	R/W!	16-bit reload timer 1	0 0 0 0 0 0 0 0 B
00003DH					– – – – 0 0 0 0 B
00003EH	TMR1/ TMRLR1	16-bit timer register/ 16-bit reload register	R/W		X X X X X X X X B
00003FH					X X X X X X X X B
000040H to 47H	—	Vacancy	*3	—	—
000048H	CSCR0	Chip select control register 0	R/W	Chip select function	– – – – 0 0 0 0 B
000049H	CSCR1	Chip select control register 1	R/W		– – – – 0 0 0 0 B
00004AH	CSCR2	Chip select control register 2	R/W		– – – – 0 0 0 0 B
00004BH	CSCR3	Chip select control register 3	R/W		– – – – 0 0 0 0 B
00004CH	CSCR4	Chip select control register 4	R/W		– – – – 0 0 0 0 B
00004DH	CSCR5	Chip select control register 5	R/W		– – – – 0 0 0 0 B
00004EH	CSCR6	Chip select control register 6	R/W		– – – – 0 0 0 0 B
00004FH	CSCR7	Chip select control register 7	R/W		– – – – 0 0 0 0 B
000050H	—	Vacancy	*3	—	—
000051H	CDCR0	UART0 (SCI) machine clock division control register	W	UART0 (SCI)	– – – – 1 1 1 1 B

(Continued)

Address	Name	Register	Read/ write*4,*5	Resource name	Initial value
000052H	—	Vacancy	*3	—	—
000053H	CDCR1	UART1 (SCI) machine clock division control register	W	UART1 (SCI)	----1111B
000054H to 57H	—	Vacancy	*3	—	—
000058H	TMCSR2	Timer control status register	R/W!	16-bit reload timer 2	00000000B
000059H					----0000B
00005AH	TMR2/ TMRLR2	16-bit timer register/ 16-bit reload register	R/W		XXXXXXXXB
00005BH					XXXXXXXXB
00005CH	TMCSR3	Timer control status register	R/W!	16-bit reload timer 3	00000000B
00005DH					----0000B
00005EH	TMR3/ TMRLR3	16-bit timer register/ 16-bit reload register	R/W		XXXXXXXXB
00005FH					XXXXXXXXB
000060H	TMCSR4	Timer control status register	R/W!	16-bit reload timer 4	00000000B
000061H					----0000B
000062H	TMR4/ TMRLR4	16-bit timer register/ 16-bit reload register	R/W		XXXXXXXXB
000063H					XXXXXXXXB
000064H	TPCR	Timer pin control register	R/W	16-bit reload timer	00010000B
000065H					00110010B
000066H					----0100B
000067H to 6EH	—	Vacancy	*3	—	—
00006FH	ROMM	ROM mirror functional selection module	W	ROM mirror function*9	--------*B
000070H to 8FH	—	Vacancy	*3	—	—
000090H to 9EH	—	Reserved system area	*1	—	—
00009FH	DIRR	Delayed interrupt generation/ release register	R/W	Delayed interrupt generation module	--------0B
0000A0H	LPMCR	Low power consumption mode control register	R/W!	Low power consumption controller circuits	00011000B
0000A1H	CKSCR	Clock selection register	R/W!		11111100B
0000A2H to A4H	—	Vacancy	*3	—	—
0000A5H	ARSR	Auto-ready function selection register	W	External bus pin controller circuits	0011--00B

(Continued)

(Continued)

Address	Name	Register	Read/ write*4,*5	Resource name	Initial value
0000A6H	HACR	External address output control register	W	External bus pin controller circuits	0 0 0 0 0 0 0 0 B
0000A7H	ECSR	Bus control signal selection register	W		– 0 0 * 0 0 0 0 B
0000A8H	WDTC	Watchdog timer control register	R/W!	Watchdog timer	X X X X X 1 1 1 B
0000A9H	TBTC	Timebase timer control register	R/W!	Timebase timer	1 – – 0 0 1 0 0 B
0000AAH to AFH	—	Vacancy	*3	—	—
0000B0H	ICR00	Interrupt control register 00	R/W!	Interrupt controller	0 0 0 0 0 1 1 1 B
0000B1H	ICR01	Interrupt control register 01	R/W!		0 0 0 0 0 1 1 1 B
0000B2H	ICR02	Interrupt control register 02	R/W!		0 0 0 0 0 1 1 1 B
0000B3H	ICR03	Interrupt control register 03	R/W!		0 0 0 0 0 1 1 1 B
0000B4H	ICR04	Interrupt control register 04	R/W!		0 0 0 0 0 1 1 1 B
0000B5H	ICR05	Interrupt control register 05	R/W!		0 0 0 0 0 1 1 1 B
0000B6H	ICR06	Interrupt control register 06	R/W!		0 0 0 0 0 1 1 1 B
0000B7H	ICR07	Interrupt control register 07	R/W!		0 0 0 0 0 1 1 1 B
0000B8H	ICR08	Interrupt control register 08	R/W!		0 0 0 0 0 1 1 1 B
0000B9H	ICR09	Interrupt control register 09	R/W!		0 0 0 0 0 1 1 1 B
0000BAH	—	Vacancy	*3		—
0000BBH	ICR11	Interrupt control register 11	R/W!		0 0 0 0 0 1 1 1 B
0000BCH	—	Vacancy	*3		—
0000BDH	ICR13	Interrupt control register 13	R/W!		0 0 0 0 0 1 1 1 B
0000BEH	ICR14	Interrupt control register 14	R/W!		0 0 0 0 0 1 1 1 B
0000BFH	ICR15	Interrupt control register 15	R/W!		0 0 0 0 0 1 1 1 B
0000C0H to FFH	(External area)*2				

Initial values

0: The initial value for this bit is “0”.
1: The initial value for this bit is “1”.
*: The initial value for this bit is “1” or “0”. (Determined by the level of the MD0 to MD2 pins.)
X: The initial value for this bit is undefined.
–: This bit is not used. The initial value is undefined.

*1: Access prohibited.

*2: This is the only external access area in the area below address 0000FFH. Access this address as an external I/O area.

*3: Areas marked as “Vacancy” in the I/O map are reserved areas. These areas are accessed by internal access. No access signals are output on the external bus.

*4: The R/W! symbol in the read/write column indicates that some bits are read-only or write-only. See the resource’s register list for details.

(Continued)

(Continued)

5: Using a read-modify-write instruction (such as the bit set instruction) to access one of the registers indicated by R/W!, R/W, or W in the read/write column sets the specified bit to the desired value. However, this can cause misoperation if the other register bits include write-only bits. Therefore, do not use read-modify-write instructions to access these registers.

*6: This register is only available when the address/data bus is in multiplex mode and in single-chip mode. Access to the register is prohibited in non-multiplex mode.

*7: This register is only available when the external data bus is in 8-bit mode and in single-chip mode. Access to the register is prohibited in 16-bit mode.

*8: All bits of DDR0/PDR0, 6-bit/7-bit of DDR5/PDR5 and 0-bit of DDRA/PDRA are available only in single-chip mode.

*9: The initial value of this register in MB90V640A is “0” and that of in MB90P641A, MB90641A is “1”.

Note: The initial values listed for write-only bits are the initial values set by a reset. Take attention that they are not the values returned by a read.
Also, LPMCR/CKSCR/WDTC are sometimes initialized and sometimes not initialized, depending on the reset type. The listed initial values are for when these registers are initialized.

■ INTERRUPT VECTOR AND INTERRUPT CONTROL REGISTER ASSIGNMENTS TO INTERRUPT SOURCES

Interrupt source	I²OS support	Interrupt vector			Interrupt control register	
		Number		Address	ICR	Address
Reset	×	#08	08H	FFFFDCH	—	—
INT 9 instruction	×	#09	09H	FFFFD8H	—	—
Exception	×	#10	0AH	FFFFD4H	—	—
DTP/external interrupt #0	○	#11	0BH	FFFFD0H	ICR00	0000B0H
DTP/external interrupt #1	○	#13	0DH	FFFFC8H	ICR01	0000B1H
DTP/external interrupt #2	○	#15	0FH	FFFFC0H	ICR02	0000B2H
DTP/external interrupt #3	○	#17	11H	FFFFB8H	ICR03	0000B3H
16-bit reload timer #2	○	#18	12H	FFFFB4H		
DTP/external interrupt #4	○	#19	13H	FFFFB0H	ICR04	0000B4H
16-bit reload timer #3	○	#20	14H	FFFFACH		
DTP/external interrupt #5	○	#21	15H	FFFFA8H	ICR05	0000B5H
16-bit reload timer #4	○	#22	16H	FFFFA4H		
DTP/external interrupt #6	○	#23	17H	FFFFA0H	ICR06	0000B6H
UART0 • send complete	○	#24	18H	FFFF9CH		
DTP/external interrupt #7	○	#25	19H	FFFF98H	ICR07	0000B7H
UART1 • send complete	○	#26	1AH	FFFF94H		
8/16-bit PPG #0	×	#27	1BH	FFFF90H	ICR08	0000B8H
8/16-bit PPG #1	×	#28	1CH	FFFF8CH		
16-bit reload timer #0	○	#29	1DH	FFFF88H	ICR09	0000B9H
16-bit reload timer #1	○	#30	1EH	FFFF84H		
Vacancy	○	#31	1FH	FFFF80H	ICR10	0000BAH
Timebase timer interval interrupt	×	#34	22H	FFFF74H	ICR11	0000BBH
Vacancy	—	#35	23H	FFFF70H	ICR12	0000BCH
UART1 • receive complete	◎	#37	25H	FFFF68H	ICR13	0000BDH
UART0 • receive complete	◎	#39	27H	FFFF60H	ICR14	0000BEH
Delayed interrupt generation module	×	#42	2AH	FFFF54H	ICR15	0000BFH

○ : indicates that the interrupt request flag is cleared by the I²OS interrupt clear signal (no stop request).
◎ : indicates that the interrupt request flag is cleared by the I²OS interrupt clear signal (with stop request).
× : indicates that the interrupt request flag is not cleared by the I²OS interrupt clear signal.

Note: Do not specify I²OS activation in interrupt control registers that do not support I²OS.

■ PERIPHERAL RESOURCES

1. Parallel Port

The MB90640A series has 75 I/O pins, and 8 open-drain output pins.

Ports 0 to 5 and ports 7 to 9 and A are I/O ports. The ports are inputs when the corresponding direction register bit is “0” and outputs when the corresponding bit is “1”.

Port 0 is only available in single-chip mode.

Port 1 is only available when in data bus 8-bit mode of non-multiplex mode or in single-chip mode.

Ports 2 and 3 are only available when the address/data bus is in multiplex mode and single-chip mode.

Port 6 is an open-drain port.

(1) Register Details

- **Port data registers**

- **Port data register**

Address : PDR1: 000001H
PDR3: 000003H
PDR5: 000005H
PDR7: 000007H
PDR9: 000009H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
PDx7	PDx6	PDx5	PDx4	PDx3	PDx2	PDx1	PDx0	XXXXXXXXB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address : PDR0: 000000H
PDR2: 000002H
PDR4: 000004H
PDR6: 000006H
PDR8: 000008H
PDRA: 00000AH

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PDx7	PDx6	PDx5	PDx4	PDx3	PDx2	PDx1	PDx0	XXXXXXXXB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
X : Indeterminate

Note: No register bit is provided for bits 0, 7 of port 7.
No register bit is provided for bit 7 of port 8.
No register bits are provided for bits 7, 6 of port 9.
Port 0 is only available in single-chip mode.
Bits 7, 6 of port 5 and bit 0 of port A are only available in single-chip mode.
Port 1 is only available when the external data bus is in 8-bit mode and single-chip mode.
Ports 2, 3 are only available in multiplex mode and single-chip mode.

Each port pin except port 6 can be specified as either an input or output by its corresponding direction register when the pin is not set for use by a peripheral. When a port is set as an input, reading the data register always reads the value corresponding to the pin level. When a port is set as an output, reading the data register reads the data register latch value. The same applies when reading using a read-modify-write instruction.
When used as control outputs, reading the data register reads the control output value, irrespective of the direction register value.

Notes: • If read-modify-write instructions (bit set instruction, etc.) are used to access this register, the bit that is the focus of the instruction is set to the prescribed value, but the contents of the output register corresponding to any other bits for which the input setting has been made are overwritten with the current input value of the corresponding pin. Therefore, when switching a pin that was being used for input over to output, first write the desired value to PDR, and then set the data DDR as output direction.

- Reading and writing an I/O port differs from reading and writing memory as follows:

  Input mode
  Reads: The read data is the level of the corresponding pin.
  Writes: The write data is stored in the output latch. The data is not output to the pin.
  Output mode
  Reads: The read data is the value stored in the PDR.
  Writes: The write data is both stored in the output latch and output to the pin.
- Take attention that the operation of R/W in port 6 is different from that of in other port.

Port 6 (P67 to P60) is an general-purpose I/O port with an open-drain output. When port 6 is used as a general-purpose port, always be sure to set the corresponding bits in DDR6 to “0”.

When port 6 is used as an input port, it is necessary set the output port data register value to “1” in order to turn off the open-drain output transistor; it is also necessary to connect a pull-up resistor to the external pins.

In addition, depending on the instruction used to read these bits, one of the following two different operations is performed:

- When read by a read-modify-write instruction:
  The contents of the output port data register are read. Even if pins are forcibly set to “0” externally, the contents of the bits not specified by the instruction do not change.
- When read by any other instruction:
  The pin level can be read.

When used as output ports, the pin values can be changed by writing the desired value to the corresponding output port data register.

In addition, the pin which corresponds to the bit of which port 6 direction register is set to “1” can be read “0”.

- **Port direction registers**

- **Port direction register**

Address : DDR1 : 000011H
DDR3 : 000013H
DDR5 : 000015H
DDR7 : 000017H
DDR9 : 000019H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
DDx7	DDx6	DDx5	DDx4	DDx3	DDx2	DDx1	DDx0	00000000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address : DDR0 : 000010H
DDR2 : 000012H
DDR4 : 000014H
DDR8 : 000018H
DDRA : 00001AH

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
DDx7	DDx6	DDx5	DDx4	DDx3	DDx2	DDx1	DDx0	00000000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable

Note: No register bit is provided for bits 0, 7 of port 7.
No register bit is provided for bit 7 of port 8.
No register bits are provided for bits 6, 7 of port 9.
Port 1 is only available in single-chip mode.
Port 1 is only available when the external data bus is in 8-bit mode and single-chip mode.
Ports 2, 3 are only available in multiplex mode and single-chip mode.

When pins are used as ports, the register bits control the corresponding pins as follows.
0: Input mode
1: Output mode

Bits are set to “0” by a reset.

- **Port 6 direction register**

- **Port 6 direction register**

Address : DDR6 : 000016H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
DD67	DD66	DD65	DD64	DD63	DD62	DD61	DD60	11111111B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

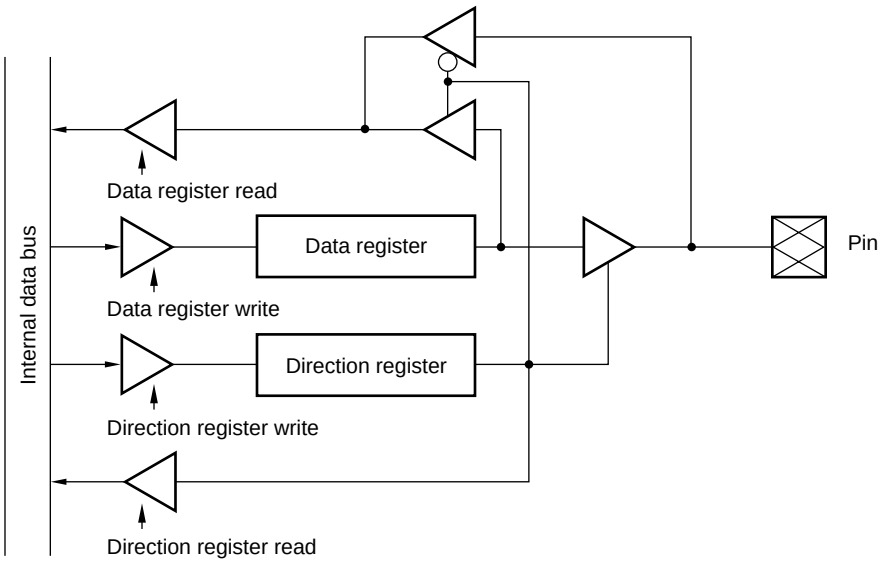
R/W : Readable and writable

Controls each pin of port 6 as follows.
0: Port input mode
1: Analog input mode

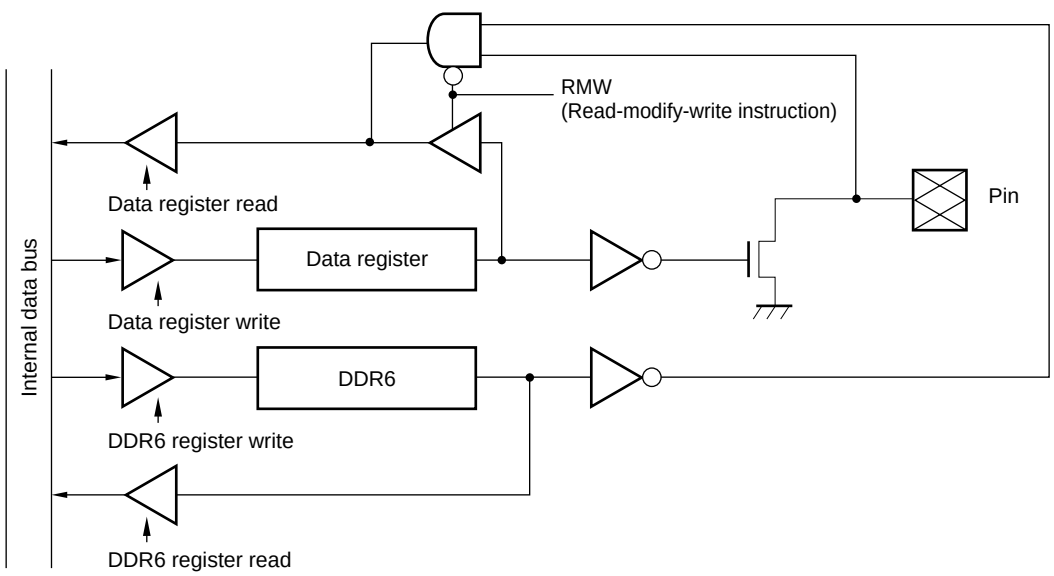
Bits are set to “1” by a reset.

(2) Block Diagrams

- **I/O port**



- **Open-drain port**



(3) Port Pin Allocation

Ports 1, 4, and 5 on the MB90640A series share pins with the external bus. The pin functions are determined by the bus mode and register settings.

Pin name	Function							
	Non-multiplex mode				Multiplex mode			
	External address control				External address control			
	Enable (address)		Disable (port)		Enable (address)		Disable (port)	
	External bus width		External bus width		External bus width		External bus width	
	8 bits	16 bits	8 bits	16 bits	8 bits	16 bits	8 bits	16 bits
D07 to D00/ AD07 to AD00	D07 to D00				AD07 to AD00			
P17 to P10/ D15 to D08/ AD15 to AD08	Port	D15 to D08	Port	D15 to D08	A15 to A08	AD15 to AD08	A15 to A08	AD15 to AD08
P27 to P20/ A07 to A00	A07 to A00				Port			
P37 to P30/ A15 to A08	A15 to A08							
P47 to P40/ A23 to A16	A23 to A16		Port		A23 to A16		Port	
P57/ALE	ALE				ALE			
$\overline{RD}$	$\overline{RD}$				$\overline{RD}$			
P55/$\overline{WRL}$	$\overline{WRL}$				$\overline{WRL}$			
P54/$\overline{WRH}$	Port	$\overline{WRH}$	Port	$\overline{WRH}$	Port	$\overline{WRH}$	Port	$\overline{WRH}$
P53/HRQ	HRQ				HRQ			
P52/$\overline{HAK}$	$\overline{HAK}$				$\overline{HAK}$			
P51/RDY	RDY				RDY			
P50/CLK	CLK				CLK			

Notes: • The upper address, $\overline{WRL}$, $\overline{WRH}$, $\overline{HAK}$, HRQ, RDY, and CLK can be set for use as ports by function selection.
• The pins mentioned above can be used as a port in single-chip mode.

2. UART0, 1 (SCI)

UART0, 1 are serial I/O ports that can be used for CLK asynchronous (start-stop synchronization) or CLK synchronous (I/O expansion serial) data transfer. The ports have the following features.

- Full duplex, double buffered
- Supports CLK asynchronous (start-stop synchronization) and CLK synchronous (I/O expansion serial) data transfer
- Multi-processor mode support
- Built-in dedicated baud rate generator
  CLK asynchronous: 62500 bps/31250 bps/19230 bps/9615 bps/4808 bps/2404 bps/1202 bps
  CLK synchronous: 2 Mbps/1 Mbps/500 kbps/250 kbps
- Supports flexible baud rate setting using an external clock
- Error detect function (parity, framing, and overrun)
- NRZ type transmission signal
- Intelligent I/O service support

(1) Register Configuration

- **Serial mode register 0, 1**

Address : SMR0: 000020H
SMR1: 000024H

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
	MD1	MD0	CS2	CS1	CS0	—	SCKE	SOE	00000-00B
	R/W	R/W	W	W	W	—	R/W	R/W	

- **Serial control register 0, 1**

Address : SCR0: 000021H
SCR1: 000025H

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
	PEN	P	SBL	CL	A/D	REC	RXE	TXE	00000100B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **Input data register 0, 1/output data register 0, 1**

Address : SIDR0 (read) / SODR0 (write) : 000022H
SIDR1 (read) / SODR1 (write) : 000026H

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **Serial status register 0, 1**

Address : SSR0: 000023H
SSR1: 000027H

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
	PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE	00001-00B
	R	R	R	R	R	—	R/W	R/W	

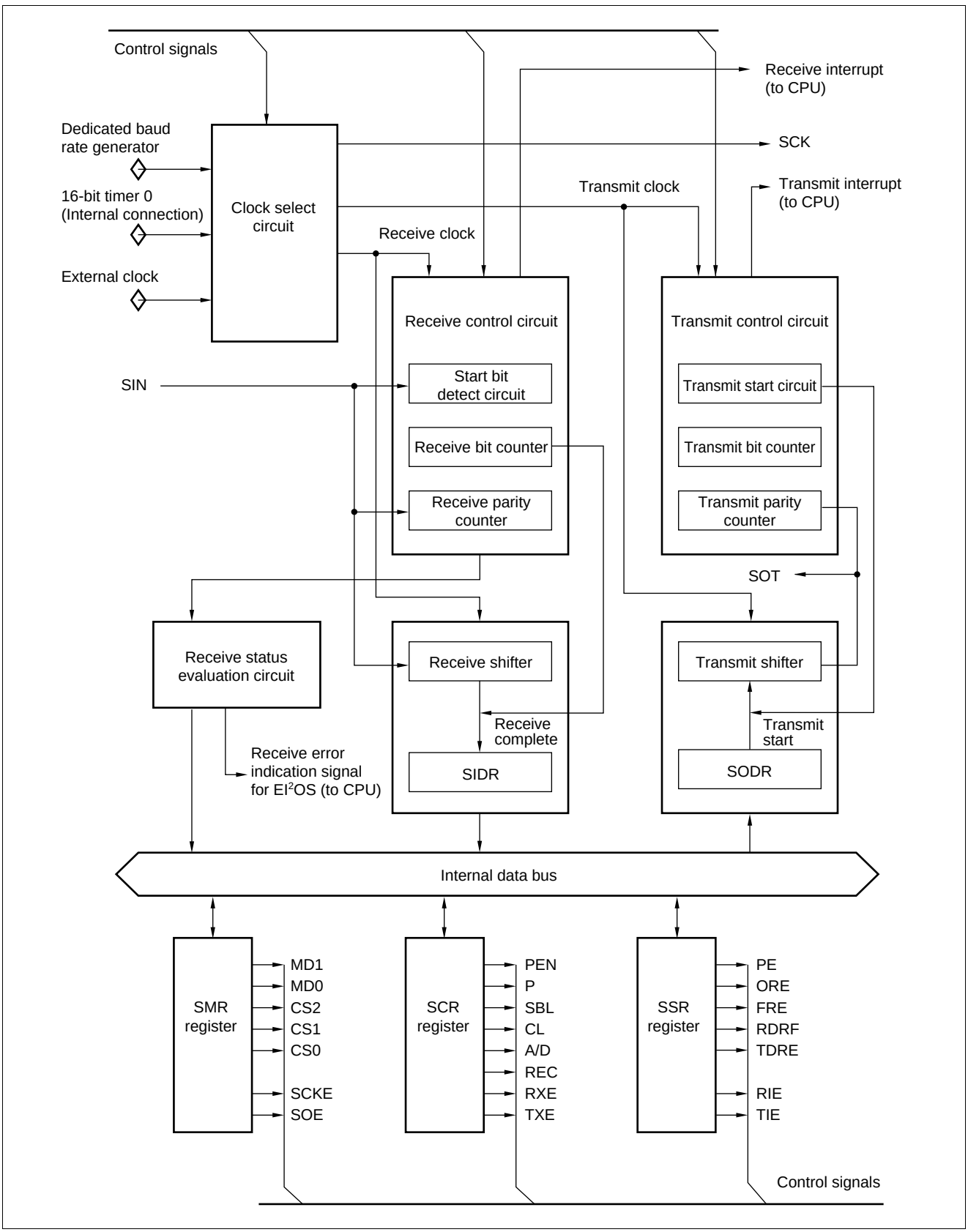
- **Machine clock division control register for UART0, 1 (SCI)**

Address : CDCR0: 000051H
CDCR1: 000053H

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
	—	—	—	—	DIV3	DIV2	DIV1	DIV0	----1111B
	—	—	—	—	W	W	W	W	

R/W: Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate

(2) Block Diagram



3. 8/16-bit PPG

8/16-bit PPG contains the 8-bit reload timer module. The block performs PPG output in which the pulse output is controlled by the operation of the timer.

The hardware consists of two 8-bit down-counters, four 8-bit reload registers, one 16-bit control register, two external pulse output pins, and two interrupt outputs. The PPG has the following functions.

- 8-bit PPG output in 2-channel independent operation mode: Two independent PPG output channels are available.
- 16-bit PPG output operation mode: One 16-bit PPG output channel is available.
- 8+8-bit PPG output operation mode: Variable-period 8-bit PPG output operation is available by using the output of channel 0 as the clock input to channel 1.
- PPG output operation: Outputs pulse waveforms with variable period and duty ratio.
  Can be used as a D/A converter in conjunction with an external circuit.

(1) Register Configuration

- **PPG0 operation mode control register**

Address : PPGC0: 000030H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PEN0	—	POE0	PIE0	PUF0	PCM1	PCM0	Reserved	0-000001B
R/W	—	R/W	R/W	R/W	R/W	R/W	—	

- **PPG1 operation mode control register**

Address : PPGC1: 000031H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
PEN1	PCS1	POE1	PIE1	PUF1	MD1	MD0	Reserved	00000001B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	—	

- **PPG0, PPG1 reload register H**

Address : PRLH0: 000035H
PRLH1: 000037H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
								XXXXXXXXB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **PPG0, PPG1 reload register L**

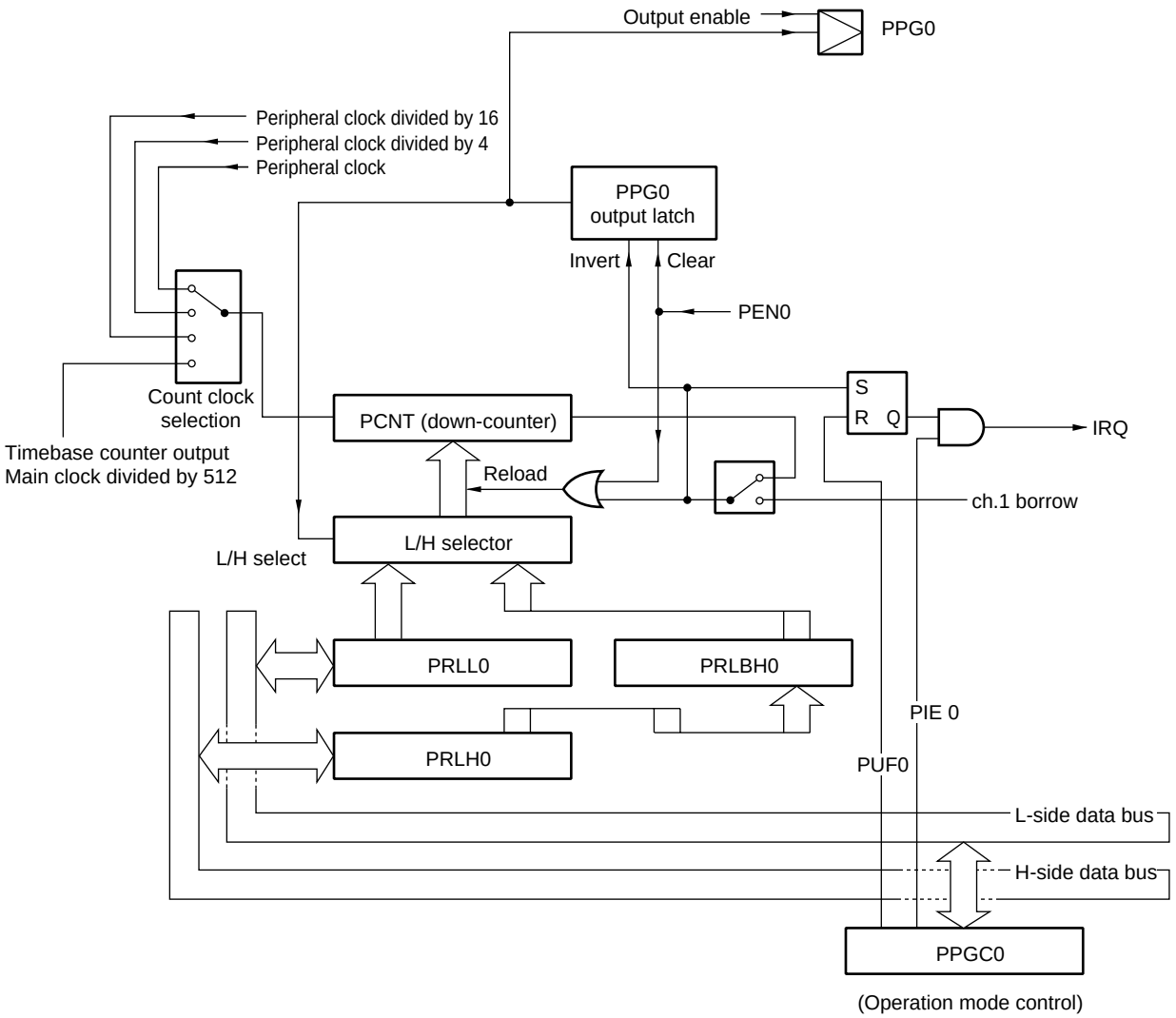
Address : PRLL0: 000034H
PRLL1: 000036H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
								XXXXXXXXB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

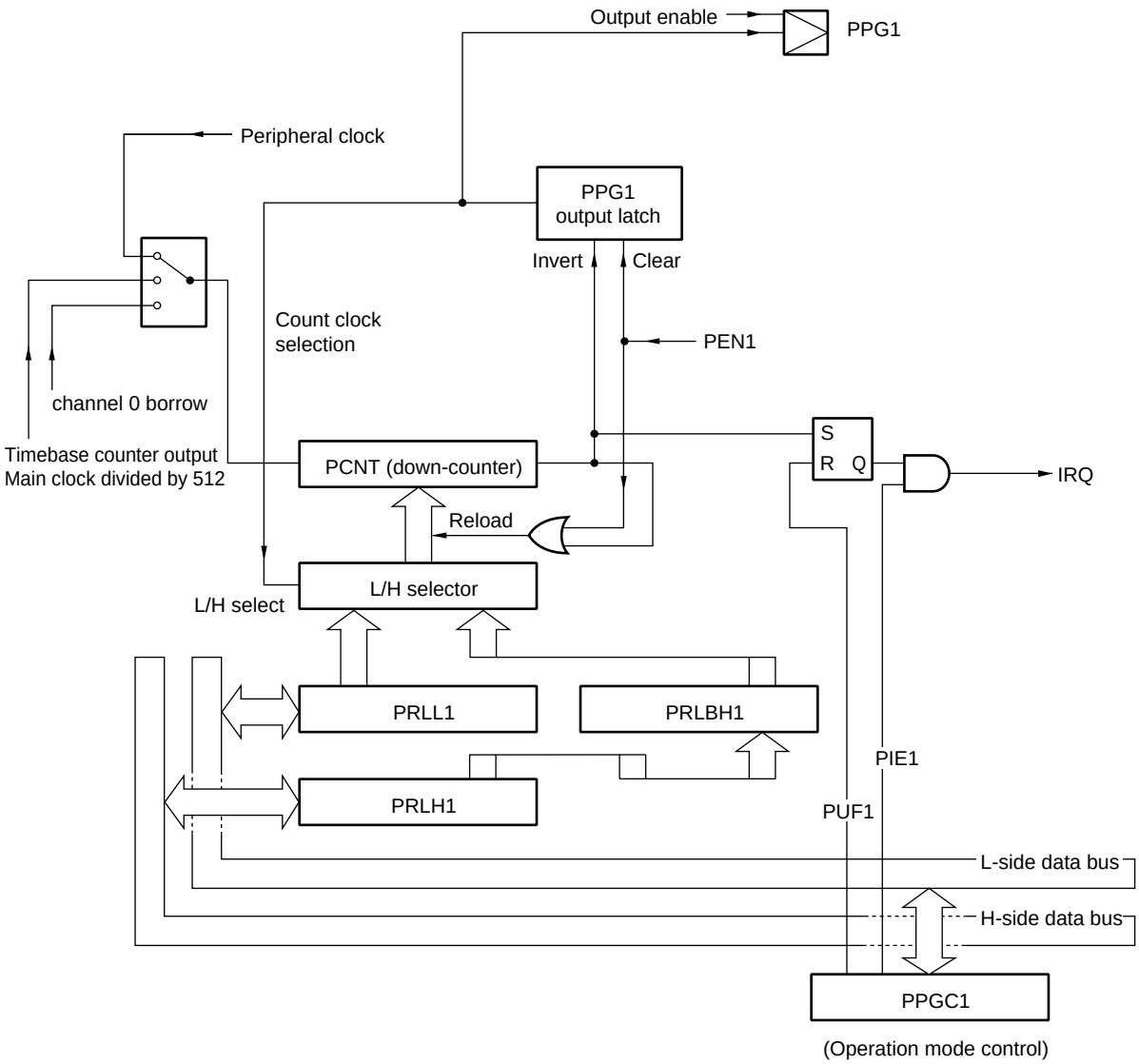
R/W : Readable and writable
— : Unused
X : Indeterminate

(2) Block Diagram

- **8/16-bit PPG (channel 0)**



- **8/16-bit PPG (channel 1)**



4. 16-bit Reload Timer (with Event Count Function)

The 16-bit reload timers consists of a 16-bit down-counter, a 16-bit reload register, input pin (TIN), output pin (TOT), and a control register. The input clock can be selected from one external clock and three types of internal clock. The output (TOT) outputs a toggle waveform in reload mode and a rectangular waveform during counting in one-shot mode. The input (TIN) functions as the event input in event count mode and as the trigger input or gate input in internal clock mode.

Input and output of timer pin TIM0 to TIM4 are set by way of the timer pin control register.

This product has five internal 16-bit reload timer channels.

(1) Register Configuration

- **Timer control status register upper**

Address : TMCSR0: 000039H
TMCSR1: 00003DH
TMCSR2: 000059H
TMCSR3: 00005DH
TMCSR4: 000061H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
—	—	—	—	CSL1	CSL0	MOD2	MOD1	----0000B
—	—	—	—	R/W	R/W	R/W	R/W	

- **Timer control status register lower**

Address : TMCSR0: 000038H
TMCSR1: 00003CH
TMCSR2: 000058H
TMCSR3: 00005CH
TMCSR4: 000060H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **16-bit timer register upper/16-bit reload register upper**

Address : TMR0/TMRLR0: 00003BH
TMR1/TMRLR1: 00003FH
TMR2/TMRLR2: 00005BH
TMR3/TMRLR3: 00005FH
TMR4/TMRLR4: 000063H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
								XXXXXXXXB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **16-bit timer register lower/16-bit reload register lower**

Address : TMR0/TMRLR0: 00003AH
TMR1/TMRLR1: 00003EH
TMR2/TMRLR2: 00005AH
TMR3/TMRLR3: 00005EH
TMR4/TMRLR4: 000062H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
								XXXXXXXXB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
— : Unused
X : Indeterminate

- **Timer pin control register upper**

Address : TPCR : 000066H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
—	—	—	—	OTE4	CSC4	CSB4	CSA4	----0100B
—	—	—	—	R/W	R/W	R/W	R/W	

- **Timer pin control register middle**

Address : TPCR : 000065H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
OTE3	CSC3	CSB3	CSA3	OTE2	CSC2	CSB2	CSA2	00110010B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

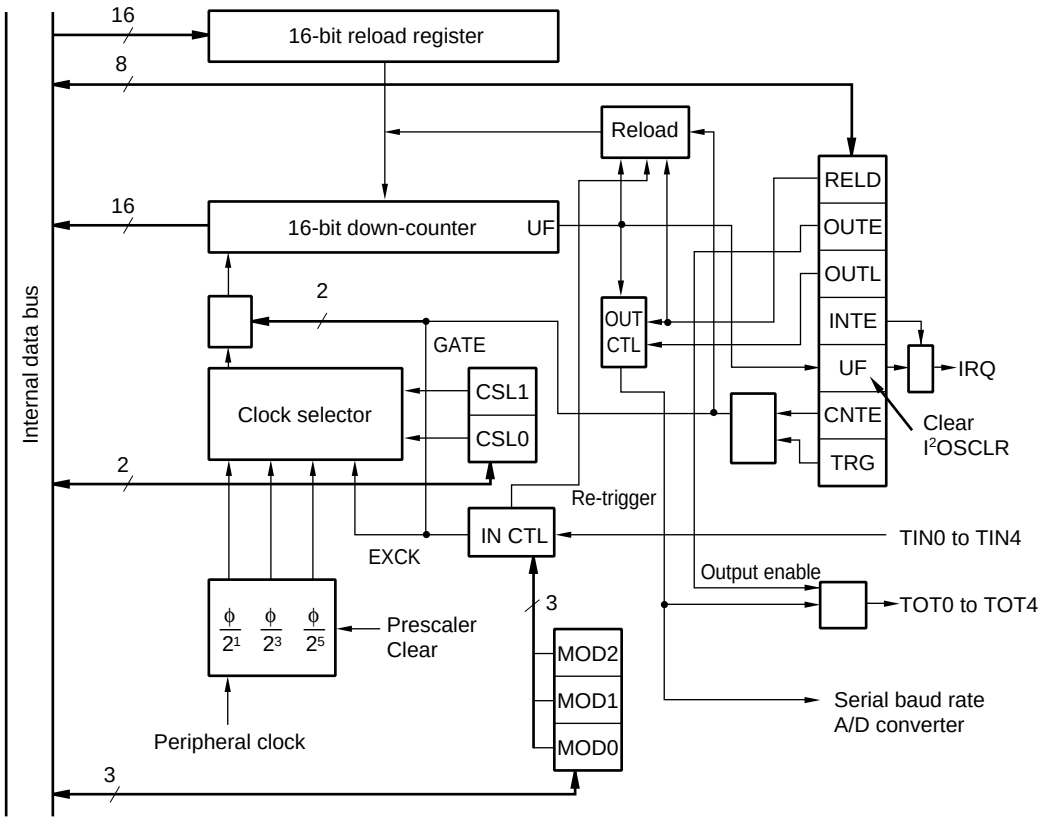
- **Timer pin control register lower**

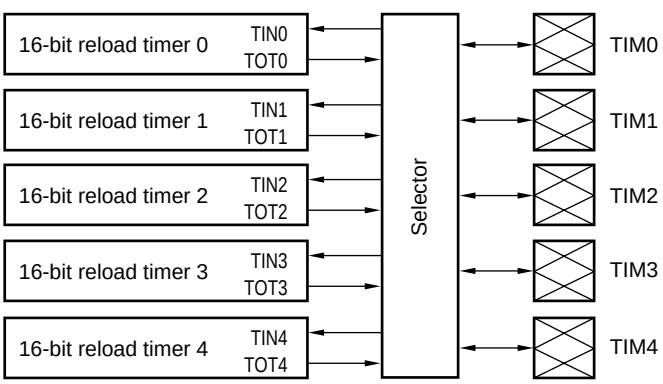
Address : TPCR : 000064H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
OTE1	CSC1	CSB1	CSA1	OTE0	CSC0	CSB0	CSA0	00010000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
— : Unused
X : Indeterminate

(2) Block Diagram





Note: Timer channel and direction (I/O) can be selected for each pin.

5. Chip Select Function

This module generates chip select signals to simplify connection of memory or I/O devices.

The module has 8 chip select output pins. The hardware outputs the chip select signals from the pins when it detects access of an address in the areas specified in the pin registers.

(1) Register Configuration

- **Chip select control register 1, 3, 5, 7**

Address : CSCR1: 000049H
CSCR3: 00004BH
CSCR5: 00004DH
CSCR7: 00004FH

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
—	—	—	—	ACTL	OPEL	CSA1	CSA0	----0000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

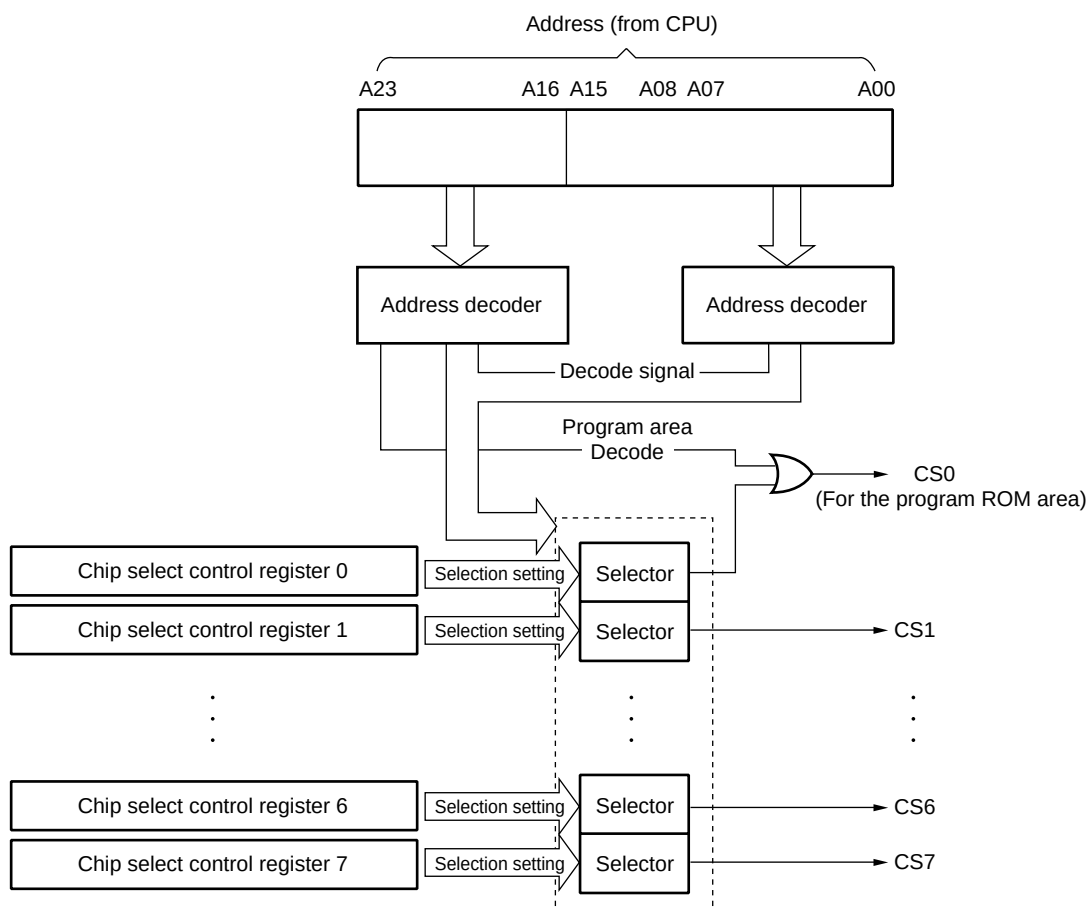
- **Chip select control register 0, 2, 4, 6**

Address : CSCR0: 000048H
CSCR2: 00004AH
CSCR4: 00004CH
CSCR6: 00004EH

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
—	—	—	—	ACTL	OPEL	CSA1	CSA0	----0000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
— : Unused

(2) Block Diagram



6. DTP/External Interrupts

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F²MC-16L CPU. The DTP receives DMA and interrupt processing requests from external peripherals and passes the requests to the F²MC-16L CPU to activate the extended intelligent I/O service or interrupt processing. Two request levels ("H" and "L") are provided for extended intelligent I/O service. For external interrupt requests, generation of interrupts on a rising or falling edge as well as on "H", "L" levels can be selected, giving a total of four types.

(1) Register Configuration

- **Interrupt/DTP enable register**

Address : ENIR: 000028H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **Interrupt/DTP source register**

Address : EIRR: 000029H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	XXXXXXXXB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **Request level setting register upper**

Address : ELVR: 00002BH

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	00000000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

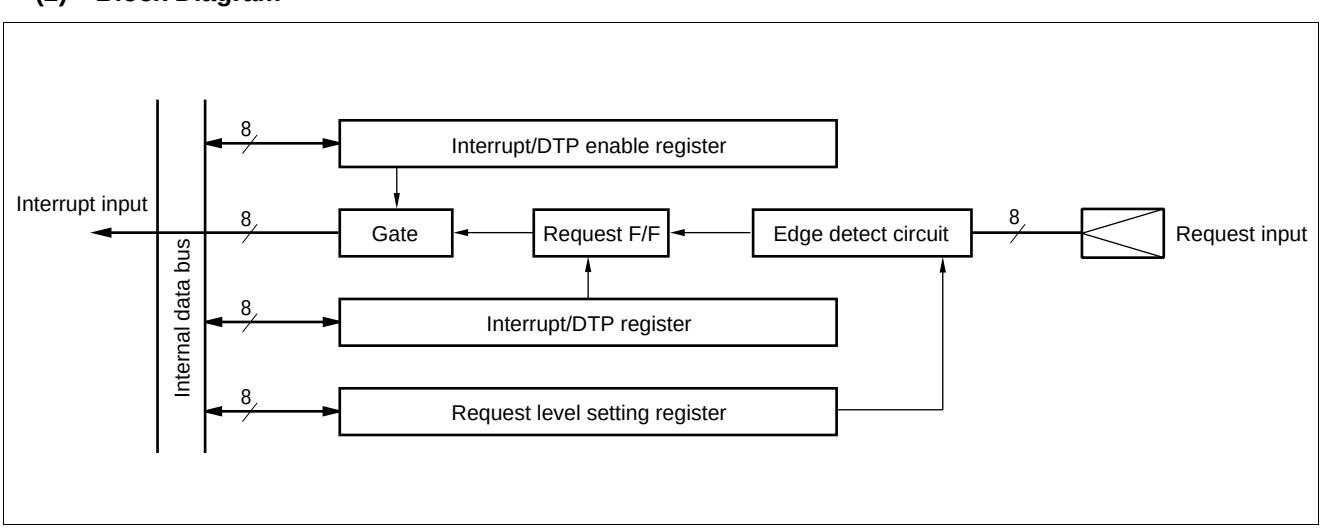
- **Request level setting register lower**

Address : ELVR: 00002AH

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
X : Indeterminate

(2) Block Diagram



7. Delayed Interrupt Generation Module

The delayed interrupt generation module is used to generate the task switching interrupt. Interrupt requests to the F^{2}MC-16L CPU can be generated and cleared by software using this module.

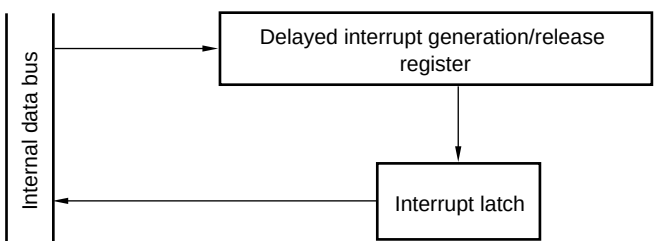
(1) Register Configuration

- **Delayed interrupt generation/release register**

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
Address : DIRR: 00009F$_H$	—	—	—	—	—	—	—	R0	-------0$_B$
	—	—	—	—	—	—	—	R/W	

R/W : Readable and writable
— : Unused

(2) Block Diagram



8. ROM Mirror Functional Selection Module

ROM mirror function selecting module can be refered to the upper 48 Kbytes of FF bank which is wired ROM at 00 bank by selecting the resister setting.

(1) Register Configuration

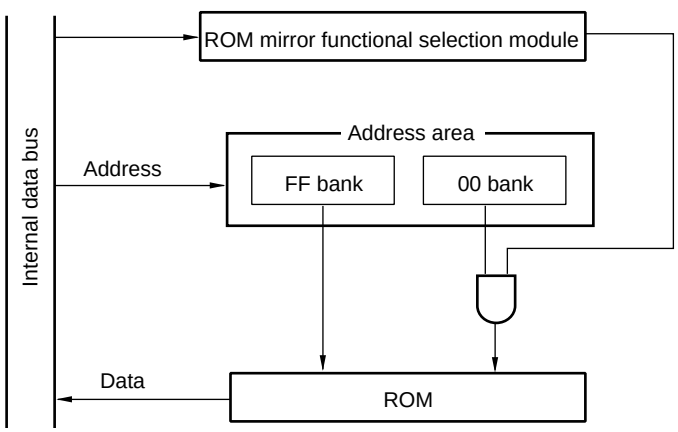
- **ROM mirror functional selection module**

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
Address : ROMM: 00006F$_H$	—	—	—	—	—	—	—	MI	-------*$_B$
	—	—	—	—	—	—	—	W	

W : Write only
— : Unused
* : “1” or “0” (determined owing to the MD0 to MD2 pin level)

Notes: • The initial value of MB90V640A is “0” and that of MB90P641A, MB90641A is “1”.
• Not to access to this register while address 04000$_H$ to 00FFFF$_H$ are in operation.

(2) Block Diagram



9. Watchdog Timer and Timebase Timer

The watchdog timer consists of a 2-bit watchdog counter, a control register, and a watchdog reset controller. The watchdog counter uses the carry-up signal from the 18-bit timebase timer as its clock source.

In addition to the 18-bit timer, the timebase timer contains an interval interrupt control circuit. The timebase timer uses the main clock, regardless of the value of the MCS bit in the CKSCR register.

(1) Register Configuration

- **Watchdog timer control register**

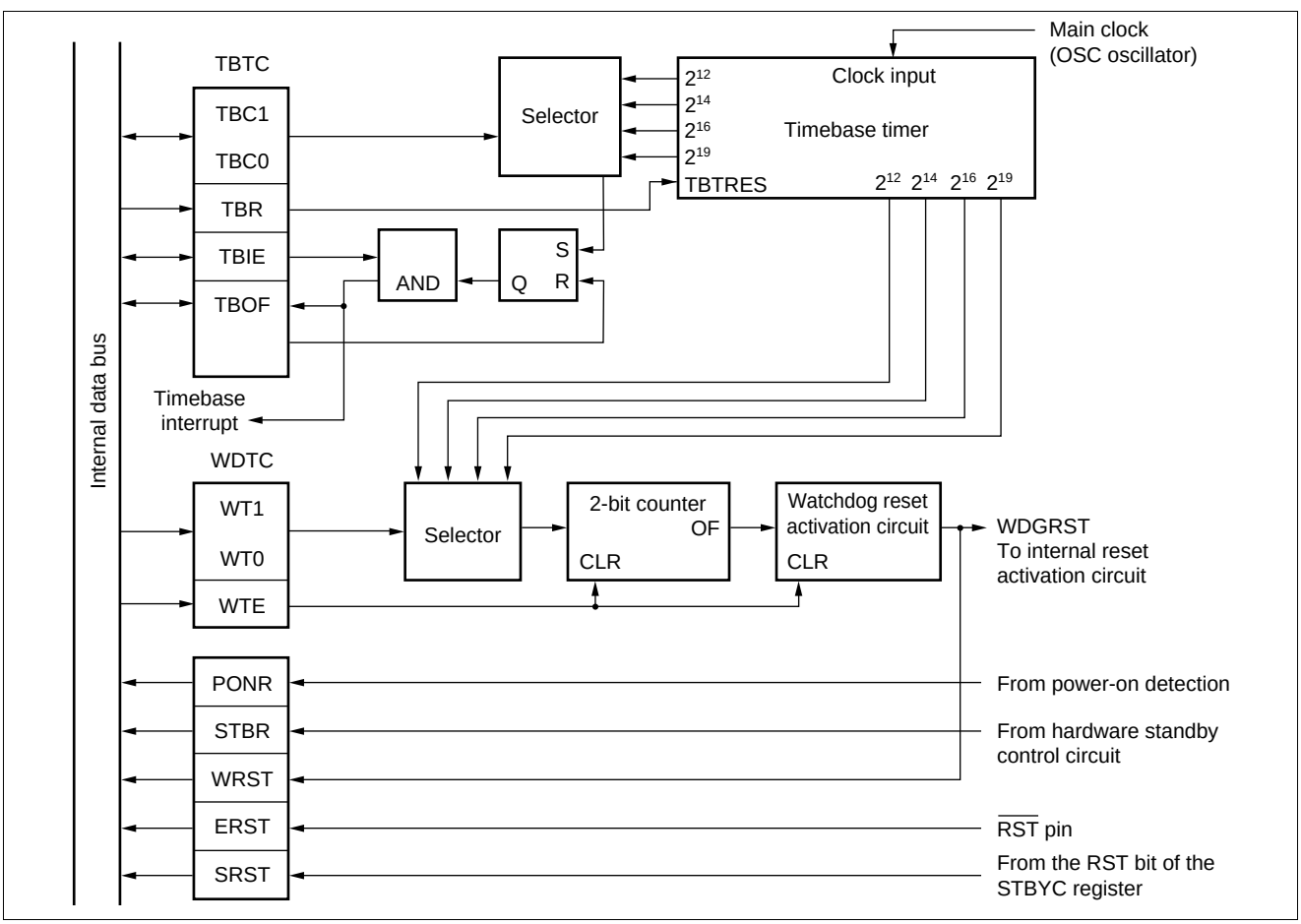
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
Address : WDTC: 0000A8H	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	XXXXX111B
	R	R	R	R	R	W	W	W	

- **Timebase timer control register**

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
Address : TBTC: 0000A9H	Reserved	—	—	TBIE	TBOF	TBR	TBC1	TBC0	1--00100B
	—	—	—	R/W	R/W	W	R/W	R/W	

R/W : Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate

(2) Block Diagram



10. Low-power Control Circuits (CPU Intermittent Operation Function, Oscillation Stabilization Delay Time, and Clock Multiplier Function)

The following operation modes are available: PLL clock mode, PLL sleep mode, timer mode, main clock mode, main sleep mode, stop mode, and hardware standby mode. Operation modes other than PLL clock mode are classified as low-power consumption modes.

In main clock mode and main sleep mode, the device operates on the main clock only (OSC oscillator clock). The PLL clock (VCO oscillator clock) is stopped in these modes and the main clock divided by 2 is used as the operating clock.

In PLL sleep mode and main sleep mode, the CPU's operating clock only is stopped and other elements continue to operate.

In timer mode, only the timebase timer operates.

Stop mode and hardware standby mode stop the oscillator. These modes maintain existing data with minimum power consumption.

The CPU intermittent operation function provides an intermittent clock to the CPU when register, internal memory, internal resource, or external bus access is performed. This function reduces power consumption by lowering the CPU execution speed while still providing a high-speed clock to internal resources.

The PLL clock multiplier ratio can be set to 1, 2, 3, 4 by the CS1, CS0 bits.

The WS1, WS0 bits set the delay time to wait for the main clock oscillation to stabilize when recovering from stop mode or hardware standby mode.

(1) Register Configuration

- **Low-power consumption mode control register**

Address : LPMCR: $0000A0_H$

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
	STP	SLP	SPL	RST	Reserved	CG1	CG0	Reserved	00011000_B
	W	W	R/W	W	—	R/W	R/W	—	

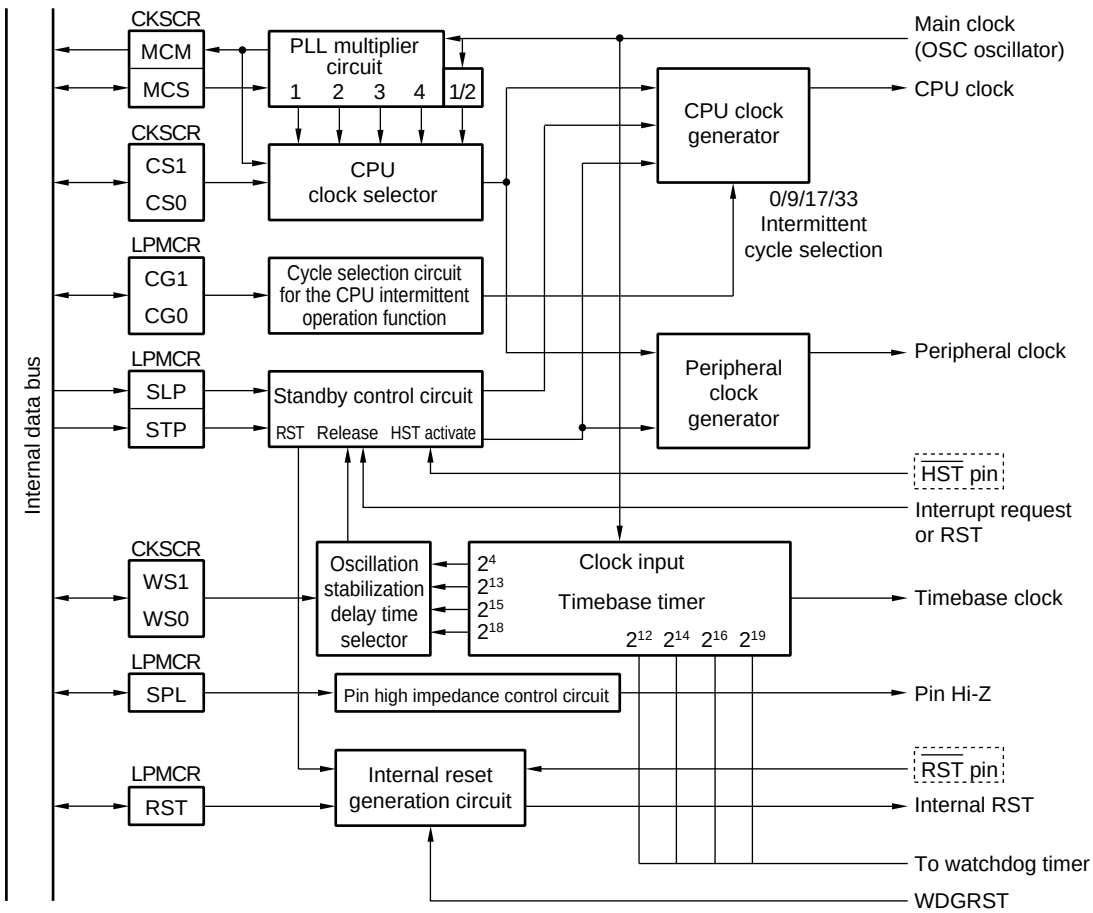
- **Clock select register**

Address : CKSCR: $0000A1_H$

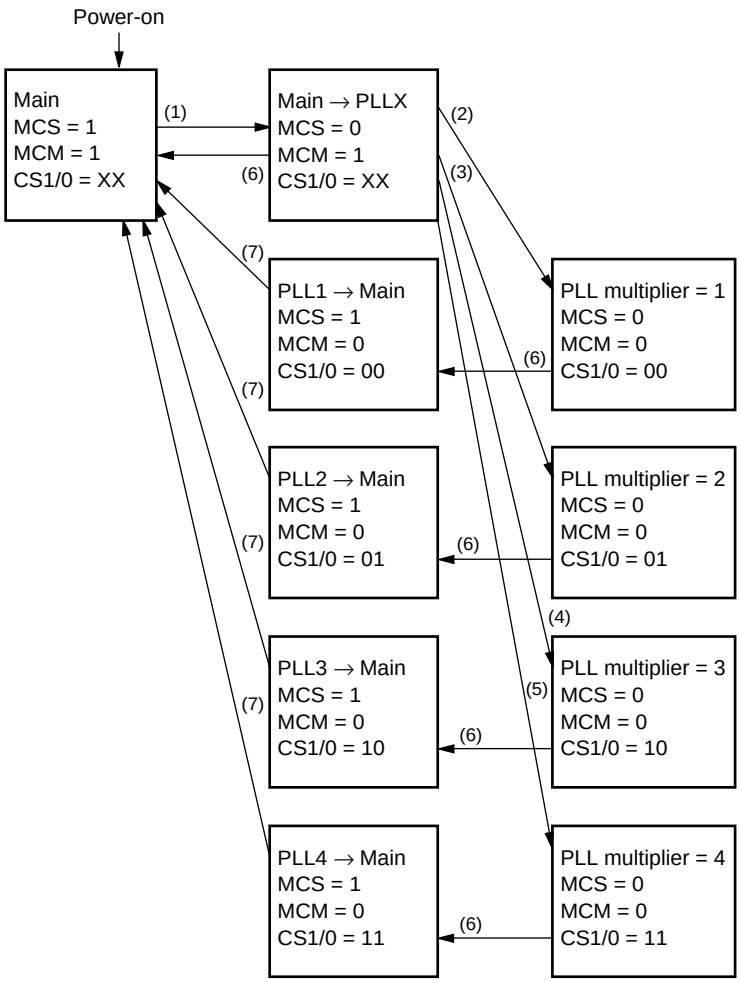
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
Reserved	MCM	WS1	WS0	Reserved	MCS	CS1	CS0	11111100_B
—	R	R/W	R/W	—	R/W	R/W	R/W	

R/W : Readable and writable
R : Read only
W : Write only

(2) Block Diagram



- **State transition diagram for clock selection**



(1) MCS bit cleared
(2) PLL clock oscillation stabilization delay complete and CS1/0 = 00
(3) PLL clock oscillation stabilization delay complete and CS1/0 = 01
(4) PLL clock oscillation stabilization delay complete and CS1/0 = 10
(5) PLL clock oscillation stabilization delay complete and CS1/0 = 11
(6) MCS bit set (including a hardware standby or watchdog reset)
(7) PLL clock and main clock synchronized timing

11. Interrupt Controller

The interrupt control registers are located in the interrupt controller. An interrupt control register is provided for each I/O with an interrupt function. The registers have the following three functions.

- Set the interrupt level of the corresponding peripheral.
- Select whether to treat interrupts from the corresponding peripheral as standard interrupts or activate the extended intelligent I/O service.
- Select the extended intelligent I/O service channel.

(1) Register Configuration

- **Interrupt control register 01, 03, 05, 07, 09, 11, 13, 15**

Address : ICR01: 0000B1H
ICR03: 0000B3H
ICR05: 0000B5H
ICR07: 0000B7H
ICR09: 0000B9H
ICR11: 0000BBH
ICR13: 0000BDH
ICR15: 0000BFH

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
	ICS3	ICS2	ICS1 or S1	ICS0 or S0	ISE	IL2	IL1	IL0	00000111B
	W	W	R/W	R/W	R/W	R/W	R/W	R/W	

- **Interrupt control register 00, 02, 04, 06, 08, 10, 12, 14**

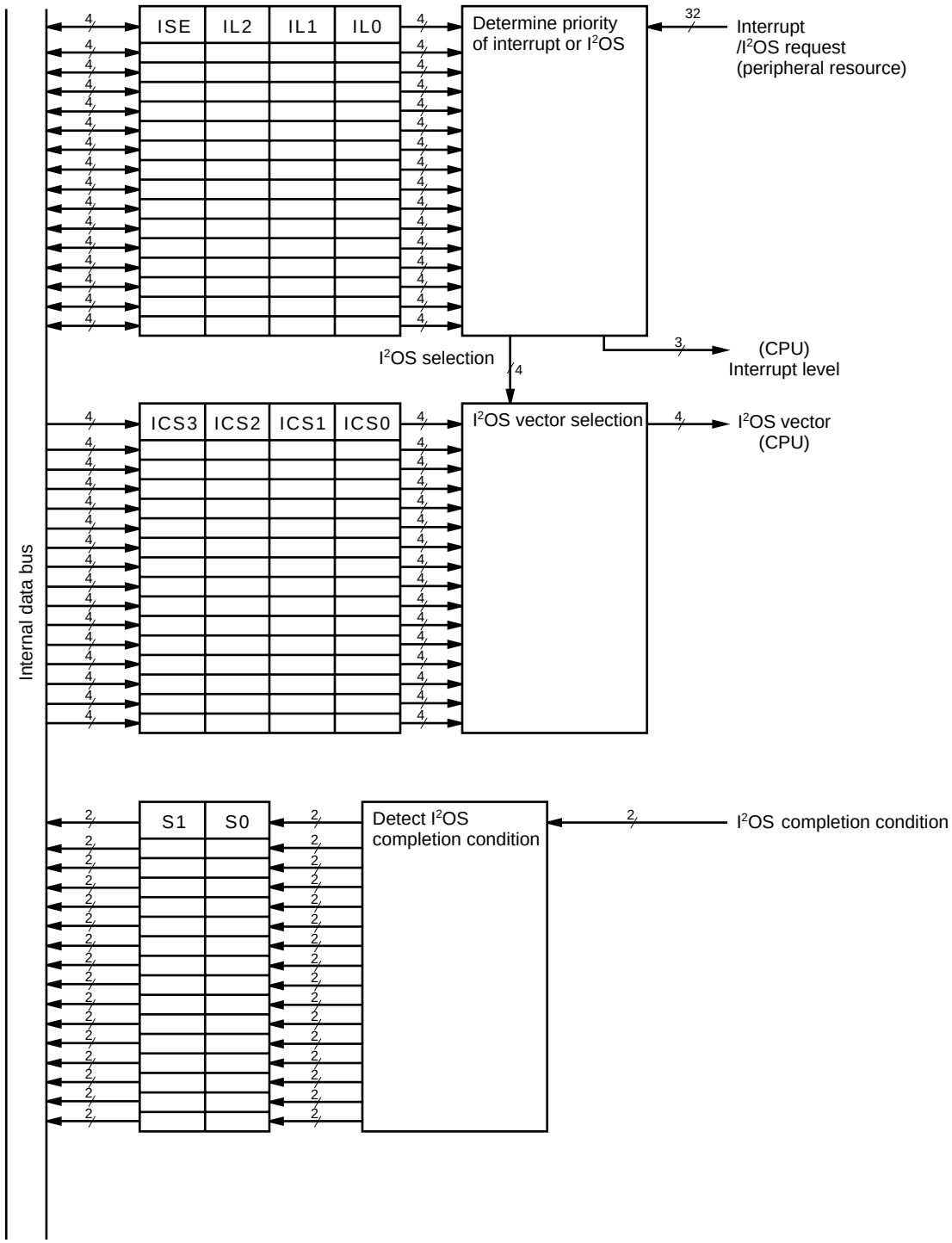
Address : ICR00: 0000B0H
ICR02: 0000B2H
ICR04: 0000B4H
ICR06: 0000B6H
ICR08: 0000B8H
ICR14: 0000BEH

	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
	ICS3	ICS2	ICS1 or S1	ICS0 or S0	ISE	IL2	IL1	IL0	00000111B
	W	W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
W : Write only

Note: Do not access these registers using read-modify-write instructions as this can cause misoperation.

(2) Block Diagram



12. External Bus Terminal Control Circuit

This circuit controls the external bus terminals intended to extend outwardly the CPU's address/data bus.

(1) Register Configuration

- **Register for selection of AUTO ready function**

Address : ARSR: 0000A5H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
IOR1	IOR0	HMR1	HMR0	—	—	LMR1	LMR0	0011--00B
W	W	W	W	—	—	W	W	

- **Register for control of external address output**

Address : HACR: 0000A6H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
E23	E22	E21	E20	E19	E18	E17	E16	00000000B
W	W	W	W	W	W	W	W	

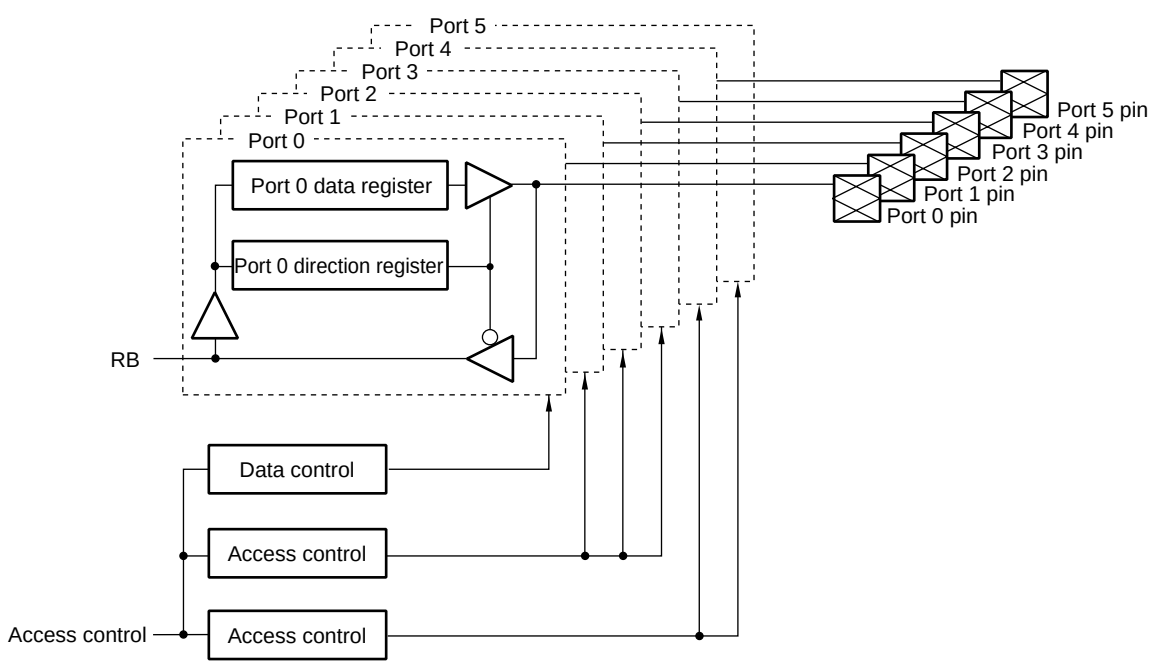
- **Register for selection of bus control signal**

Address : ECSR: 0000A7H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
—	LMBS	WRE	HMBS	IOBS	HDE	RYE	CKE	-00*0000B
—	W	W	W	W	W	W	W	

W: Write only
—: Unused
X : Indeterminate
* : "1" or "0" (determined owing to the MD0 to MD2 pin level)

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current*2	I_{OL}	—	15	mA	
“L” level average output current*3	I_{OLAV}	—	4	mA	
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*4	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*2	I_{OH}	—	–15	mA	
“H” level average output current*3	I_{OHAV}	—	–4	mA	
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current*4	ΣI_{OHAV}	—	–50	mA	
Power consumption	P_D	—	+150	mW	MB90641A
		—	+400	mW	MB90P641A
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: V_I and V_O must not exceed V_{CC} + 0.3 V.
*2: The maximum output current must not be exceeded at any individual pin.
*3: The average output current is the operating current running through an appropriate pin × the operating rate.
*4: The average total output current is the operating current running through all the appropriate pins × the operating rate.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	4.5	5.5	V	For normal operation
	V_{CC}	3.5	5.5	V	To maintain statuses in stop mode
"H" level input voltage	V_{IH}	2.2	V_{CC} + 0.3	V	TTL level input pins
	V_{IHC}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS level input pins
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins*
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD input pin
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.8	V	TTL level input pins
	V_{ILC}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS level input pins
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	Hysteresis input pins*
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD input pin
Smoothing capacitor	C_S	0.1	1.0	µF	Use the ceramic capacitor or the capacitor which has the similar frequency characteristic as ceramic capacitor. When attach the smoothing capacitor to V_{CC}, use the capacitor whose capacitance is larger than C_S.
Operating temperature	T_A	–40	+85	°C	

* : Target pins are P60 to P67, P71 to P76, P80 to P86, P90 to P95, $\overline{HST}$, and $\overline{RST}$. (When used as general purpose pins)

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH}	Other than P60 to P67	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current	I_{IL}	Other than P60 to P67	V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	
Open-drain output leakage current	I_{leak}	P60 to P67	—	—	0.1	5	µA	
Pull-up resistance	R_{UP}	—	—	15	50	100	kΩ	
Pull-down resistance	R_{DOWN}	—	—	15	50	200	kΩ	
Power supply current*	I_{CC}	V_{CC} = 5.0 V	Internal 16 MHz operation Normal operation	—	50	70	mA	MB90V640A/ P641A
				—	15	20	mA	MB90641A
	I_{CCS}		Internal 16 MHz operation Sleep mode	—	25	30	mA	MB90V640A/ P641A
				—	5	10	mA	MB90641A
	I_{CCH}		T_A = +25°C Stop mode	—	0.1	10	µA	MB90V640A/ P641A
				—	5	20	µA	MB90641A
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}, C	—	—	10	—	pF	

* : Because the current values are tentative values, they are subject to change without notice due to our efforts to improve the characteristics of these devices.

4. AC Characteristics

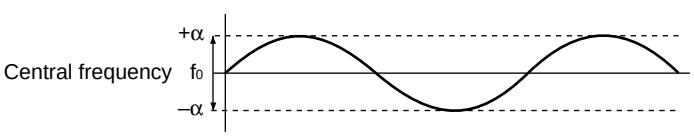
(1) Clock Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

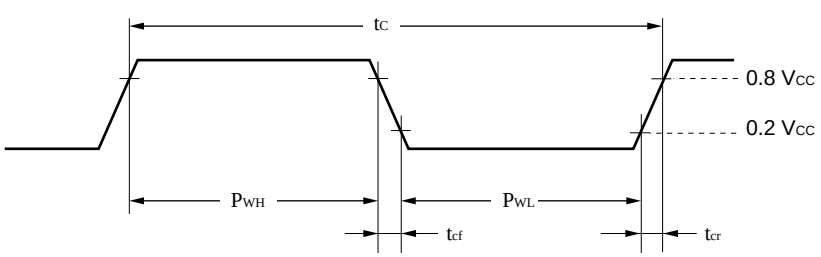
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Source oscillation frequency	F_C	X0, X1	—	3	17	MHz	
Source oscillation cycle time	t_C	X0, X1	—	58.8	333	ns	
Frequency variation ratio* (when locked)	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH} P_{WL}	X0	—	10	—	ns	The duty ratio should be in the range 30 to 70%
Input clock rise time and fall time	t_{cr} t_{cf}	X0	—	—	5	ns	
Internal operating clock frequency	f_{CP}	—	—	1.5	17	MHz	
Internal operating clock cycle time	t_{CP}	—	—	58.8	666	ns	

* : The frequency variation ratio is the maximum variation from the specified central frequency when the multiplier PLL is locked. The value is expressed as a proportion.

$$\Delta f = \frac{|\alpha|}{f_0} \times 100\ (\%)$$

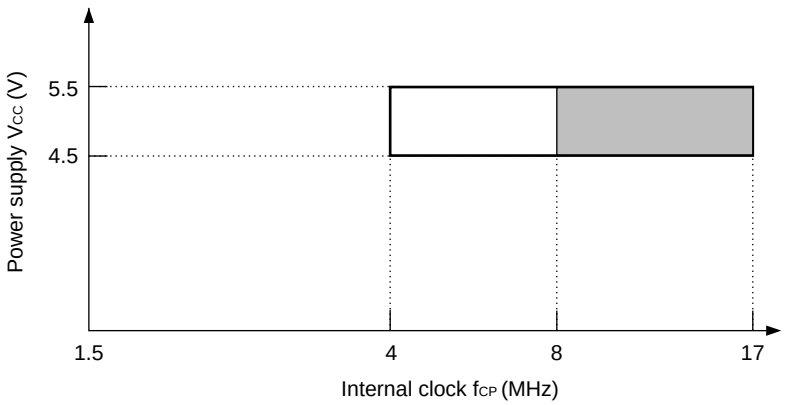


- **Clock timing**



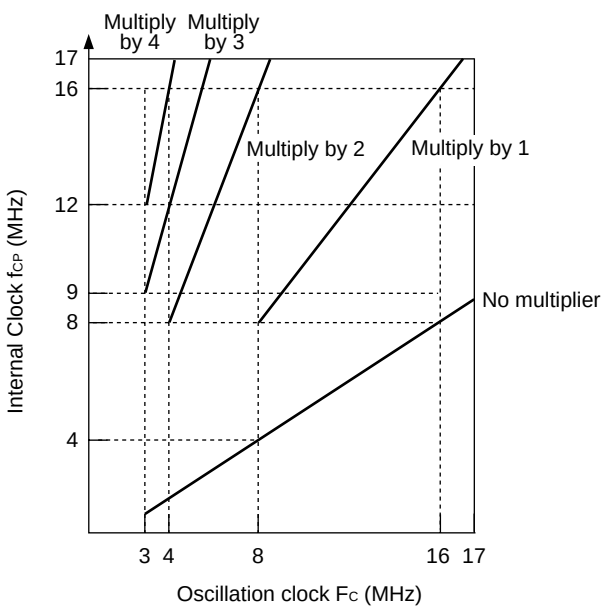
- **PLL operation assurance range**

Relationship between the internal operating clock frequency and supply voltage



: Normal operation assurance range : PLL operation assurance range

Relationship between the oscillation frequency and internal operating clock frequency



The AC characteristics are for the following measurement reference voltages.

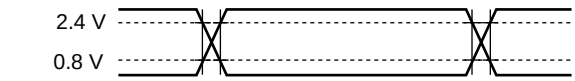
- **Input signal waveform**

Hysteresis input pins

Other than hysteresis/MD input pins

- **Output signal waveform**

Output pins

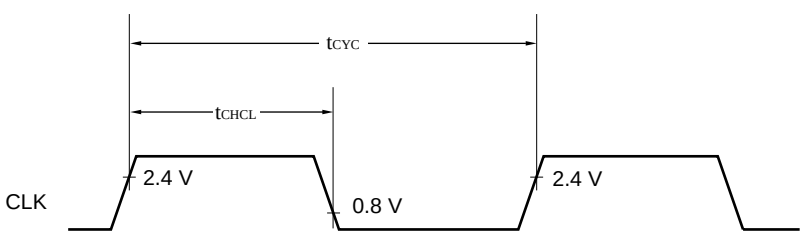


(2) Clock Output Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

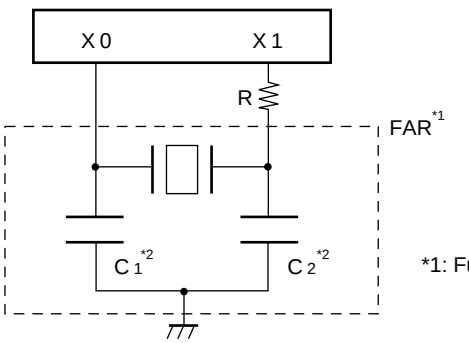
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	
CLK ↑ → CLK ↓	t_{CHCL}			$t_{CP}/2 - 20$	$t_{CP}/2 + 20$	ns	

t_{CP}: See “ (1) Clock Timing.”



(3) Recommended Resonator Manufacturers

- **Sample application of piezoelectric resonator (FAR family)**



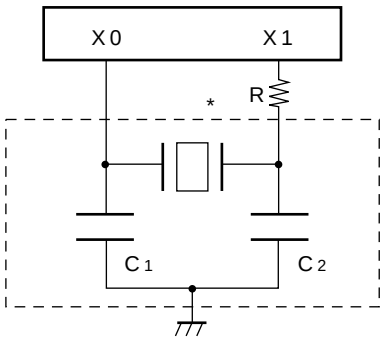
*1: Fujitsu Acoustic Resonator

FAR part number (built-in capacitor type)	Frequency (MHz)	Dumping resistor	Initial deviation of FAR frequency (T_A = +25°C)	Temperature characteristics of FAR frequency (T_A = –20°C to +60°C)	Loading capacitors*2
FAR-C4CC-02000-L20	2.00	1 kΩ	±0.5%	±0.5%	Built-in
FAR-C4CA-04000-M01	4.00	—	±0.5%	±0.5%	
FAR-C4CB-08000-M02	8.00	—	±0.5%	±0.5%	
FAR-C4CB-10000-M02	10.00	—	±0.5%	±0.5%	
FAR-C4CB-16000-M02	16.00	—	±0.5%	±0.5%	

Inquiry: FUJITSU LIMITED

MB90640A Series

- **Sample application of ceramic resonator**



Resonator manufacturer*	Resonator	Frequency (MHz)	C_1 (pF)	C_2 (pF)	R
Kyocera Corporation	KBR-2.0MS	2.00	150	150	Not required
	PBRC2.00A		150	150	Not required
	KBR-4.0MSA	4.00	33	33	680 Ω
	KBR-4.0MKS		Built-in	Built-in	680 Ω
	PBRC4.00A		33	33	680 Ω
	PBRC4.00B		Built-in	Built-in	680 Ω
	KBR-6.0MSA	6.00	33	33	Not required
	KBR-6.0MKS		Built-in	Built-in	Not required
	PBRC6.00A		33	33	Not required
	PBRC6.00B		Built-in	Built-in	Not required
	KBR-8.0M	8.00	33	33	560 Ω
	PBRC8.00A		33	33	Not required
	PBRC8.00B		Built-in	Built-in	Not required
	KBR-10.0M	10.00	33	33	330 Ω
	PBRC10.00B		Built-in	Built-in	680 Ω
	KBR-12.0M	12.00	33	33	330 Ω
	PBRC12.00B		Built-in	Built-in	680 Ω

(Continued)

(Continued)

Resonator manufacturer	Resonator	Frequency (MHz)	C_1 (pF)	C_2 (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CST2.00MG040		Built-in	Built-in	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CST4.00MGW040		Built-in	Built-in	Not required
	CSA6.00MG	6.00	30	30	Not required
	CST6.00MGW		Built-in	Built-in	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CST8.00MTW		Built-in	Built-in	Not required
	CSA10.00MTZ	10.00	30	30	Not required
	CST10.00MTW		Built-in	Built-in	Not required
	CSA12.00MTZ	12.00	30	30	Not required
	CST12.00MTW		Built-in	Built-in	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CST16.00MXW0C3		Built-in	Built-in	Not required
	CSA20.00MXZ040	20.00	10	10	Not required
	CSA24.00MXZ040	24.00	5	5	Not required
	CSA32.00MXZ040	32.00	5	5	Not required

Inquiry: Kyocera Corporation

- AVX Corporation
  North American Sales Headquarters: TEL 1-803-448-9411
- AVX Limited
  European Sales Headquarters: TEL 44-1252-770000
- AVX/Kyocera H.K. Ltd.
  Asian Sales Headquarters: TEL 852-363-3303

Murata Mfg. Co., Ltd.

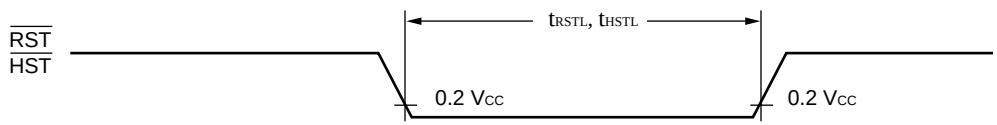
- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233

(4) Reset and Hardware Standby Inputs

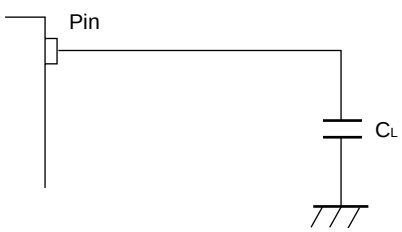
(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$	—	16 t_{CP}	—	ns	

t_{CP}: See “ (1) Clock Timing.”



- **Conditions for measurement of AC reference**



C_L: Load capacity during testing

For CLK and ALE, C_L = 30 pF
For address and data buses (AD15 to AD00), $\overline{RD}$ and $\overline{WR}$, C_L = 80 pF

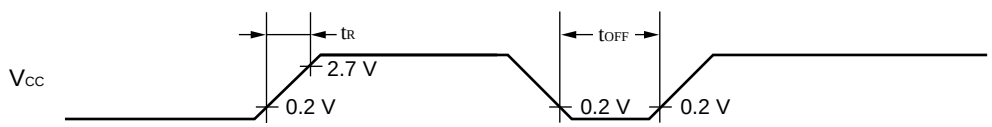
(5) Power on Supply Specifications (Power-on Reset)

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

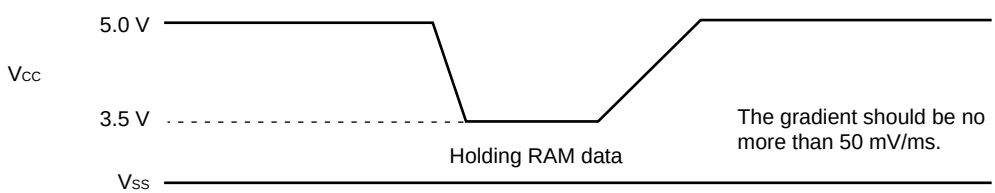
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Power supply rise time	t_R	V_{CC}	—	0.05	30	ms	
Power supply cut-off time	t_{OFF}	V_{CC}	—	50	—	ms	For repetition of the operation

* : V_{CC} should be lower than 0.2 V before power supply rise.

Notes: • The above values are the values required for a power-on reset.
• When $\overline{HST}$ = “L”, this standard must be followed to turn on power supply for power-on reset whether or not necessary.
• The device has built-in registers which are initialized only by power-on reset. For possible initialization of these registers, turn on power supply according to this standard.



Abrupt changes in the power supply voltage may cause a power-on reset.
When changing the power supply voltage during operation, the change should be as smooth as possible, as shown in the following figure.

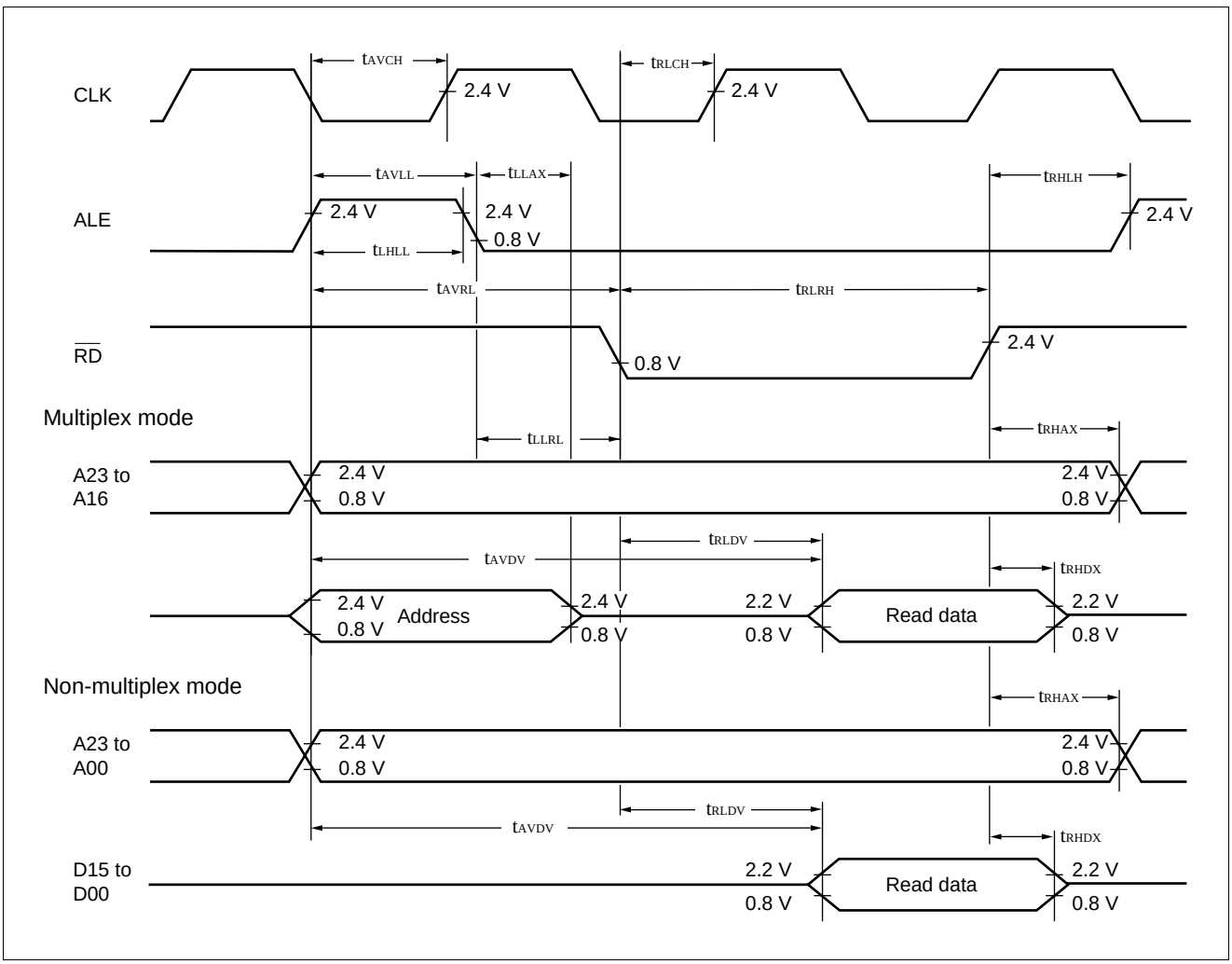


(6) Bus Timing (Read)

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$	—	ns	
Valid address → ALE ↓ time	t_{AVLL}	Address	—	$t_{CP}/2 - 20$	—	ns	
ALE ↓ → address valid time	t_{LLAX}	Address	—	$t_{CP}/2 - 15$	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	Address	—	$t_{CP} - 15$	—	ns	
Valid address → valid data input	t_{AVDV}	Address/ data	—	—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	$3\ t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → valid data input	t_{RLDV}	Data	—	—	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	Data	—	0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE	—	$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ → address valid time	t_{RHAX}	Address, $\overline{RD}$	—	$t_{CP}/2 - 10$	—	ns	
Valid address → CLK ↑ time	t_{AVCH}	Address, CLK	—	$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK	—	$t_{CP}/2 - 20$	—	ns	
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$	—	$t_{CP}/2 - 15$	—	ns	

t_{CP}: See “ (1) Clock Timing.”

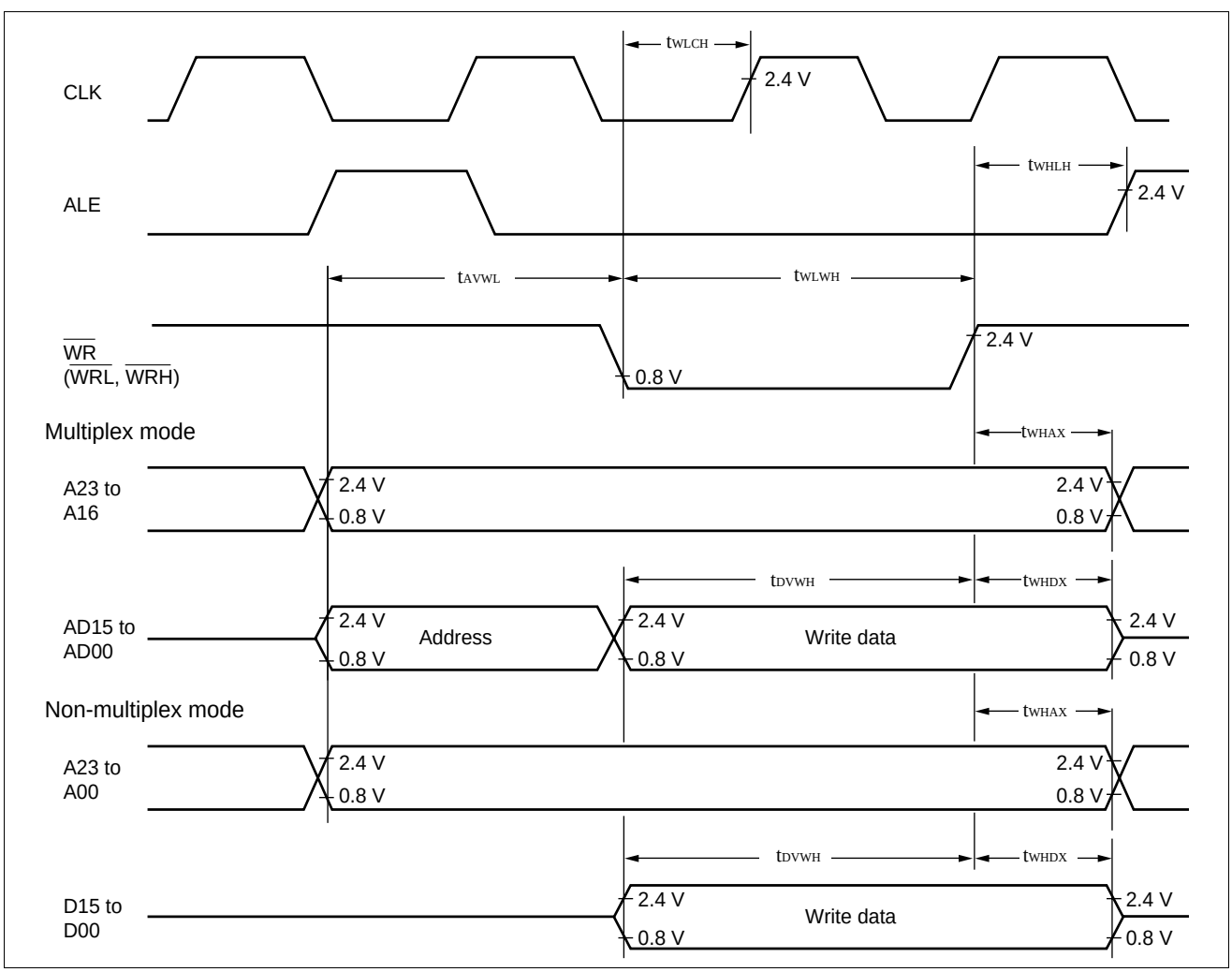

CLK
tAVCH
2.4 V
tRLCH
2.4 V
ALE
tAVLL
tLLAX
2.4 V
2.4 V
0.8 V
tLHLL
tRHLH
2.4 V
tAVRL
tRLRH
RD
0.8 V
2.4 V
Multiplex mode
tLLRL
tRHAX
A23 to A16
2.4 V
0.8 V
2.4 V
0.8 V
tRLDV
tAVDV
tRHDX
2.4 V
0.8 V
Address
2.4 V
0.8 V
2.2 V
0.8 V
Read data
2.2 V
0.8 V
Non-multiplex mode
tRHAX
A23 to A00
2.4 V
0.8 V
2.4 V
0.8 V
tRLDV
tAVDV
tRHDX
D15 to D00
2.2 V
0.8 V
Read data
2.2 V
0.8 V

(7) Bus Timing (Write)

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	Address	—	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 t_{CP}/2 – 20	—	ns	
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	Data	—	3 t_{CP}/2 – 20	—	ns	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	Data	—	20	—	ns	Multiplex mode
				30	—	ns	Non-multiplex mode
$\overline{WR}$ ↑ → address valid time	t_{WHAX}	Address	—	t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WRL}$, $\overline{WRH}$, ALE		t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WRL}$, $\overline{WRH}$, CLK		t_{CP}/2 – 20	—	ns	

t_{CP}: See “ (1) Clock Timing.”

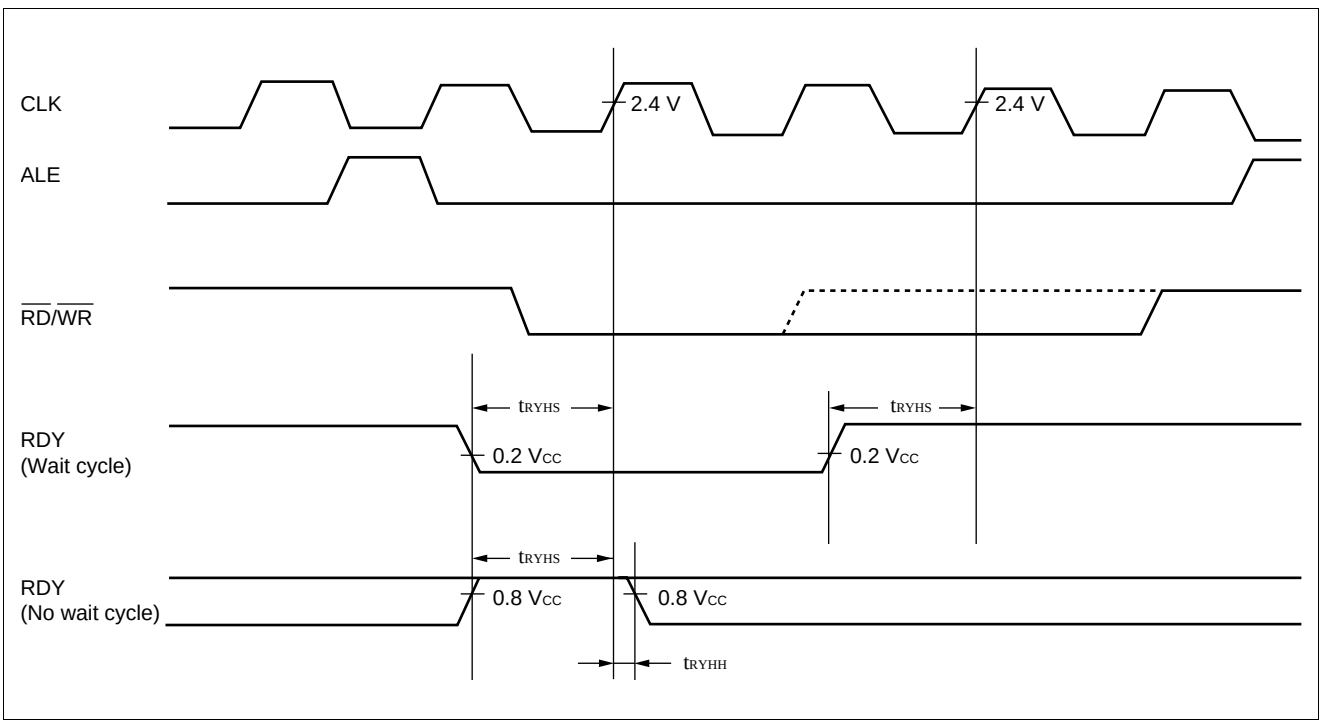


(8) Ready Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	V_{CC} = 5.0 V ±10%	45	—	ns	
RDY hold time	t_{RYHH}		—	0	—	ns	

Note: Use the auto-ready function if the setup time at fall of the RDY is too short.



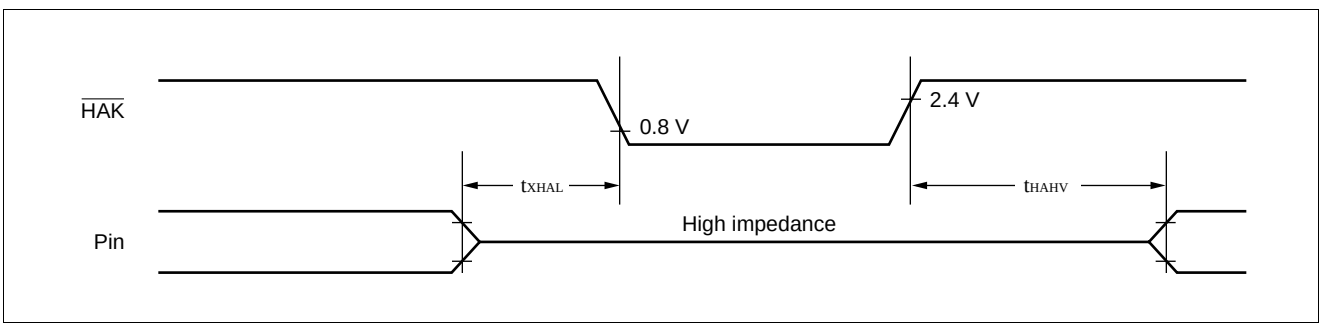
(9) Hold Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↑ → pin valid time	t_{HAHV}	$\overline{HAK}$	—	t_{CP}	2 t_{CP}	ns	

t_{CP}: See “ (1) Clock Timing.”

Note: After reading HRQ, more than one cycle is required before changing $\overline{HAK}$.



(10) I/O Extended Serial Timing

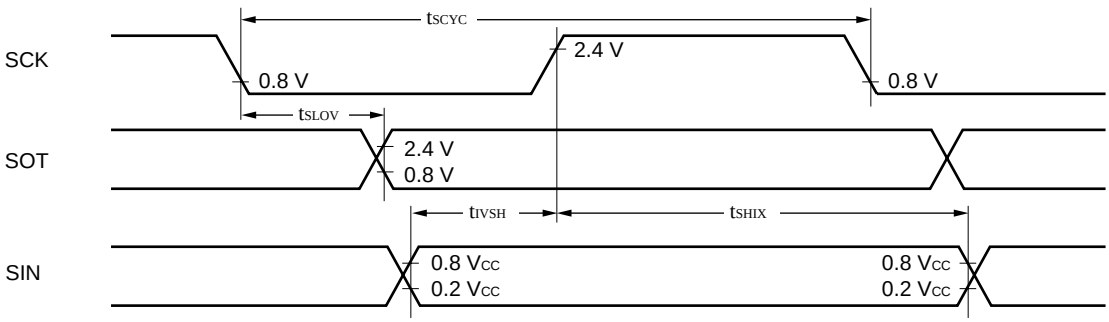
(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	C_L = 80 pF + 1 TTL for the internal shift clock mode output pin.	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	C_L = 80 pF + 1 TTL for the external shift clock mode output pin.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	

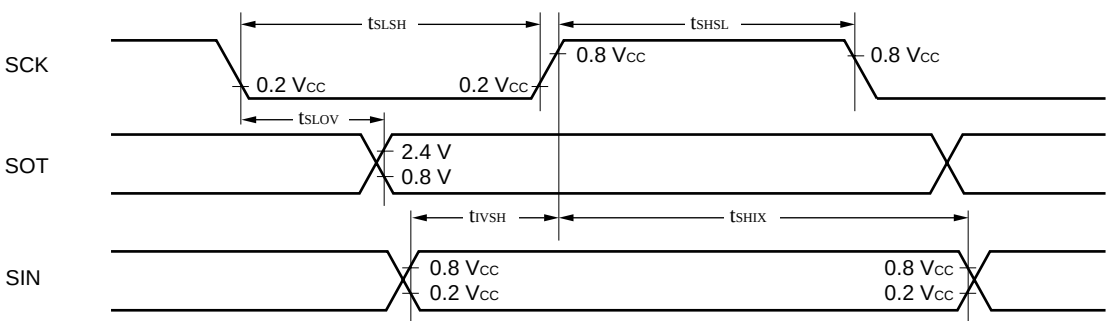
Notes: • These are the AC characteristics for CLK synchronous mode.
• C_L is the load capacitance connected to the pin at testing.
• t_{CP} is the machine cycle period (unit: ns).
• The values in the upper table are targets.

MB90640A Series

- **Internal shift clock mode**



- **External shift clock mode**

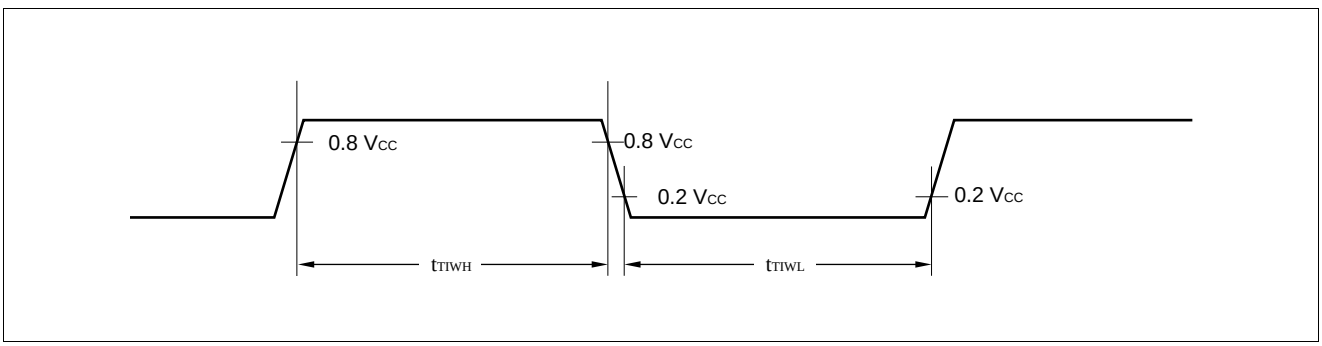


(11) Timer Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	TIM0 to TIM4	—	4 t_{CP}	—	ns	

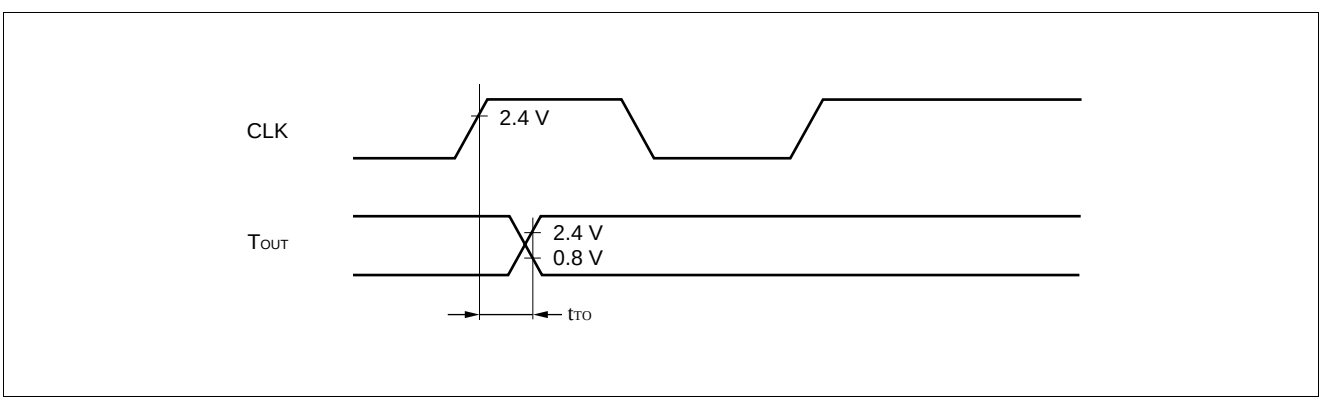
t_{CP}: See “ (1) Clock Timing.”



(12) Timer Output Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T_{OUT} change timing	t_{TO}	TIM0 to TIM4	—	30	—	ns	

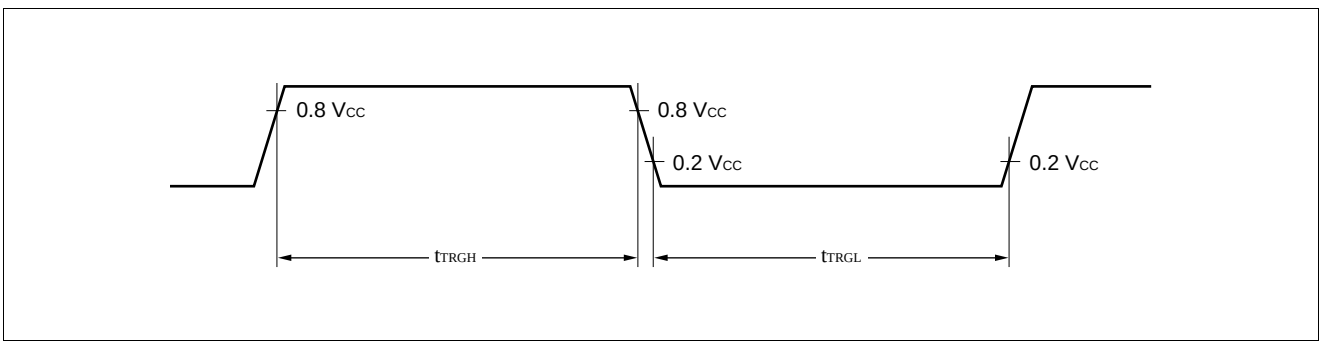


(13) Trigger Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGL}	INT0 to INT7	—	5 t_{CP}	—	ns	

t_{CP}: See “ (1) Clock Timing.”

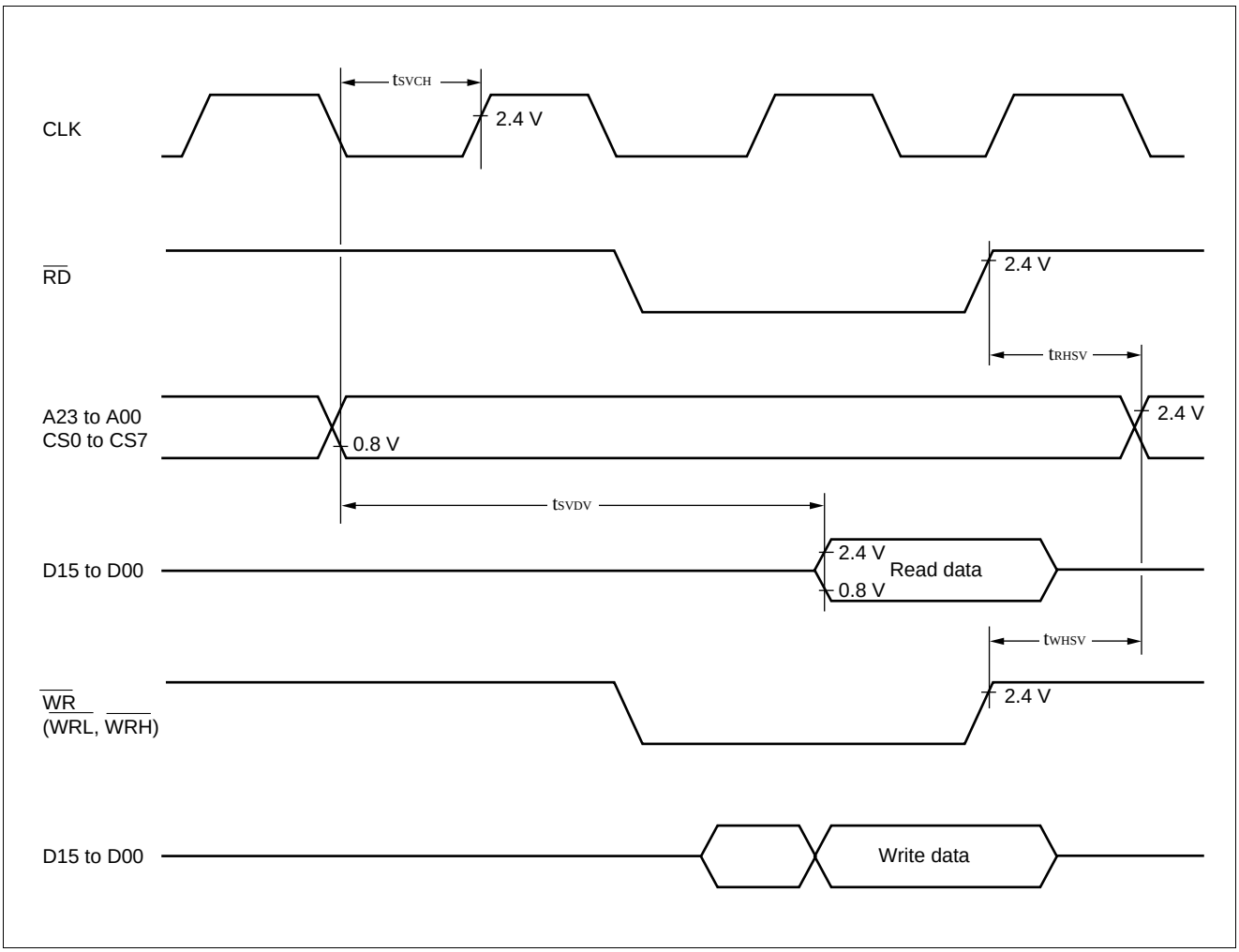


(14) Chip Select Output Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Chip select enabled → Valid data input time	t_{SVDV}	CS0 to CS7 D15 to D00	—	—	5 t_{CP}/2 – 60	ns	
$\overline{RD}$ ↑ → Chip select enabled time	t_{RHSV}	CS0 to CS7 $\overline{RD}$	—	t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ → Chip select enabled time	t_{WHSV}	CS0 to CS7 $\overline{WR}$	—	t_{CP}/2 – 10	—	ns	
Enabled chip select → CLK ↑ time	t_{SVCH}	CS0 to CS7 CLK	—	t_{CP}/2 – 20	—	ns	

t_{CP}: See “ (1) Clock Timing.”

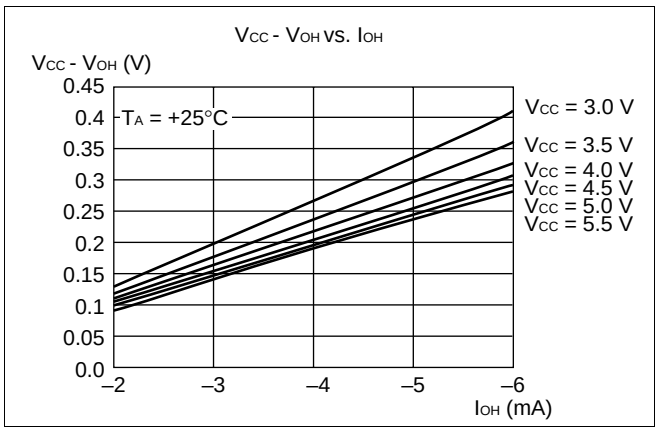

CLK
tSVCH
2.4 V
RD
2.4 V
tRHSV
A23 to A00
CS0 to CS7
0.8 V
2.4 V
tSVDV
D15 to D00
2.4 V
Read data
0.8 V
tWHSV
WR
(WRL, WRH)
2.4 V
D15 to D00
Write data

MB90640A Series

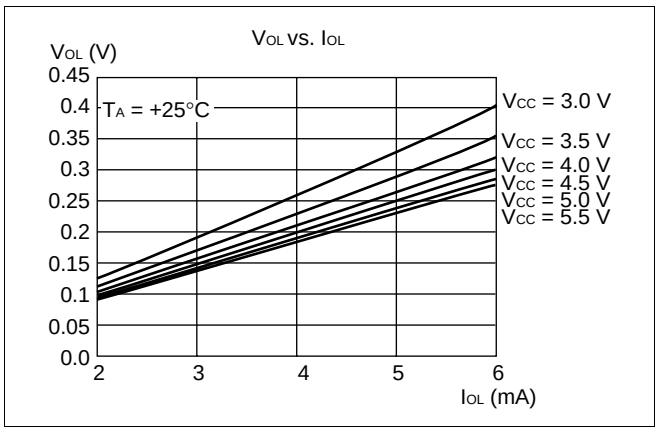
■ EXAMPLES CHARACTERISTICS

1. MB90641A

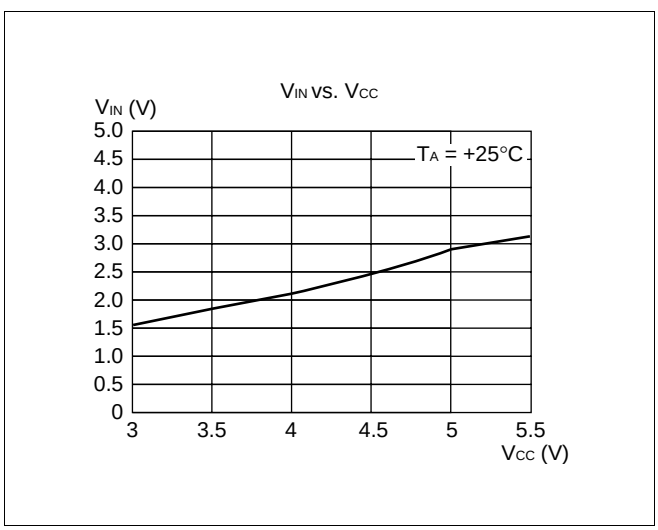
(1) “H” Level Output Voltage



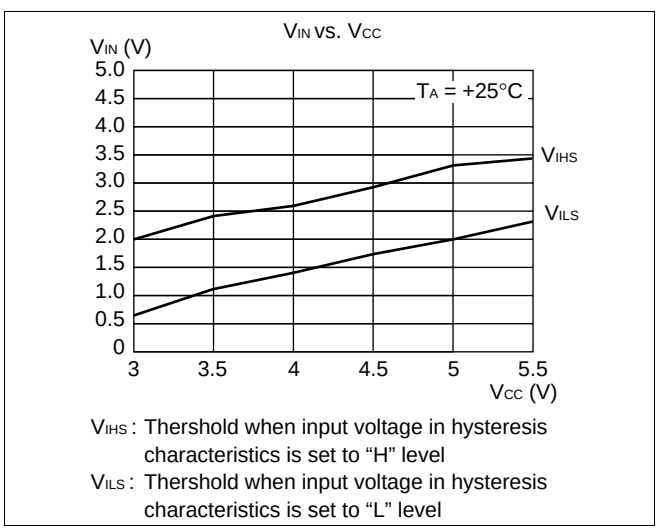
(2) “L” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



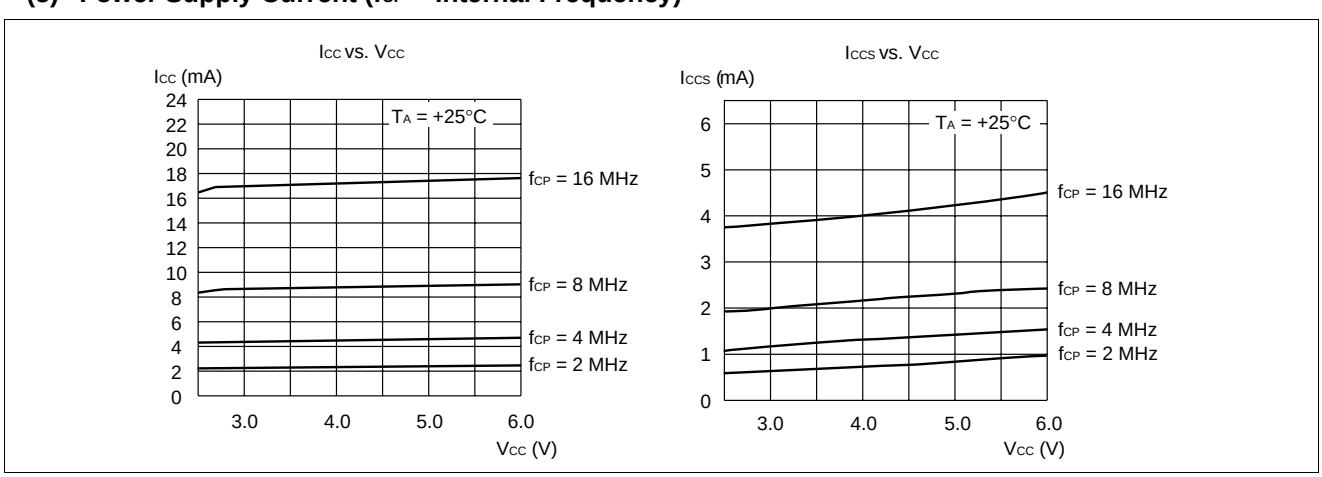
(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)



V_{IHS} : Thershold when input voltage in hysteresis characteristics is set to “H” level

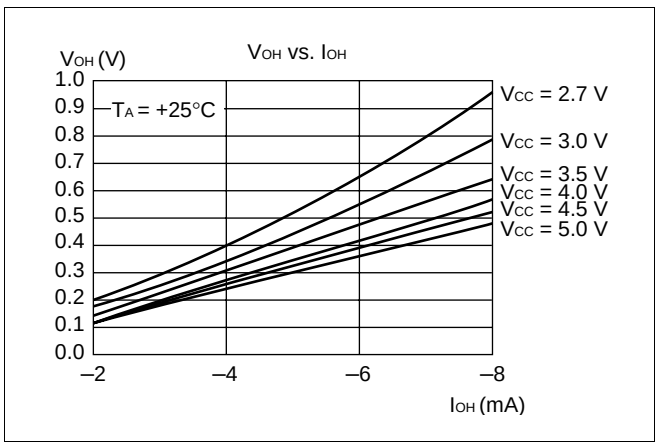
V_{ILS} : Thershold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (f_{CP} = Internal Frequency)

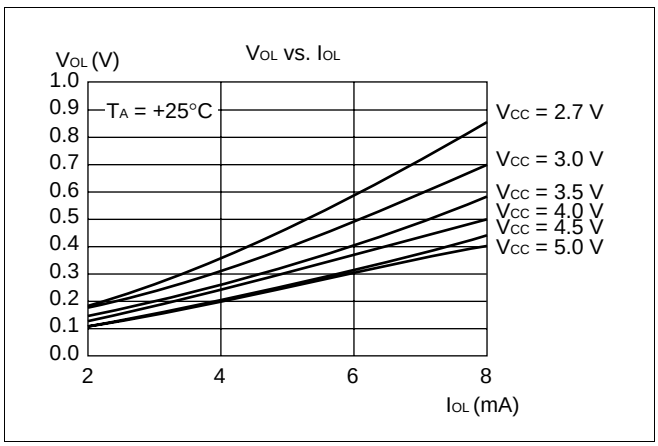


2. MB90P641A

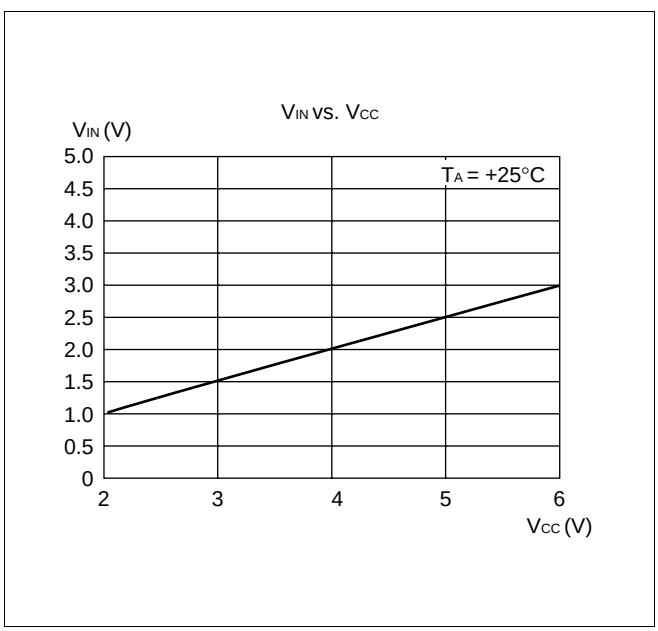
(1) “H” Level Output Voltage



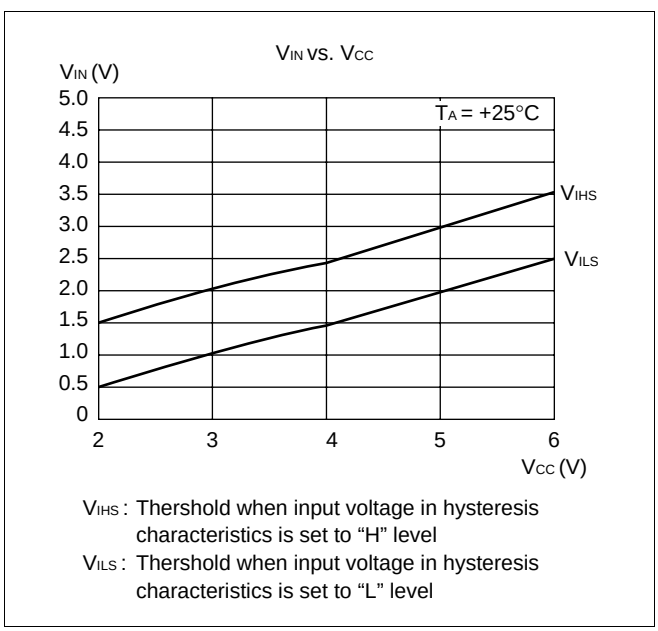
(2) “L” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



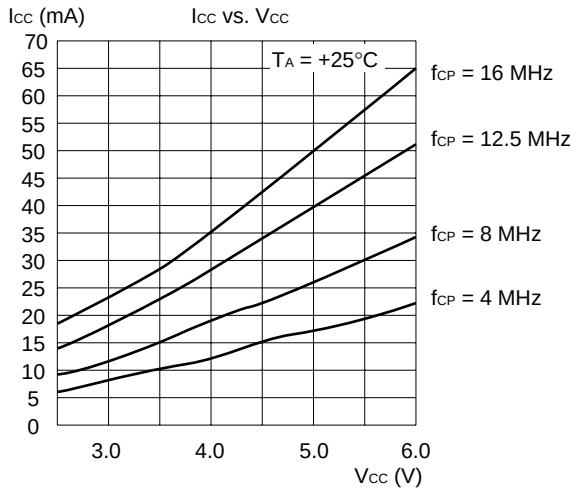
(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

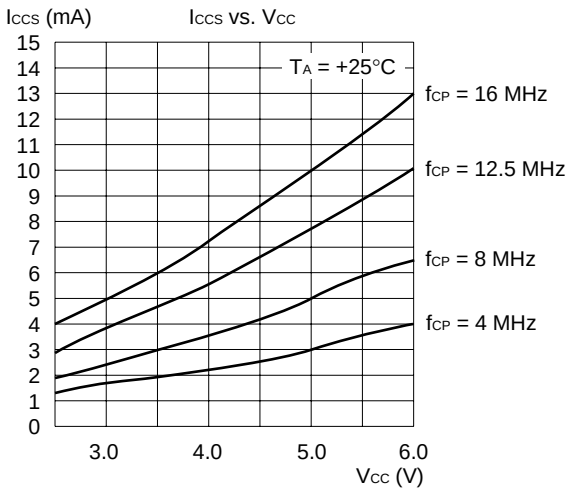


V_{IHS} : Thershold when input voltage in hysteresis characteristics is set to “H” level

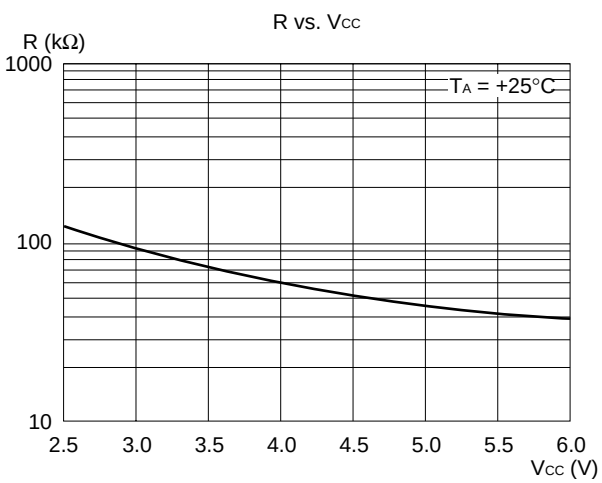
V_{ILS} : Thershold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (f_{CP} = internal frequency)





(6) Pull-up Resistance



■ INSTRUCTIONS (340 INSTRUCTIONS)

Table 1 Explanation of Items in Tables of Instructions

Item	Meaning
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler. Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction.
#	Indicates the number of bytes.
~	Indicates the number of cycles. m : When branching n : When not branching See Table 4 for details about meanings of other letters in items.
RG	Indicates the number of accesses to the register during execution of the instruction. It is used calculate a correction value for intermittent operation of CPU.
B	Indicates the correction value for calculating the number of actual cycles during execution of the instruction. (Table 5) The number of actual cycles during execution of the instruction is the correction value summed with the value in the “~” column.
Operation	Indicates the operation of instruction.
LH	Indicates special operations involving the upper 8 bits of the lower 16 bits of the accumulator. Z : Transfers “0”. X : Extends with a sign before transferring. – : Transfers nothing.
AH	Indicates special operations involving the upper 16 bits in the accumulator. * : Transfers from AL to AH. – : No transfer. Z : Transfers 00_H to AH. X : Transfers 00_H or FF_H to AH by signing and extending AL.
I	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). * : Changes due to execution of instruction. – : No change. S : Set by execution of instruction. R : Reset by execution of instruction.
S	
T	
N	
Z	
V	
C	
RMW	Indicates whether the instruction is a read-modify-write instruction. (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.) * : Instruction is a read-modify-write instruction. – : Instruction is not a read-modify-write instruction. Note: A read-modify-write instruction cannot be used on addresses that have different meanings depending on whether they are read or written.

Table 2 Explanation of Symbols in Tables of Instructions

Symbol	Meaning
A	32-bit accumulator The bit length varies according to the instruction. Byte : Lower 8 bits of AL Word : 16 bits of AL Long : 32 bits of AL:AH
AH AL	Upper 16 bits of A Lower 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir	Compact direct addressing
addr16 addr24 ad24 0 to 15 ad24 16 to 23	Direct addressing Physical direct addressing Bit 0 to bit 15 of addr24 Bit 16 to bit 23 of addr24
io	I/O area (000000_H to $0000FF_H$)
imm4 imm8 imm16 imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
( )b	Bit address

(Continued)

(Continued)

Symbol	Meaning
rel	Branch specification relative to PC
ear eam	Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

Table 3 Effective Address Fields

Code	Notation	Address format	Number of bytes in address extension *
00 01 02 03 04 05 06 07	R0 RW0 RL0 R1 RW1 (RL0) R2 RW2 RL1 R3 RW3 (RL1) R4 RW4 RL2 R5 RW5 (RL2) R6 RW6 RL3 R7 RW7 (RL3)	Register direct “ea” corresponds to byte, word, and long-word types, starting from the left	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3	Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +	Register indirect with post-increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8	Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16	Register indirect with 16-bit displacement	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

Note: The number of bytes in the address extension is indicated by the “+” symbol in the “#” (number of bytes) column in the tables of instructions.

Table 4 Number of Execution Cycles for Each Type of Addressing

Code	Operand	(a) Number of execution cycles for each type of addressing	Number of register accesses for each type of addressing
00 to 07	Ri RWi RLi	Listed in tables of instructions	Listed in tables of instructions
08 to 0B	@RWj	2	1
0C to 0F	@RWj +	4	2
10 to 17	@RWi + disp8	2	1
18 to 1B	@RWj + disp16	2	1
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	4 4 2 1	2 2 0 0

Note: “(a)” is used in the “~” (number of states) column and column B (correction value) in the tables of instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b) byte		(c) word		(d) long	
	Number of cycles	Number of access	Number of cycles	Number of access	Number of cycles	Number of access
Internal register	+0	1	+0	1	+0	2
Internal memory even address Internal memory odd address	+0 +0	1 1	+0 +2	1 2	+0 +4	2 4
Even address on external data bus (16 bits) Odd address on external data bus (16 bits)	+1 +1	1 1	+1 +4	1 2	+2 +8	2 4
External data bus (8 bits)	+1	1	+4	2	+8	4

Notes: • “(b)”, “(c)”, and “(d)” are used in the “~” (number of states) column and column B (correction value) in the tables of instructions.
• When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

Table 6 Correction Values for Number of Cycles Used to Calculate Number of Program Fetch Cycles

Instruction	Byte boundary	Word boundary
Internal memory	—	+2
External data bus (16 bits)	—	+3
External data bus (8 bits)	+3	—

Notes: • When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.
• Because instruction execution is not slowed down by all program fetches in actuality, these correction values should be used for “worst case” calculations.

Table 7 Transfer Instructions (Byte) [41 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOV	A, dir	2	3	0	(b)	byte (A) ← (dir)	Z	*	–	–	–	*	*	–	–	–
MOV	A, addr16	3	4	0	(b)	byte (A) ← (addr16)	Z	*	–	–	–	*	*	–	–	–
MOV	A, Ri	1	2	1	0	byte (A) ← (Ri)	Z	*	–	–	–	*	*	–	–	–
MOV	A, ear	2	2	1	0	byte (A) ← (ear)	Z	*	–	–	–	*	*	–	–	–
MOV	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	Z	*	–	–	–	*	*	–	–	–
MOV	A, io	2	3	0	(b)	byte (A) ← (io)	Z	*	–	–	–	*	*	–	–	–
MOV	A, #imm8	2	2	0	0	byte (A) ← imm8	Z	*	–	–	–	*	*	–	–	–
MOV	A, @A	2	3	0	(b)	byte (A) ← ((A))	Z	–	–	–	–	*	*	–	–	–
MOV	A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	Z	*	–	–	–	*	*	–	–	–
MOVN	A, #imm4	1	1	0	0	byte (A) ← imm4	Z	*	–	–	–	R	*	–	–	–
MOVX	A, dir	2	3	0	(b)	byte (A) ← (dir)	X	*	–	–	–	*	*	–	–	–
MOVX	A, addr16	3	4	0	(b)	byte (A) ← (addr16)	X	*	–	–	–	*	*	–	–	–
MOVX	A, Ri	2	2	1	0	byte (A) ← (Ri)	X	*	–	–	–	*	*	–	–	–
MOVX	A, ear	2	2	1	0	byte (A) ← (ear)	X	*	–	–	–	*	*	–	–	–
MOVX	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	X	*	–	–	–	*	*	–	–	–
MOVX	A, io	2	3	0	(b)	byte (A) ← (io)	X	*	–	–	–	*	*	–	–	–
MOVX	A, #imm8	2	2	0	0	byte (A) ← imm8	X	*	–	–	–	*	*	–	–	–
MOVX	A, @A	2	3	0	(b)	byte (A) ← ((A))	X	–	–	–	–	*	*	–	–	–
MOVX	A,@RWi+disp8	2	5	1	(b)	byte (A) ← ((RWi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOVX	A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOV	dir, A	2	3	0	(b)	byte (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	addr16, A	3	4	0	(b)	byte (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, A	1	2	1	0	byte (Ri) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	ear, A	2	2	1	0	byte (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	eam, A	2+	3+ (a)	0	(b)	byte (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	io, A	2	3	0	(b)	byte (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	@RLi+disp8, A	3	10	2	(b)	byte ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, ear	2	3	2	0	byte (Ri) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, eam	2+	4+ (a)	1	(b)	byte (Ri) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOV	ear, Ri	2	4	2	0	byte (ear) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV	eam, Ri	2+	5+ (a)	1	(b)	byte (eam) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, #imm8	2	2	1	0	byte (Ri) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV	io, #imm8	3	5	0	(b)	byte (io) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	dir, #imm8	3	5	0	(b)	byte (dir) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	ear, #imm8	3	2	1	0	byte (ear) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV	eam, #imm8	3+	4+ (a)	0	(b)	byte (eam) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV /MOV	@AL, AH @A, T	2	3	0	(b)	byte ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCH	A, ear	2	4	2	0	byte (A) ↔ (ear)	Z	–	–	–	–	–	–	–	–	–
XCH	A, eam	2+	5+ (a)	0	2× (b)	byte (A) ↔ (eam)	Z	–	–	–	–	–	–	–	–	–
XCH	Ri, ear	2	7	4	0	byte (Ri) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCH	Ri, eam	2+	9+ (a)	2	2× (b)	byte (Ri) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 8 Transfer Instructions (Word/Long Word) [38 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	3	0	(c)	word (A) ← (dir)	–	*	–	–	–	*	*	–	–	–
MOVW A, addr16	3	4	0	(c)	word (A) ← (addr16)	–	*	–	–	–	*	*	–	–	–
MOVW A, SP	1	1	0	0	word (A) ← (SP)	–	*	–	–	–	*	*	–	–	–
MOVW A, RWi	1	2	1	0	word (A) ← (RWi)	–	*	–	–	–	*	*	–	–	–
MOVW A, ear	2	2	1	0	word (A) ← (ear)	–	*	–	–	–	*	*	–	–	–
MOVW A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	*	–	–	–	*	*	–	–	–
MOVW A, io	2	3	0	(c)	word (A) ← (io)	–	*	–	–	–	*	*	–	–	–
MOVW A, @A	2	3	0	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW A, #imm16	3	2	0	0	word (A) ← imm16	–	*	–	–	–	*	*	–	–	–
MOVW A, @RWi+disp8	2	5	1	(c)	word (A) ← ((RWi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @RLi+disp8	3	10	2	(c)	word (A) ← ((RLi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW dir, A	2	3	0	(c)	word (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW addr16, A	3	4	0	(c)	word (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW SP, A	1	1	0	0	word (SP) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, A	1	2	1	0	word (RWi) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW ear, A	2	2	1	0	word (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW eam, A	2+	3+ (a)	0	(c)	word (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW io, A	2	3	0	(c)	word (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RWi+disp8, A	2	5	1	(c)	word ((RWi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RLi+disp8, A	3	10	2	(c)	word ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, ear	2	3	2	(0)	word (RWi) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, eam	2+	4+ (a)	1	(c)	word (RWi) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVW ear, RWi	2	4	2	0	word (ear) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW eam, RWi	2+	5+ (a)	1	(c)	word (eam) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, #imm16	3	2	1	0	word (RWi) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW io, #imm16	4	5	0	(c)	word (io) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW ear, #imm16	4	2	1	0	word (ear) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW eam, #imm16	4+	4+ (a)	0	(c)	word (eam) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW AL, AH /MOVW @A, T	2	3	0	(c)	word ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCHW A, ear	2	4	2	0	word (A) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW A, eam	2+	5+ (a)	0	2× (c)	word (A) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, ear	2	7	4	0	word (RWi) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, eam	2+	9+ (a)	2	2× (c)	word (RWi) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
MOVL A, ear	2	4	2	0	long (A) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVL A, eam	2+	5+ (a)	0	(d)	long (A) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVL A, #imm32	5	3	0	0	long (A) ← imm32	–	–	–	–	–	*	*	–	–	–
MOVL ear, A	2	4	2	0	long (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL eam, A	2+	5+ (a)	0	(d)	long (eam) ← (A)	–	–	–	–	–	*	*	–	–	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD	A,#imm8	2	2	0	0	byte (A) ← (A) +imm8	Z	–	–	–	–	*	*	*	*	–
ADD	A, dir	2	5	0	(b)	byte (A) ← (A) +(dir)	Z	–	–	–	–	*	*	*	*	–
ADD	A, ear	2	3	1	0	byte (A) ← (A) +(ear)	Z	–	–	–	–	*	*	*	*	–
ADD	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) +(eam)	Z	–	–	–	–	*	*	*	*	–
ADD	ear, A	2	3	2	0	byte (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADD	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) + (A)	Z	–	–	–	–	*	*	*	*	*
ADDC	A	1	2	0	0	byte (A) ← (AH) + (AL) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC	A, ear	2	3	1	0	byte (A) ← (A) + (ear) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) + (eam) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDDC	A	1	3	0	0	byte (A) ← (AH) + (AL) + (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
SUB	A, #imm8	2	2	0	0	byte (A) ← (A) –imm8	Z	–	–	–	–	*	*	*	*	–
SUB	A, dir	2	5	0	(b)	byte (A) ← (A) – (dir)	Z	–	–	–	–	*	*	*	*	–
SUB	A, ear	2	3	1	0	byte (A) ← (A) – (ear)	Z	–	–	–	–	*	*	*	*	–
SUB	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam)	Z	–	–	–	–	*	*	*	*	–
SUB	ear, A	2	3	2	0	byte (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUB	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBC	A	1	2	0	0	byte (A) ← (AH) – (AL) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC	A, ear	2	3	1	0	byte (A) ← (A) – (ear) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBDC	A	1	3	0	0	byte (A) ← (AH) – (AL) – (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
ADDW	A	1	2	0	0	word (A) ← (AH) + (AL)	–	–	–	–	–	*	*	*	*	–
ADDW	A, ear	2	3	1	0	word (A) ← (A) +(ear)	–	–	–	–	–	*	*	*	*	–
ADDW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) +(eam)	–	–	–	–	–	*	*	*	*	–
ADDW	A, #imm16	3	2	0	0	word (A) ← (A) +imm16	–	–	–	–	–	*	*	*	*	–
ADDW	ear, A	2	3	2	0	word (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADDW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) + (A)	–	–	–	–	–	*	*	*	*	*
ADDCW	A, ear	2	3	1	0	word (A) ← (A) + (ear) + (C)	–	–	–	–	–	*	*	*	*	–
ADDCW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) + (eam) + (C)	–	–	–	–	–	*	*	*	*	–
SUBW	A	1	2	0	0	word (A) ← (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
SUBW	A, ear	2	3	1	0	word (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBW	A, #imm16	3	2	0	0	word (A) ← (A) –imm16	–	–	–	–	–	*	*	*	*	–
SUBW	ear, A	2	3	2	0	word (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUBW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBCW	A, ear	2	3	1	0	word (A) ← (A) – (ear) – (C)	–	–	–	–	–	*	*	*	*	–
SUBCW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam) – (C)	–	–	–	–	–	*	*	*	*	–
ADDL	A, ear	2	6	2	0	long (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDL	A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDL	A, #imm32	5	4	0	0	long (A) ← (A) +imm32	–	–	–	–	–	*	*	*	*	–
SUBL	A, ear	2	6	2	0	long (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBL	A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBL	A, #imm32	5	4	0	0	long (A) ← (A) –imm32	–	–	–	–	–	*	*	*	*	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC	ear	2	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC	ear	2	3	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DEC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW	ear	2	3	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW	ear	2	3	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL	ear	2	7	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL	ear	2	7	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP	A	1	1	0	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP	A, ear	2	2	1	0	byte (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMP	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMP	A, #imm8	2	2	0	0	byte (A) ← imm8	–	–	–	–	–	*	*	*	*	–
CMPW	A	1	1	0	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW	A, ear	2	2	1	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPW	A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPW	A, #imm16	3	2	0	0	word (A) ← imm16	–	–	–	–	–	*	*	*	*	–
CMPL	A, ear	2	6	2	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPL	A, eam	2+	7+ (a)	0	(d)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPL	A, #imm32	5	3	0	0	word (A) ← imm32	–	–	–	–	–	*	*	*	*	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 12 Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIVU	A	1	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	–	–	–	–	–	–	–	*	*	–
DIVU	A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	–	–	–	–	–	–	–	*	*	–
DIVU	A, eam	2+	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU	A	1	*8	0	0	byte (AH) *byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, eam	2+	*10	0	(b)	byte (A) *byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A	1	*11	0	0	word (AH) *word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, eam	2+	*13	0	(c)	word (A) *word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

*1: 3 when the result is zero, 7 when an overflow occurs, and 15 normally.
*2: 4 when the result is zero, 8 when an overflow occurs, and 16 normally.
*3: 6 + (a) when the result is zero, 9 + (a) when an overflow occurs, and 19 + (a) normally.
*4: 4 when the result is zero, 7 when an overflow occurs, and 22 normally.
*5: 6 + (a) when the result is zero, 8 + (a) when an overflow occurs, and 26 + (a) normally.
*6: (b) when the result is zero or when an overflow occurs, and 2 × (b) normally.
*7: (c) when the result is zero or when an overflow occurs, and 2 × (c) normally.
*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not zero.
*9: 4 when byte (ear) is zero, and 8 when byte (ear) is not zero.
*10: 5 + (a) when byte (eam) is zero, and 9 + (a) when byte (eam) is not 0.
*11: 3 when word (AH) is zero, and 11 when word (AH) is not zero.
*12: 4 when word (ear) is zero, and 12 when word (ear) is not zero.
*13: 5 + (a) when word (eam) is zero, and 13 + (a) when word (eam) is not zero.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 13 Logical 1 Instructions (Byte/Word) [39 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
AND	A, #imm8	2	2	0	0	byte (A) ← (A) and imm8	–	–	–	–	–	*	*	R	–	–
AND	A, ear	2	3	1	0	byte (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
AND	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
AND	ear, A	2	3	2	0	byte (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
AND	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
OR	A, #imm8	2	2	0	0	byte (A) ← (A) or imm8	–	–	–	–	–	*	*	R	–	–
OR	A, ear	2	3	1	0	byte (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
OR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
OR	ear, A	2	3	2	0	byte (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
OR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XOR	A, #imm8	2	2	0	0	byte (A) ← (A) xor imm8	–	–	–	–	–	*	*	R	–	–
XOR	A, ear	2	3	1	0	byte (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XOR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XOR	ear, A	2	3	2	0	byte (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XOR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOT	A	1	2	0	0	byte (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOT	ear	2	3	2	0	byte (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOT	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*
ANDW	A	1	2	0	0	word (A) ← (AH) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	A, #imm16	3	2	0	0	word (A) ← (A) and imm16	–	–	–	–	–	*	*	R	–	–
ANDW	A, ear	2	3	1	0	word (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ANDW	ear, A	2	3	2	0	word (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
ORW	A	1	2	0	0	word (A) ← (AH) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	A, #imm16	3	2	0	0	word (A) ← (A) or imm16	–	–	–	–	–	*	*	R	–	–
ORW	A, ear	2	3	1	0	word (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
ORW	ear, A	2	3	2	0	word (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XORW	A	1	2	0	0	word (A) ← (AH) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	A, #imm16	3	2	0	0	word (A) ← (A) xor imm16	–	–	–	–	–	*	*	R	–	–
XORW	A, ear	2	3	1	0	word (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XORW	ear, A	2	3	2	0	word (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOTW	A	1	2	0	0	word (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOTW	ear	2	3	2	0	word (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOTW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 14 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	6	2	0	long (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ORL A, ear	2	6	2	0	long (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
XORL A, ea	2	6	2	0	long (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–

Table 15 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	0	byte (A) ← 0 – (A)	X	–	–	–	–	*	*	*	*	–
NEG ear	2	3	2	0	byte (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEG eam	2+	5+ (a)	0	2× (b)	byte (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*
NEGW A	1	2	0	0	word (A) ← 0 – (A)	–	–	–	–	–	*	*	*	*	–
NEGW ear	2	3	2	0	word (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEGW eam	2+	5+ (a)	0	2× (c)	word (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*

Table 16 Normalize Instruction (Long Word) [1 Instruction]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*1	1	0	long (A) ← Shift until first digit is “1” byte (R0) ← Current shift count	–	–	–	–	–	–	*	–	–	–

*1: 4 when the contents of the accumulator are all zeroes, 6 + (R0) in all other cases (shift count).

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 17 Shift Instructions (Byte/Word/Long Word) [18 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
RORC A	2	2	0	0	byte (A) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC A	2	2	0	0	byte (A) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC ear	2	3	2	0	byte (ear) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	*
ROLC ear	2	3	2	0	byte (ear) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	*
ASR A, R0	2	*1	1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSR A, R0	2	*1	1	0	byte (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSL A, R0	2	*1	1	0	byte (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRW A	1	2	0	0	word (A) ← Arithmetic right shift (A, 1 bit)	–	–	–	–	*	*	*	–	*	–
LSRW A/SHRW A	1	2	0	0	word (A) ← Logical right shift (A, 1 bit)	–	–	–	–	*	R	*	–	*	–
LSLW A/SHLW A	1	2	0	0	word (A) ← Logical left shift (A, 1 bit)	–	–	–	–	–	*	*	–	*	–
ASRW A, R0	2	*1	1	0	word (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRW A, R0	2	*1	1	0	word (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLW A, R0	2	*1	1	0	word (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRL A, R0	2	*2	1	0	long (A) ← Arithmetic right shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRL A, R0	2	*2	1	0	long (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLL A, R0	2	*2	1	0	long (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–

*1: 6 when R0 is 0, 5 + (R0) in all other cases.
*2: 6 when R0 is 0, 6 + (R0) in all other cases.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 18 Branch 1 Instructions [31 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
BZ/BEQ rel	2	*1	0	0	Branch when (Z) = 1	–	–	–	–	–	–	–	–	–	–
BNZ/BNE rel	2	*1	0	0	Branch when (Z) = 0	–	–	–	–	–	–	–	–	–	–
BC/BLO rel	2	*1	0	0	Branch when (C) = 1	–	–	–	–	–	–	–	–	–	–
BNC/BHS rel	2	*1	0	0	Branch when (C) = 0	–	–	–	–	–	–	–	–	–	–
BN rel	2	*1	0	0	Branch when (N) = 1	–	–	–	–	–	–	–	–	–	–
BP rel	2	*1	0	0	Branch when (N) = 0	–	–	–	–	–	–	–	–	–	–
BV rel	2	*1	0	0	Branch when (V) = 1	–	–	–	–	–	–	–	–	–	–
BNV rel	2	*1	0	0	Branch when (V) = 0	–	–	–	–	–	–	–	–	–	–
BT rel	2	*1	0	0	Branch when (T) = 1	–	–	–	–	–	–	–	–	–	–
BNT rel	2	*1	0	0	Branch when (T) = 0	–	–	–	–	–	–	–	–	–	–
BLT rel	2	*1	0	0	Branch when (V) xor (N) = 1	–	–	–	–	–	–	–	–	–	–
BGE rel	2	*1	0	0	Branch when (V) xor (N) = 0	–	–	–	–	–	–	–	–	–	–
BLE rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BGT rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BLS rel	2	*1	0	0	Branch when (C) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BHI rel	2	*1	0	0	Branch when (C) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BRA rel	2	*1	0	0	Branch unconditionally	–	–	–	–	–	–	–	–	–	–
JMP @A	1	2	0	0	word (PC) ← (A)	–	–	–	–	–	–	–	–	–	–
JMP addr16	3	3	0	0	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
JMP @ear	2	3	1	0	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
JMP @eam	2+	4+ (a)	0	(c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
JMPP @ear *3	2	5	2	0	word (PC) ← (ear), (PCB) ← (ear +2)	–	–	–	–	–	–	–	–	–	–
JMPP @eam *3	2+	6+ (a)	0	(d)	word (PC) ← (eam), (PCB) ← (eam +2)	–	–	–	–	–	–	–	–	–	–
JMPP addr24	4	4	0	0	word (PC) ← ad24 0 to 15, (PCB) ← ad24 16 to 23	–	–	–	–	–	–	–	–	–	–
CALL @ear *4	2	6	1	(c)	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
CALL @eam *4	2+	7+ (a)	0	2× (c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
CALL addr16 *5	3	6	0	(c)	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
CALLV #vct4 *5	1	7	0	2× (c)	Vector call instruction	–	–	–	–	–	–	–	–	–	–
CALLP @ear *6	2	10	2	2× (c)	word (PC) ← (ear) 0 to 15 (PCB) ← (ear) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP @eam *6	2+	11+ (a)	0	*2	word (PC) ← (eam) 0 to 15 (PCB) ← (eam) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP addr24 *7	4	10	0	2× (c)	word (PC) ← addr0 to 15, (PCB) ← addr16 to 23	–	–	–	–	–	–	–	–	–	–

*1: 4 when branching, 3 when not branching.
*2: (b) + 3 × (c)
*3: Read (word) branch address.
*4: W: Save (word) to stack; R: read (word) branch address.
*5: Save (word) to stack.
*6: W: Save (long word) to W stack; R: read (long word) R branch address.
*7: Save (long word) to stack.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 19 Branch 2 Instructions [19 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CBNE A, #imm8, rel	3	*1	0	0	Branch when byte (A) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE A, #imm16, rel	4	*1	0	0	Branch when word (A) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CBNE ear, #imm8, rel	4	*2	1	0	Branch when byte (ear) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CBNE eam, #imm8, rel*9	4+	*3	0	(b)	Branch when byte (eam) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE ear, #imm16, rel	5	*4	1	0	Branch when word (ear) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CWBNE eam, #imm16, rel*9	5+	*3	0	(c)	Branch when word (eam) ≠ imm16	–	–	–	–	–	*	*	*	*	–
DBNZ ear, rel	3	*5	2	0	Branch when byte (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DBNZ eam, rel	3+	*6	2	2× (b)	Branch when byte (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
DWBNZ ear, rel	3	*5	2	0	Branch when word (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DWBNZ eam, rel	3+	*6	2	2× (c)	Branch when word (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
INT #vct8	2	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT addr16	3	16	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INTP addr24	4	17	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT9	1	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
RETI	1	15	0	6× (c)	Return from interrupt	–	–	*	*	*	*	*	*	*	–
LINK #local8	2	6	0	(c)	At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area	–	–	–	–	–	–	–	–	–	–
UNLINK	1	5	0	(c)	At constant entry, retrieve old frame pointer from stack.	–	–	–	–	–	–	–	–	–	–
RET *7	1	4	0	(c)	Return from subroutine	–	–	–	–	–	–	–	–	–	–
RETP *8	1	6	0	(d)	Return from subroutine	–	–	–	–	–	–	–	–	–	–

*1: 5 when branching, 4 when not branching
*2: 13 when branching, 12 when not branching
*3: 7 + (a) when branching, 6 + (a) when not branching
*4: 8 when branching, 7 when not branching
*5: 7 when branching, 6 when not branching
*6: 8 + (a) when branching, 7 + (a) when not branching
*7: Retrieve (word) from stack
*8: Retrieve (long word) from stack
*9: In the CBNE/CWBNE instruction, do not use the RWj+ addressing mode.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 20 Other Control Instructions (Byte/Word/Long Word) [36 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW A	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (A)	–	–	–	–	–	–	–	–	–	–
PUSHW AH	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (AH)	–	–	–	–	–	–	–	–	–	–
PUSHW PS	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (PS)	–	–	–	–	–	–	–	–	–	–
PUSHW rlst	2	*3	*5	*4	(SP) ← (SP) –2n, ((SP)) ← (rlst)	–	–	–	–	–	–	–	–	–	–
POPW A	1	3	0	(c)	word (A) ← ((SP)), (SP) ← (SP) +2	–	*	–	–	–	–	–	–	–	–
POPW AH	1	3	0	(c)	word (AH) ← ((SP)), (SP) ← (SP) +2	–	–	–	–	–	–	–	–	–	–
POPW PS	1	4	0	(c)	word (PS) ← ((SP)), (SP) ← (SP) +2	–	–	*	*	*	*	*	*	*	–
POPW rlst	2	*2	*5	*4	(rlst) ← ((SP)), (SP) ← (SP) +2n	–	–	–	–	–	–	–	–	–	–
JCTX @A	1	14	0	6× (c)	Context switch instruction	–	–	*	*	*	*	*	*	*	–
AND CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) and imm8	–	–	*	*	*	*	*	*	*	–
OR CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) or imm8	–	–	*	*	*	*	*	*	*	–
MOV RP, #imm8	2	2	0	0	byte (RP) ←imm8	–	–	–	–	–	–	–	–	–	–
MOV ILM, #imm8	2	2	0	0	byte (ILM) ←imm8	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, ear	2	3	1	0	word (RWi) ←ear	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, eam	2+	2+ (a)	1	0	word (RWi) ←eam	–	–	–	–	–	–	–	–	–	–
MOVEA A, ear	2	1	0	0	word (A) ←ear	–	*	–	–	–	–	–	–	–	–
MOVEA A, eam	2+	1+ (a)	0	0	word (A) ←eam	–	*	–	–	–	–	–	–	–	–
ADDSP #imm8	2	3	0	0	word (SP) ← (SP) +ext (imm8)	–	–	–	–	–	–	–	–	–	–
ADDSP #imm16	3	3	0	0	word (SP) ← (SP) +imm16	–	–	–	–	–	–	–	–	–	–
MOV A, brgl	2	*1	0	0	byte (A) ← (brgl)	Z	*	–	–	–	*	*	–	–	–
MOV brg2, A	2	1	0	0	byte (brg2) ← (A)	–	–	–	–	–	*	*	–	–	–
NOP	1	1	0	0	No operation	–	–	–	–	–	–	–	–	–	–
ADB	1	1	0	0	Prefix code for accessing AD space	–	–	–	–	–	–	–	–	–	–
DTB	1	1	0	0	Prefix code for accessing DT space	–	–	–	–	–	–	–	–	–	–
PCB	1	1	0	0	Prefix code for accessing PC space	–	–	–	–	–	–	–	–	–	–
SPB	1	1	0	0	Prefix code for accessing SP space	–	–	–	–	–	–	–	–	–	–
NCC	1	1	0	0	Prefix code for no flag change	–	–	–	–	–	–	–	–	–	–
CMR	1	1	0	0	Prefix code for common register bank	–	–	–	–	–	–	–	–	–	–

*1: PCB, ADB, SSB, USB, and SPB : 1 state
DTB, DPR : 2 states

*2: 7 + 3 × (pop count) + 2 × (last register number to be popped), 7 when rlst = 0 (no transfer register)

*3: 29 + (push count) – 3 × (last register number to be pushed), 8 when rlst = 0 (no transfer register)

*4: Pop count × (c), or push count × (c)

*5: Pop count or push count.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 21 Bit Manipulation Instructions [21 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVB	A, dir:bp	3	5	0	(b)	byte (A) ← (dir:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, addr16:bp	4	5	0	(b)	byte (A) ← (addr16:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, io:bp	3	4	0	(b)	byte (A) ← (io:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	dir:bp, A	3	7	0	2× (b)	bit (dir:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	addr16:bp, A	4	7	0	2× (b)	bit (addr16:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	io:bp, A	3	6	0	2× (b)	bit (io:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
SETB	dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	io:bp	3	7	0	2× (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
CLRB	dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	io:bp	3	7	0	2× (b)	bit (io:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
BBC	dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBS	dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 1	–	–	–	–	–	–	*	–	–	–
SBBS	addr16:bp, rel	5	*3	0	2× (b)	Branch when (addr16:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
WBTS	io:bp	3	*4	0	*5	Wait until (io:bp) b = 1	–	–	–	–	–	–	–	–	–	–
WBTC	io:bp	3	*4	0	*5	Wait until (io:bp) b = 0	–	–	–	–	–	–	–	–	–	–

*1: 8 when branching, 7 when not branching
*2: 7 when branching, 6 when not branching
*3: 10 when condition is satisfied, 9 when not satisfied
*4: Undefined count
*5: Until condition is satisfied

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 22 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
SWAP	1	3	0	0	byte (A) 0 to 7 ↔ (A) 8 to 15	–	–	–	–	–	–	–	–	–	–
SWAPW/XCHW AL, AH	1	2	0	0	word (AH) ↔ (AL)	–	*	–	–	–	–	–	–	–	–
EXT	1	1	0	0	byte sign extension	X	–	–	–	–	*	*	–	–	–
EXTW	1	2	0	0	word sign extension	–	X	–	–	–	*	*	–	–	–
ZEXT	1	1	0	0	byte zero extension	Z	–	–	–	–	R	*	–	–	–
ZEXTW	1	1	0	0	word zero extension	–	Z	–	–	–	R	*	–	–	–

Table 23 String Instructions [10 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVS/MOVSI	2	*2	*5	*3	Byte transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSD	2	*2	*5	*3	Byte transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCEQ/SCEQI	2	*1	*5	*4	Byte retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCEQD	2	*1	*5	*4	Byte retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FISL/FILSI	2	6m +6	*5	*3	Byte filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–
MOVSW/MOVSWI	2	*2	*8	*6	Word transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSWD	2	*2	*8	*6	Word transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCWEQ/SCWEQI	2	*1	*8	*7	Word retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCWEQD	2	*1	*8	*7	Word retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FILSW/FILSWI	2	6m +6	*8	*6	Word filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–

m: RW0 value (counter value)
n: Loop count

*1: 5 when RW0 is 0, 4 + 7 × (RW0) for count out, and 7 × n + 5 when match occurs
*2: 5 when RW0 is 0, 4 + 8 × (RW0) in any other case
*3: (b) × (RW0) + (b) × (RW0) when accessing different areas for the source and destination, calculate (b) separately for each.
*4: (b) × n
*5: 2 × (RW0)
*6: (c) × (RW0) + (c) × (RW0) when accessing different areas for the source and destination, calculate (c) separately for each.
*7: (c) × n
*8: 2 × (RW0)

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Part number	Package	Remarks
MB90641APFV MB90P641APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90641APF MB90P641APF	100-pin Plastic QFP (FPT-100P-M06)	

■ PACKAGE DIMENSIONS

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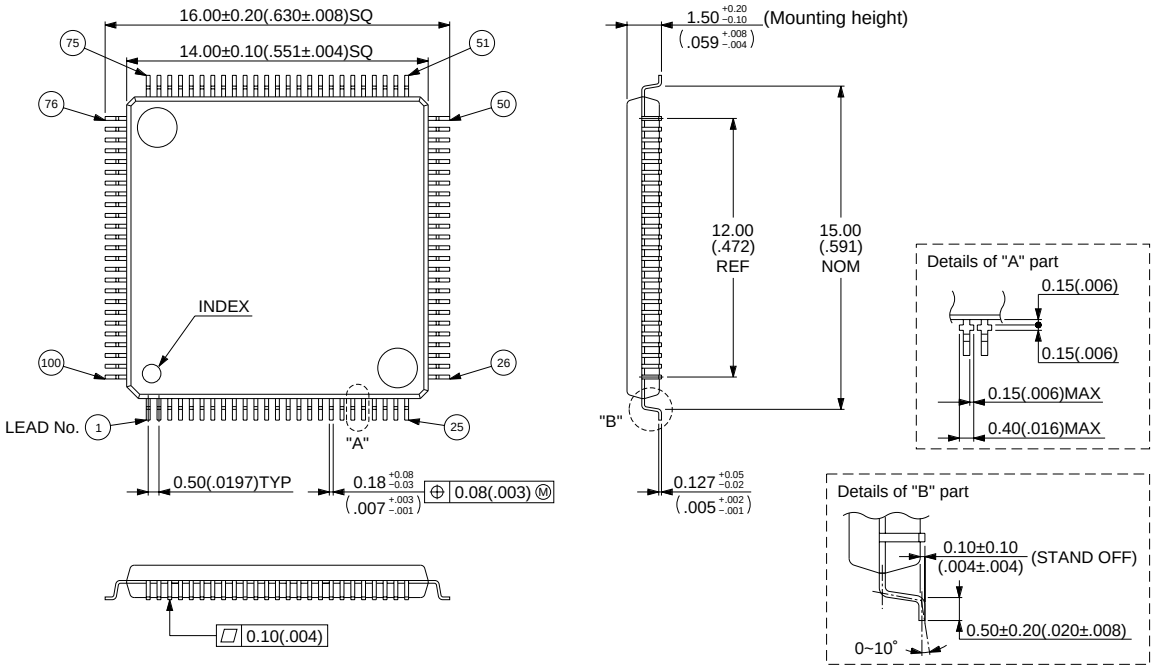

Dimensions in mm (inches)

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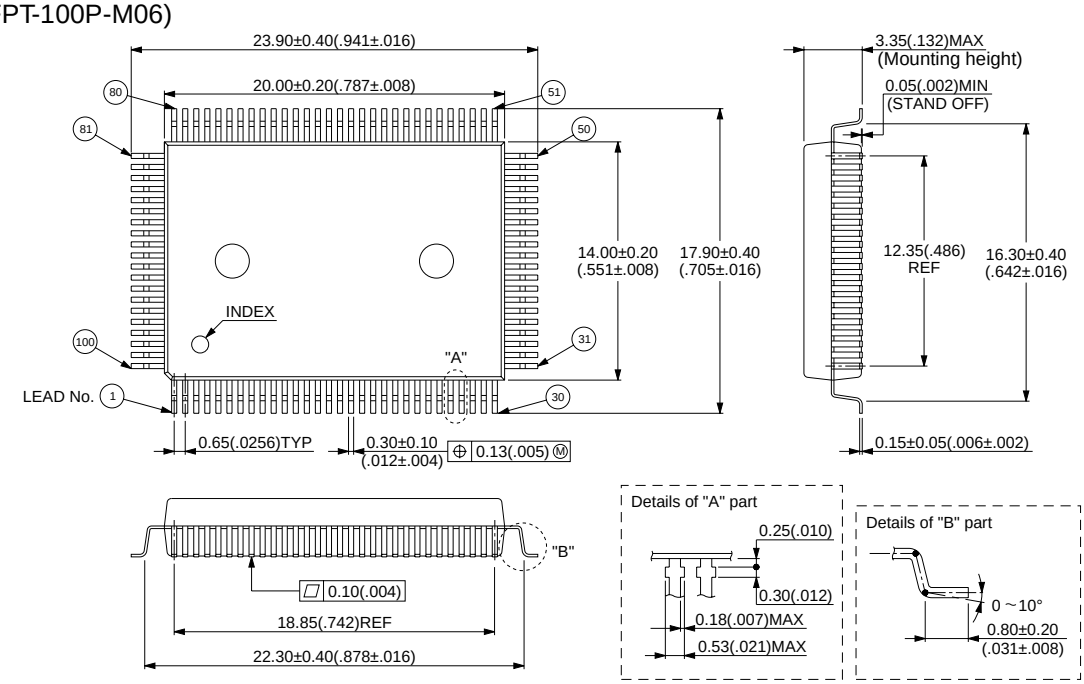

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