MV1471

HDB3/AMI ENCODER/DECODER

The MV1471, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The MV1471 is also capable of operating at clock rates up to 10MHz. The MV1471 circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1471 is an encoder/decoder for pseudo–ternary transmission codes. The code can be selected as either true Alternate Mark Inversion (AMI) code or AMI modified according to the HDB3 coding laws specified in Annex A of CCITT Recommendation G. 703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding and all ones detection. In addition a loop back function is provided for terminal testing.

FEATURES

- Single +5V supply
- All Inputs and Outputs TTL compatible
- Selectable HDB3 or AMI coding
- HDB3 Encoding and Decoding to CCITT Recommendation G. 703
- Simultaneous Encoding and Decoding
- Clock Recovery Signal allows Clock Regeneration from Incoming PCM data
- Loop Back Control
- HDB3 error monitor
- Alarm Indication Signal Monitor
- Low Power Operation
- 2.048MHz or 8.448MHz Operation

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Supply Voltage	–0.5V to +7V
Input Voltage	–0.5V to V_{DD} +0.5V
Output Voltage	–0.5V to V_{DD} +0.5V
Storage temperature (DP)	–55 to +150°C
Storage temperature (DG)	–65 to +150°C

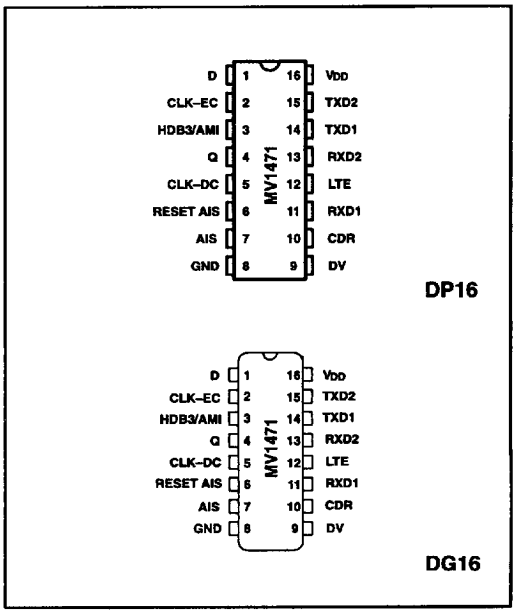


Fig. 1 Pin connections top view

ORDERING INFORMATION

MV1471/CG/DPAS
MV1471/CG/DGAS

Functional Description

High density bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zero's, the last zero is substituted by a mark of the same polarity as the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC components to the HDB3 signal.

The MV1471 consists of two main blocks, the HDB3/AMI Encoder and the HDB3/AMI Decoder, with the block diagram being shown in Fig. 2. The function of each block is now described separately.

HDB3/AMI Encoder

The HDB3/AMI Encoder is responsible for converting the incoming NRZ data into pseudo–ternary form for transmission over a 2.048Mbit/8.448Mbit PCM link according to either the true AMI rules or AMI modified according to the HDB3 encoding rules. In HDB3 mode, this conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G. 703, Annex A. Selection between the two encoding schemes is controlled by the HDB3/AMI control input. A logic high on this pin will configure the device in HDB3 mode.

The data to be encoded is input on the D input pin and the encoding process is synchronised to the 2.048/8.448MHz clock signal being input on the CLK–EC pin. The HDB3/AMI Encoder has two outputs, TXD1 and TXD2, which represent the encoded PCM data stream in pseudo–ternary form. If a mark or HDB3 violation is to be transmitted the output pulses high after the rising edge of the clock, with the length of the pulse set by the clock high pulse width. The timing diagram of the HDB3/AMI Encoder is shown in Fig. 3.

HDB3/AMI Decoder

The HDB3/AMI Decoder circuit is responsible for converting the 2.048Mbit/8.448Mbit HDB3/AMI encoded pseudo–ternary PCM data stream on its inputs, RXD1 and RXD2, into NRZ binary form to be output on the Q output pin. In HDB3 mode this conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G. 703, Annex A. The HDB3/AMI decoder synchronously decodes the data on its RXD input pins into NRZ form under control of the 2.048MHz/8.448MHz clock being input on its CLK–DC pin. There is a 5 clock period delay between the encoded data being clocked in from the RXD inputs and the NRZ data appearing on the Q output. The Decoder clock must be externally regenerated from the incoming PCM data streams and in order to aid this clock recovery a logical 'OR' function of the decoder inputs is output on the CDR pin.

In addition to the HDB3/AMI decoding the circuit also provides two alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zero's have been detected in the preceding two RESET AIS=1 periods (i.e. between two RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. All the alarm circuit as well as the decoding process is synchronised to the clock signal being input on the CLK–DC pin. The clock signal may by asynchronous with the CLK–EC signal. The timing diagrams of the HDB3/AMI Decoder circuit are shown in Fig.4. In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LTE (Loop Test Enable) input high. In this mode, the HDB3/AMI encoded pseudo–ternary data outputs of the encoder block are fed back as the inputs to the decoder block, which in turn decodes this data and outputs it in NRZ form.

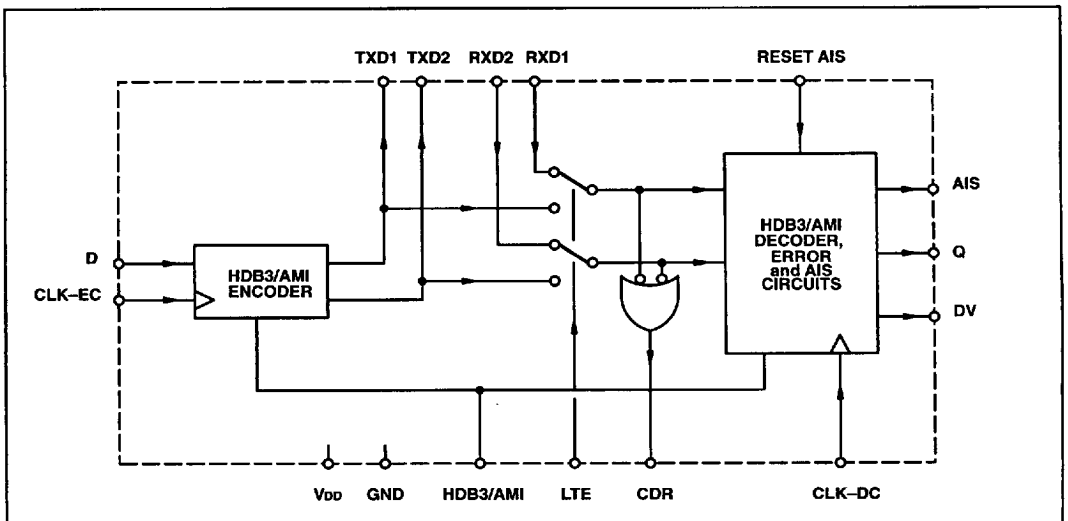
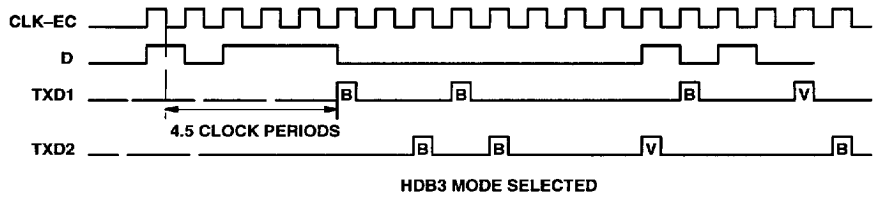
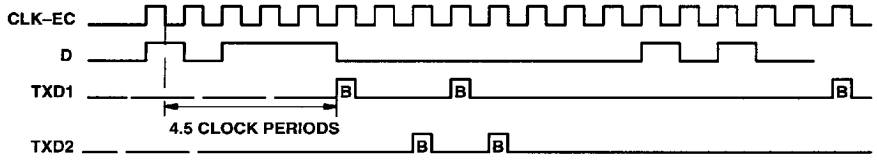


Fig. 2 Block diagram



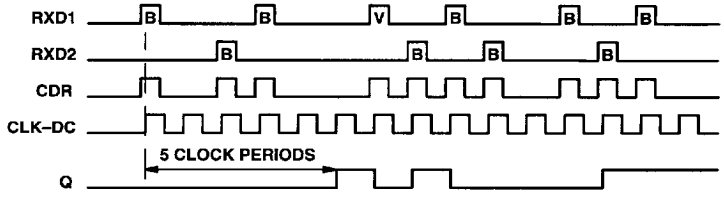
HDB3 MODE SELECTED



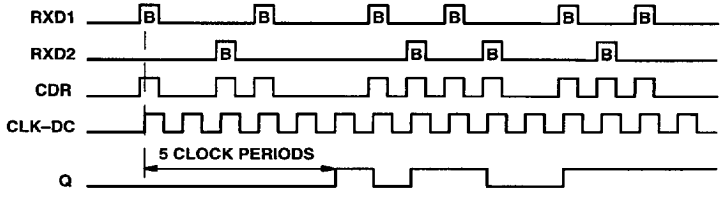
AMI MODE SELECTED

NOTES 1) The Encoder outputs, TXD1/2 are delayed by 4.5 clock periods with respect to D.
2) B is a HDB3 mark, V is a HDB3 violation.
3) Both diagrams assume the last mark occured on TXD2 and the last violation on TXD1.

Fig. 3 HDB3/AMI Encoder waveforms



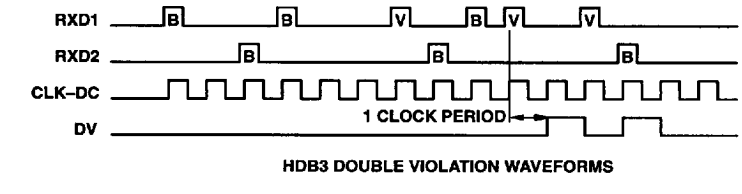
DECODER WAVEFORMS – HDB3 MODE SELECTED



DECODER WAVEFORMS – AMI MODE SELECTED

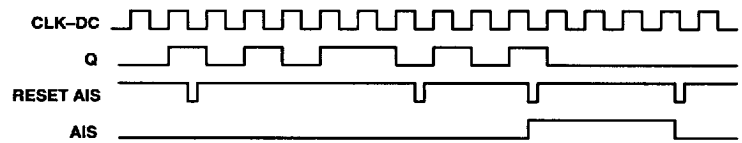
NOTES 1) The decoder NRZ output is delayed by 5 clock periods with respect to the PCM inputs.
2) B is a HDB3 mark, V is a HDB3 violation.
3) The diagrams assume that the last mark and last violation both occured on RXD2.

Fig. 4 HDB3/AMI Decoder waveforms



HDB3 DOUBLE VIOLATION WAVEFORMS

NOTES 1) The DV output is delayed by 1 clock period with respect to the PCM inputs
2) The diagrams assume that the last mark and last violation both occured on RXD2.
3) B is a HDB3 mark, V is a HDB3 violation.



AIS WAVEFORMS

Fig. 4 HDB3/AMI Decoder waveforms ***(continued)***

PIN DESCRIPTION

Pin Name	Pin No	Description
D	1	NRZ Data Input pin to HDB3/AMI Encoder. The NRZ binary data on this pin is input to the HDB3/AMI Encoder for conversion to HDB3/AMI pseudo–ternary form under control of the CLK–EC signal. The D input is latched into the encoder block by the falling edge of CLK–EC.
CLK–EC	2	2.048MHz Clock Input to HDB3 Encoder. The clock signal on this input is used for the encoding of data on pin 1.
HDB3/AMI	3	HDB3/AMI Mode Select Input. A logic high on this pin selects HDB3 operation. A logic low selects AMI mode.
Q	4	NRZ Data Output from HDB3/AMI Decoder. This output represents the HDB3/AMI input data decoded back into NRZ binary form, with a 5 clock period delay from the PCM inputs to the NRZ output. This decoding process is carried out under control of the CLK–DC signal.
CLK–DC	5	2.048MHz Clock Input to HDB3/AMI Decoder. The clock signal on this pin is used for decoding of data on the RXD input pins, or the TXD pins in Loop Test Mode. This pin is used to input the externally regenerated clock signal recovered from the incoming HDB3/AMI waveforms back to the decoder block.
RESET AIS	6	Reset AIS Input to HDB3/AMI Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3/AMI decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding two RESET AIS=1 periods. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
AIS	7	Alarm Indicator Signal Output from HDB3/AMI Decoder. See description for RESET AIS pin.
GND	8	Digital Ground. 0V.
DV	9	Double Violation Alarm Output from HDB3/AMI Decoder. This output goes high for one period of CLK–DC, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
CDR	10	Clock Recovery Output from HDB3/AMI Decoder. This pin is used to output the logical 'OR' function of the PCM inputs for the use of the external clock recovery circuit.

RXD1	11	HDB3/AMI Encoded Input 1 to HDB3/AMI Decoder. This is one of the pair of 2.048Mbit/8.448Mbit pseudo–ternary PCM data stream inputs to the HDB3/AMI Decoder. This input asynchronously latches the incoming HDB3/AMI data and is rising edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
LTE	12	Loop Test Enable Control Input. A logic low on this pin selects normal operation, with encoding and decoding being independent and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied.
RXD2	13	HDB3/AMI Encoded Input 2 to HDB3/AMI Decoder. See description for pin RXD1.
TXD1	14	HDB3/AMI Encoded Pseudo–Ternary Output 1 from HDB3/AMI Encoder. The NRZ PCM data stream being input on the D pin is HDB3/AMI encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK–EC to TXD1.
TXD2	15	HDB3/AMI Encoded Pseudo–Ternary Output 1 from HDB3/AMI Encoder. See Pin TXD1 description.
VDD	16	Digital Supply Voltage. 5V.

NOTES

1. All inputs except HDB3/AMI have 100K on–chip pull down resistors. HDB3/AMI has a 100K on–chip pull–up resistor.

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply Voltage V_{DD} = 5V ±0.5V Ambient Temperature T_{amb} = 0°C to + 70°C

STATIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low level input voltage	V_{IL}	0.0		0.8	V	
High level input voltage	V_{IH}	2.0		V_{DD}	V	
Low level output voltage	V_{OL}			0.4	V	I_{sink} = 2mA
High level output voltage	V_{OHT}	2.4			V	I_{source} = 2mA
	V_{OHC}	V_{DD}–1.0			V	I_{source} = 1mA
Input leakage current	I_{IL}	–10		200	µA	V_{in} = V_{DD} or GND
Supply current	I_S			5	mA	2.048MHz operation Note 1.
				15	mA	8.448MHz operation Note 1.
Input capacitance	C_{IN}		5		pF	All inputs
Output capacitance	C_{OUT}		5		pF	All outputs

NOTES

1. All supply currents measured with outputs unloaded. These currents are not tested but are guaranteed by characterisation and a static current test.

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock period	t_{CP}	100			ns	See Fig. 5
Clock rise/fall time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock high/low time	t_{CH}/t_{CL}	30			ns	See Fig. 5

(cont.)DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
ENCODER						
Encoder data setup time	t_{EDS}	15			ns	See Fig. 6
Encoder data hold time	t_{EDH}	15			ns	See Fig. 6
TXD1/TXD2 output propagation delay	t_{EPDR} t_{EPDF}			45	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 data setup time	t_{RS}	20			ns	See Fig. 7
RXD1/2 pulse width	t_{RW}	20			ns	See Fig. 7
CDR propagation delay	t_{CPDR}/ t_{CPDF}			45	ns	See Fig. 7, Note 1.
Decoder output propagation delay	t_{OPD}			45	ns	See Fig. 7, Note 1.and 2.
RESET AIS hold–off time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS pulse width	t_{RAW}	15			ns	See Fig. 7
Reset AIS setup time	t_{RAS}	10			ns	See Fig. 7
AIS propagation delay	t_{APD}			55	ns	See Fig. 7, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. The t_{OPD} parameter applies to outputs Q, and DV, but does not apply to AIS.

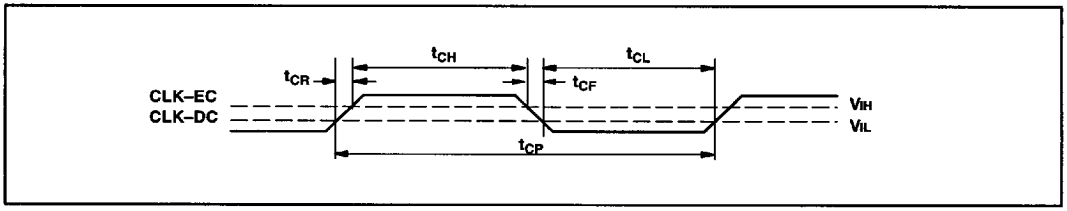


Fig. 5 Clock timing parameters

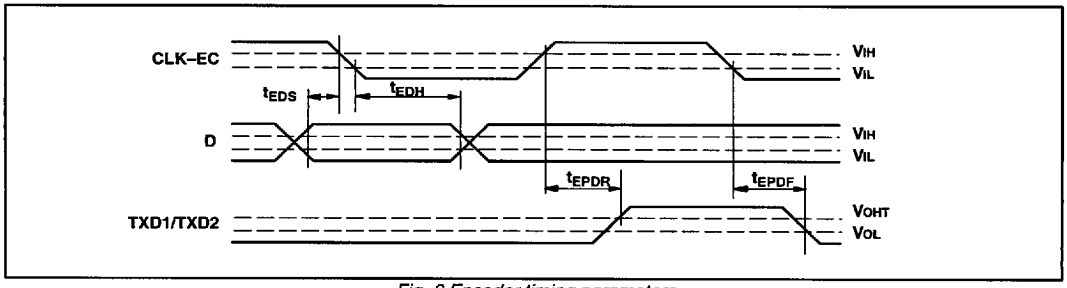


Fig. 6 Encoder timing parameters

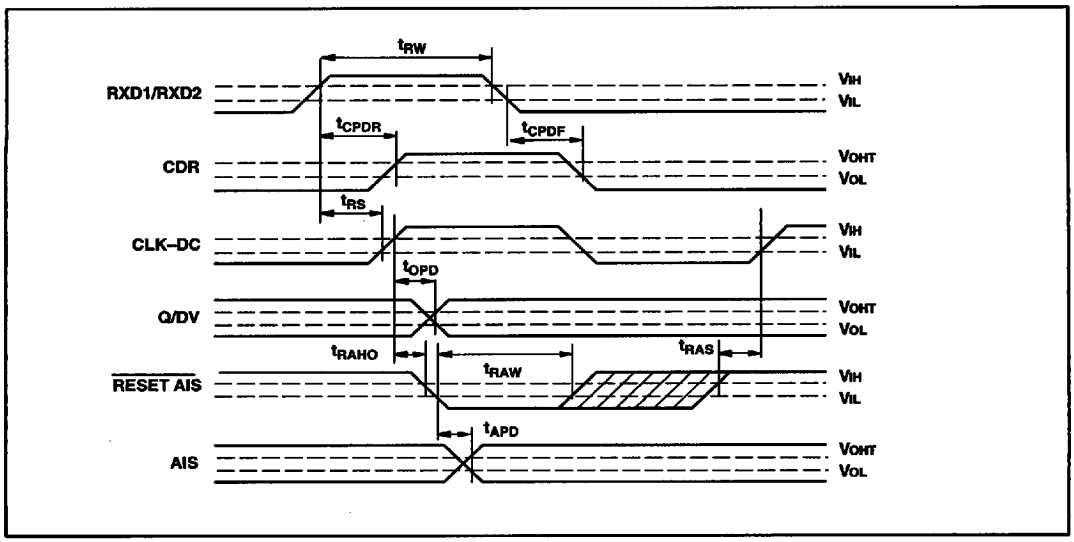


Fig. 7 Decoder timing parameters