

QL92010M QuickMIPS™ IDE Controller Core Data Sheet



••••• QuickMIPS Embedded Standard Products (ESP) Family

Introduction

This data sheet describes the QL92010M QuickMIPS Integrated Drive Electronics (IDE) controller core and how to use it in applications. This document also defines the core's capabilities and functionality.

NOTE: This data sheet only covers the IDE controller core, see the QL902M data sheet for information regarding the remainder of the QuickMIPS device.

The IDE controller core consists of three blocks; these blocks are the IDE control, Fabric slave, and secondary interrupt request (SIRQ) control. The SIRQ control block manages IDE- and Fabric-based interrupts which are forwarded to the MIPS CPU. The Fabric slave block provides a simplified System bus style interface available for designers to connect their Fabric designs.

Features

The IDE controller core has the following features:

- PIO Mode 0 to PIO Mode 4 support.
- Fabric-accessible slave bus interface running at up to 100 MHz. One slave can be connected by the Fabric designer.
- AHB and Fabric slave interfaces support bursting.
- Internal IDE sector buffering for increased performance (back-to-back sector transfer).

- Controller performance close to maximum PIO mode performance (in back-to-back mode at 100 MHz/32-bit mode, running up to 15.25 MBps excluding OS overhead).
- 32-bit data transfers supported.
- Internal ATA timing registers for PIO modes.
- Compact flash/PCMCIA card compatible in TRUE-IDE/ATA mode.
- SIRQ control block supports level or edge interrupts.
- Maximum of four interrupt sources available for Fabric design.
- SIRQ enable and status registers.
- Selectable interrupt input polarity.
- 1,695 logic cells available for Fabric designs.
- 32 RAM blocks available for Fabric designs.

Applications

The QL92010M device can be used in:

- Set-top boxes
- DVD players
- PDAs
- Industrial control
- Embedded systems
- Laptops

QL92010M IDE Controller Core

This section describes the functionality of the IDE controller core. For detailed information relating to the IDE controller registers, see the [QL90xM QuickMIPS User Manual](#), Appendix B. For detailed information about interfacing to the Fabric slave port in this device, see the [QL90xM QuickMIPS User Manual](#), Appendix A. **Figure 1** shows a block diagram of the QL92010M device including the IDE controller core.

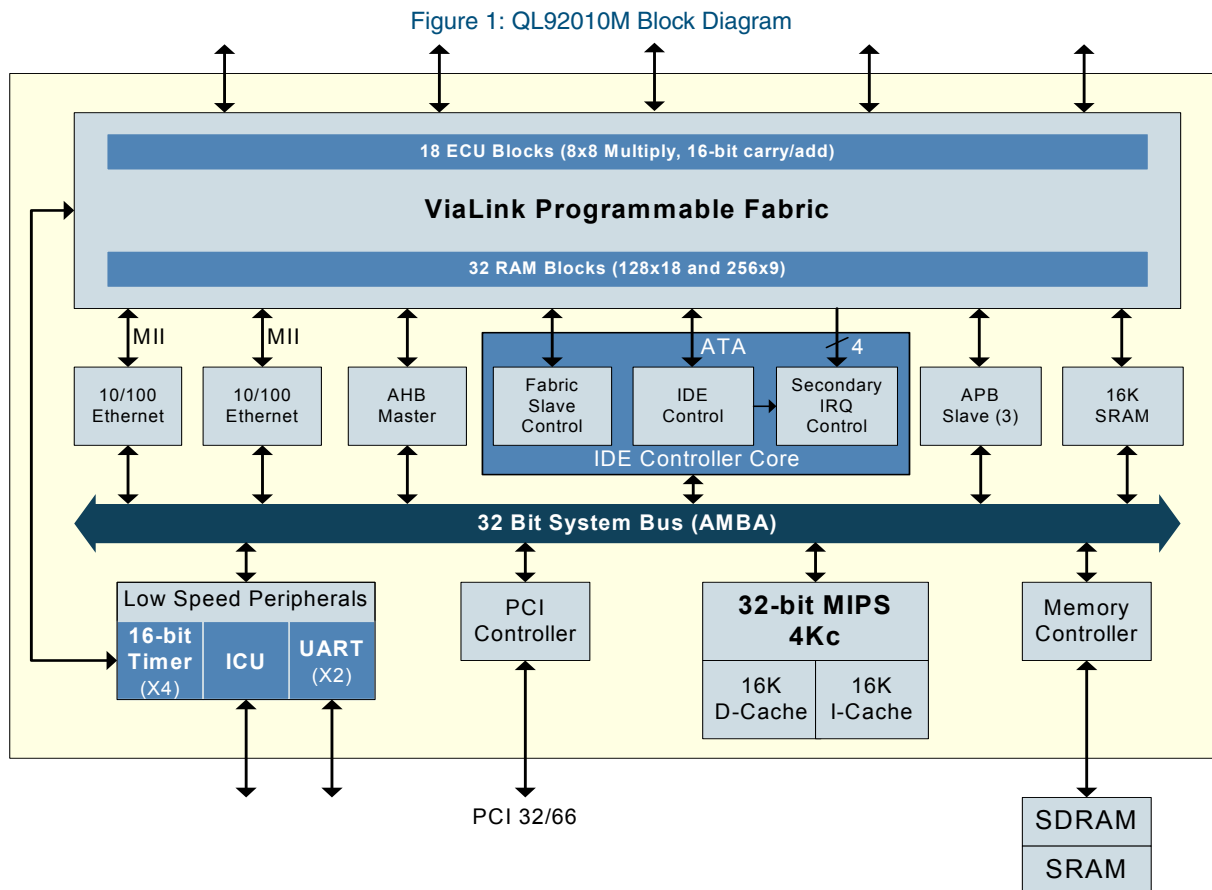
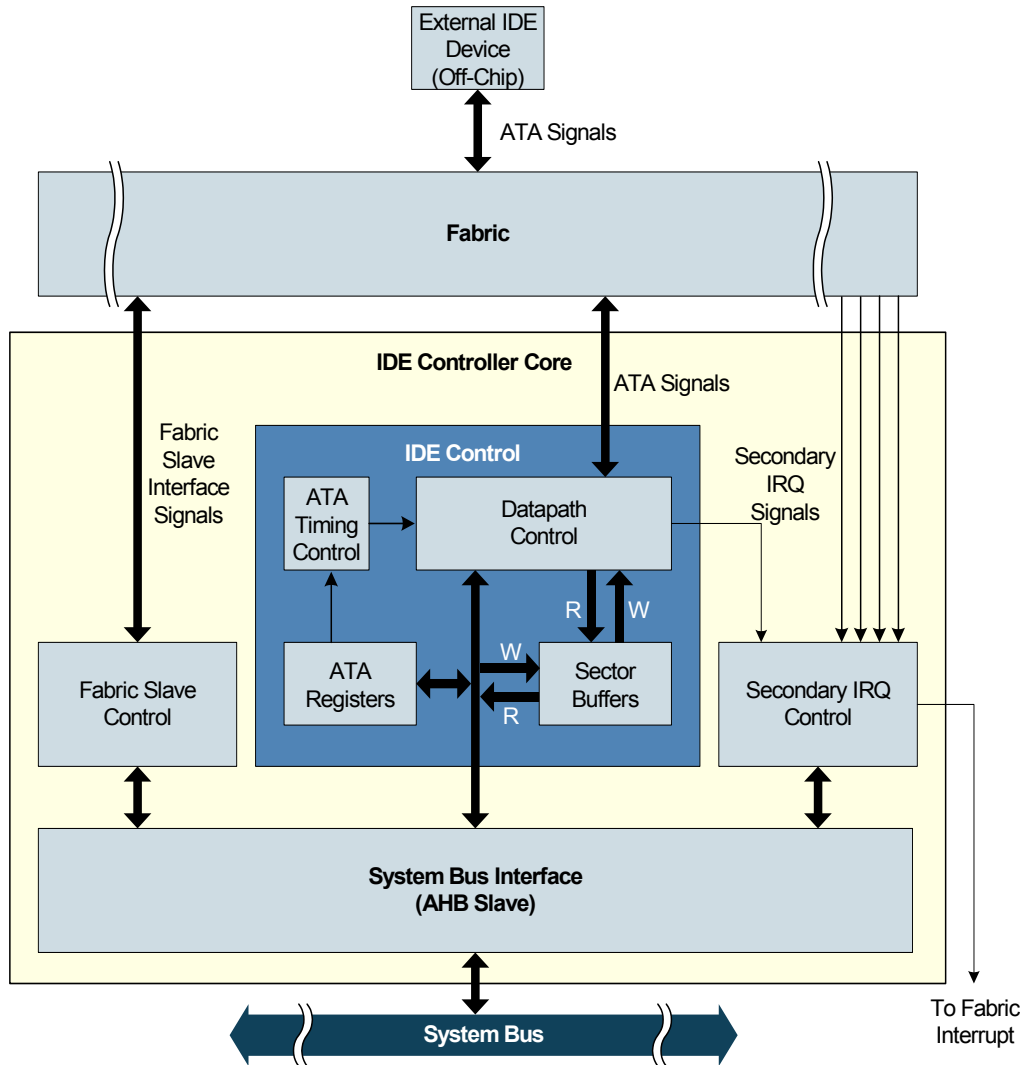


Figure 2 shows a detailed block diagram of the IDE controller core. The sub-blocks of the core are also shown, including the Fabric slave control, IDE control, and secondary IRQ control blocks.

Figure 2: IDE Controller Core Block Diagram



Interface Ports

Table 1 describes the Fabric-accessible interface ports for the IDE controller core. Some ports must be connected directly to Fabric I/O pins while other ports provide Fabric design connection to the System bus (AMBA) internal to the device. All signals beginning with “ata_” should be routed directly to Fabric I/O pins on the QL92010M device. The design database included in the QuickWorks software for the QL92010M device also includes a top level VHDL or Verilog file showing an example of tying these signals to Fabric I/O pins. All other signals in **Table 1** can be used by the designer’s specific Fabric design (e.g., Fabric slaves or interrupt sources).

Table 1: IDE Controller Port Descriptions

Port	I/O ^a	Function
ATA Interface Signals		
ata_addr(2:0)	O	ATA address lines. Addresses registers contained in the external device.
ata_cs1_n	O	ATA chip select 1. Chip select for the externally connected device.
ata_cs0_n	O	ATA chip select 0. Chip select for the externally connected device.
ata_data_in(15:0)	I	ATA data input. Read data from the externally connected device.
ata_data_out(15:0)	O	ATA data output. Write data to the externally connected device.
ata_data_oe	O	ATA data output enable. When high, ata_data_out is driven to the external device.
ata_io_rd_n	O	ATA I/O read. When low, a read is performed from the externally connected device.
ata_io_wr_n	O	ATA I/O write. When low, a write is performed to the externally connected device.
ata_intr	I	ATA interrupt input. Interrupt from the externally connected device.
ata_io_rdy	I	ATA I/O ready. When high, indicates that the external device is ready for access.
ata_reset_n	O	ATA reset. Active low reset output to the externally connected device.
Fabric Slave Interface Signals		
hclk	O	Fabric slave interface clock. This clock is synchronous to the System bus (AMBA) clock.
hresetn	O	Fabric slave active low reset. This signal can be used to reset all Fabric logic implemented by the designer.
ahb_sl_sel	O	Indicates that the Fabric slave is selected for the current transaction.
ahb_sl_addr(31:0)	O	Fabric slave address.
ahb_sl_wdata(31:0)	O	Fabric slave write data.
ahb_sl_rdata(31:0)	I	Fabric slave read data.
ahb_sl_we	O	Indicates that the current Fabric slave transaction is a write operation.
ahb_sl_re	O	Indicates that the current Fabric slave transaction is a read operation.
ahb_sl_hsize(2:0)	O	Indicates the size of the current Fabric slave transfer (8, 16, or 32 bits).
ahb_sl_burst(2:0)	O	Indicates the burst type and length of the current Fabric slave transfer (SINGLE, INCR, WRAP4, INCR4, WRAP8, INCR8, WRAP16 or INCR16).
ahb_sl_burst_start	O	Indicates that the Fabric slave is starting a burst transaction.
ahb_sl_burst_cont	O	Indicates that the Fabric slave is continuing a burst transaction.
ahb_sl_wait	I	When high, indicates that the Fabric slave intends to insert wait states to the current transfer.

Table 1: IDE Controller Port Descriptions (Continued)

Port	I/O ^a	Function
ahb_sl_ign_ws	I	When high, indicates that the Fabric slave, when inserting wait states with the ahb_sl_wait signal, intends to do so indefinitely. When low, the transaction is automatically completed after a maximum of 16 cycles regardless of the ahb_sl_wait signal.
Secondary IRQ Signals		
sirq_in(4:1)	I	Secondary interrupt controller input signals.

a. Interface direction is specified with respect to the ASSP portion of the device. I designates an input to the ASSP and O designates an output from the ASSP.

Table 2 shows the IDE Controller ATA interface ports and the corresponding Fabric pin names and locations. The pin locations in **Table 2** indicate the default location for using the QL92010M device in the QuickMIPS Development Platform (QDP) when using the IDE/VGA daughter card. Alternatively, designers can choose other pin locations for their specific target system.

Table 2: ATA Interface Signals and Recommended Fabric IO Pin Locations

ATA Interface Signal	ATA Interface Direction ^a	Fabric Pin Signal	Fabric Pin Type	Fabric Pin Location
ata_addr(0)	O	ata_addr(0)	O	D20
ata_addr(1)	O	ata_addr(1)	O	E17
ata_addr(2)	O	ata_addr(2)	O	D17
ata_cs1_n	O	ata_cs1_n	O	A21
ata_cs0_n	O	ata_cs0_n	O	D21
ata_data_in(0)	I	ata_data(0)	I/O	J24
ata_data_out(0)	O			
ata_data_in(1)	I	ata_data(1)	I/O	G22
ata_data_out(1)	O			
ata_data_in(2)	I	ata_data(2)	I/O	J23
ata_data_out(2)	O			
ata_data_in(3)	I	ata_data(3)	I/O	F22
ata_data_out(3)	O			
ata_data_in(4)	I	ata_data(4)	I/O	E22
ata_data_out(4)	O			
ata_data_in(5)	I	ata_data(5)	I/O	G23
ata_data_out(5)	O			
ata_data_in(6)	I	ata_data(6)	I/O	E23
ata_data_out(6)	O			
ata_data_in(7)	I	ata_data(7)	I/O	G24
ata_data_out(7)	O			
ata_data_in(8)	I	ata_data(8)	I/O	H23
ata_data_out(8)	O			
ata_data_in(9)	I	ata_data(9)	I/O	D19
ata_data_out(9)	O			

Table 2: ATA Interface Signals and Recommended Fabric IO Pin Locations (Continued)

ATA Interface Signal	ATA Interface Direction ^a	Fabric Pin Signal	Fabric Pin Type	Fabric Pin Location
ata_data_in(10)	I	ata_data(10)	I/O	E19
ata_data_out(10)	O			
ata_data_in(11)	I	ata_data(11)	I/O	D18
ata_data_out(11)	O			
ata_data_in(12)	I	ata_data(12)	I/O	E18
ata_data_out(12)	O			
ata_data_in(13)	I	ata_data(13)	I/O	E20
ata_data_out(13)	O			
ata_data_in(14)	I	ata_data(14)	I/O	E21
ata_data_out(14)	O			
ata_data_in(15)	I	ata_data(15)	I/O	D22
ata_data_out(15)	O			
ata_data_oe	O	NA	N/A	NA
ata_io_rd_n	O	ata_io_rd_n	O	C16
ata_io_wr_n	O	ata_io_wr_n	O	C20
ata_intr	I	ata_intr	I	A25
ata_io_rdy	I	ata_io_rdy	I	B19
ata_reset_n	O	ata_reset_n	O	B20

a. ATA Interface direction is specified with respect to the ASSP portion of the device. I designates an input to the ASSP and O designates an output from the ASSP.

NOTE: The ATA data signals, `ata_data_in(15:0)` and `ata_data_out(15:0)`, are unidirectional interface ports on the IDE Controller core. These signals must be connected along with the `ata_data_oe` signal to the `bipad_25um` macro. Instantiating this macro is required for each of the 16 ATA data signals to connect them to bidirectional Fabric I/O pins.

Fabric Slave Control Block

The Fabric slave interface is closely related to the System bus (AMBA AHB). However, the Fabric interface has been simplified which also simplifies the design of slave devices, saves logic cells, and pipelines the design to reduce high fanout signals. The Fabric slave interface supports one slave that the designer can implement in the Fabric design. The slave responds to a certain address range in the QL92010M memory map. For detailed information about the Fabric slave interface in this device, see the [QL90xM QuickMIPS User Manual](#), Appendix A.

Secondary IRQ Control Block

The secondary IRQ control block is responsible for consolidating four Fabric interrupt sources and the IDE interrupt from the IDE control block and forwarding these interrupts to the CPU. The Fabric interrupts are available for connection to the fabric logic created by the designer. These interrupts are highly configurable and can be controlled and monitored by the CPU. For a detailed description of how to use the secondary IRQ signals, see the [QL90xM QuickMIPS User Manual](#), Appendix B.

IDE Control Block

The IDE control block can be used to control any device supporting PIO modes 0 through 4. The IDE control block consists of the following logic sections:

- ATA Registers
- ATA Timing Control
- Sector Buffers
- Datapath Control

ATA Registers

The IDE control block in the QL92010M device has several registers used for setting the controller mode, indicating the state machine status, and setting the PIO mode timings related to the chosen System bus (AMBA) clock frequency. All registers are memory mapped, and the external device IDE registers are combined with the ATA registers present in the IDE control block core. See the [QL90xM QuickMIPS User Manual](#), Appendix B for a detailed description of the IDE control and ATA registers.

ATA Timing Control

PIO mode timing is determined from the PIO mode timing registers ATA_T1_REG through ATA_T4_REG and ATA_TIORDY_REG. All timing is based upon the frequency of the System bus (AMBA) clock. See the [QL90xM QuickMIPS User Manual](#), Appendix B for a detailed description of the PIO mode timing registers.

NOTE: Setting a value in a register that does not meet the PIO mode timings will result in operating failure and could cause data corruption.

For a detailed description of PIO Mode timing see the ATA/ATAPI-5 specification document *ANSI NCITS 340-2000*.

Sector Buffers

The IDE control block has two sector buffers which can hold 512 bytes of information each. One buffer is used for reading and one for writing.

The IDE control block can operate in two modes of operation, normal and back-to-back modes. When operating in normal mode the sector buffers are bypassed. In back-to-back mode the sector buffers are also bypassed when accessing IDE disk control registers. However, in back-to-back mode when transferring data, the internal buffers are filled first, and then the data is transferred to the IDE disk at the rate defined by the PIO mode timing registers.

Software must not access any IDE disk registers when transferring data to or from the IDE disk in back-to-back mode because this can cause data corruption. Most standard IDE disk drivers avoid this as a normal practice. The actual start of reading or writing is triggered automatically by the controller when in back-to-back mode:

- The first read access to the data register is flagged to the bus interface as if the controller is busy. The software (or hardware bus master) keeps trying until it succeeds. To accomplish this, the busy bit in the IDE ATA_CTRL register is continuously polled. While polling, the CPU can also perform other tasks. During this time the IDE disk must be setup so that data can be transferred. The controller transfers the data to the internal buffers. After the transfer is completed the busy flag is cleared and the software (or bus master) can try again and the action will succeed.

NOTE: Do not access any other IDE disk register during the polling process, as this will cause data corruption.

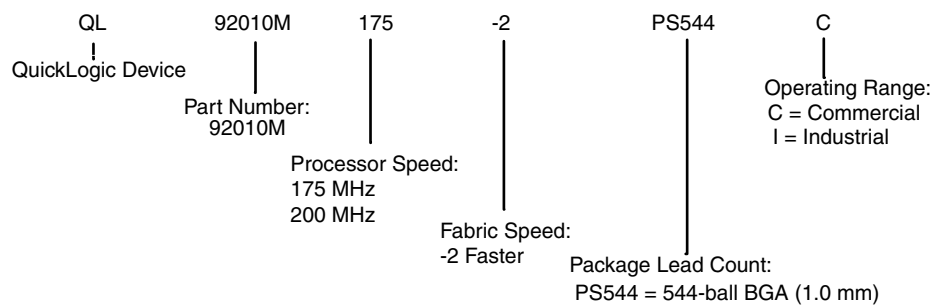
- The buffer registers are the destination for the write accesses. After the last word written, the controller automatically transfers the data to the IDE disk. The disk must be set up correctly and ready to accept data.

The sector buffers can accept two types of data, 16-bit or 32-bit. 32-bit mode is supported only when the controller is in back-to-back mode. In 32-bit mode, the IDE data is transferred into the sector buffers 32 bits at a time and transferred to the external IDE disk in 16-bit accesses. Regardless of the selected data mode, when accessing the external IDE disk registers, only the lower 8 bits are used, the rest of the bits are discarded.

Datapath Control

The IDE control block contains a datapath control section that manages the ATA_ signal ports in the Fabric of the QL92010M device. The datapath control section is responsible for reading and writing of external ATA data, including accesses to external ATA device registers. All ATA signal timing is also implemented in this section based upon control from the ATA Timing Control section. Management of read and write data to/from the sector buffers is also handled by the datapath control logic.

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Revision History

Revision	Date	Originator and Comments
Revision A	November 2004	Judd Heape, Richard Meester, and Kathleen Murchek General reformat and edit. Combined Quest IDE Controller IP and IRQ Controller IP data sheets.
Revision B	March 2005	Judd Heape and Kathleen Murchek Removed ata_dma_req and ata_dma_ack interface signals. Updated number of logic cells available for Fabric designs.

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