

# SED1351

## GRAPHICS LCD CONTROLLER

### DESCRIPTION

The SED1351F is a graphics LCD controller capable of controlling medium to large resolution displays. It transfers data from MPU to external frame buffer RAM and converts this data to display signals for LCD drivers. The SED1351F can display images with 4 gray shades and support display duty cycle as high as 1/1024.

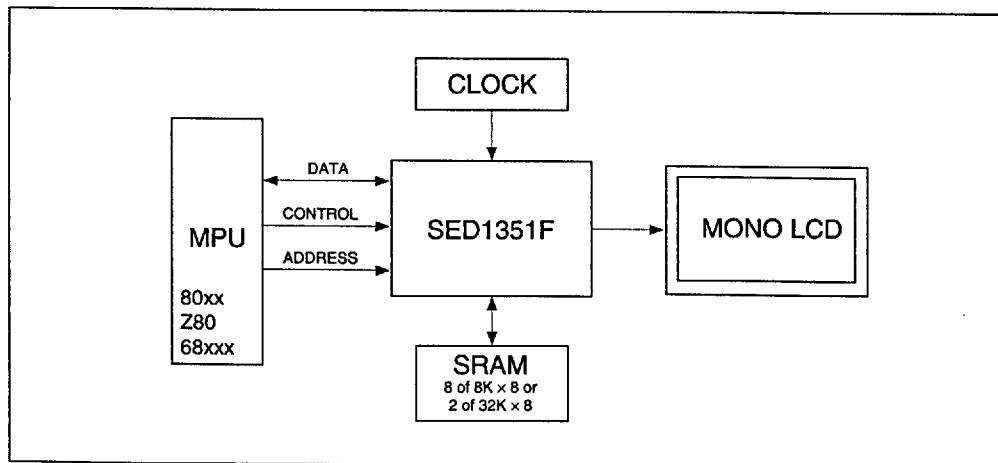
The SED1351F is designed to achieve high efficiency and data throughput to the LCD. It has a cycle steal mode which allows MPU to access frame buffer RAM without interfering with the display operation. The SED1351F can directly interface with up to eight 64K-bit SRAMs or two 256K-bit SRAMs.

The SED1351F can operate with either 5V or 3V power supply. The 5V version chip is the SED1351F0A and the 3V version chip is the SED1351FLB.

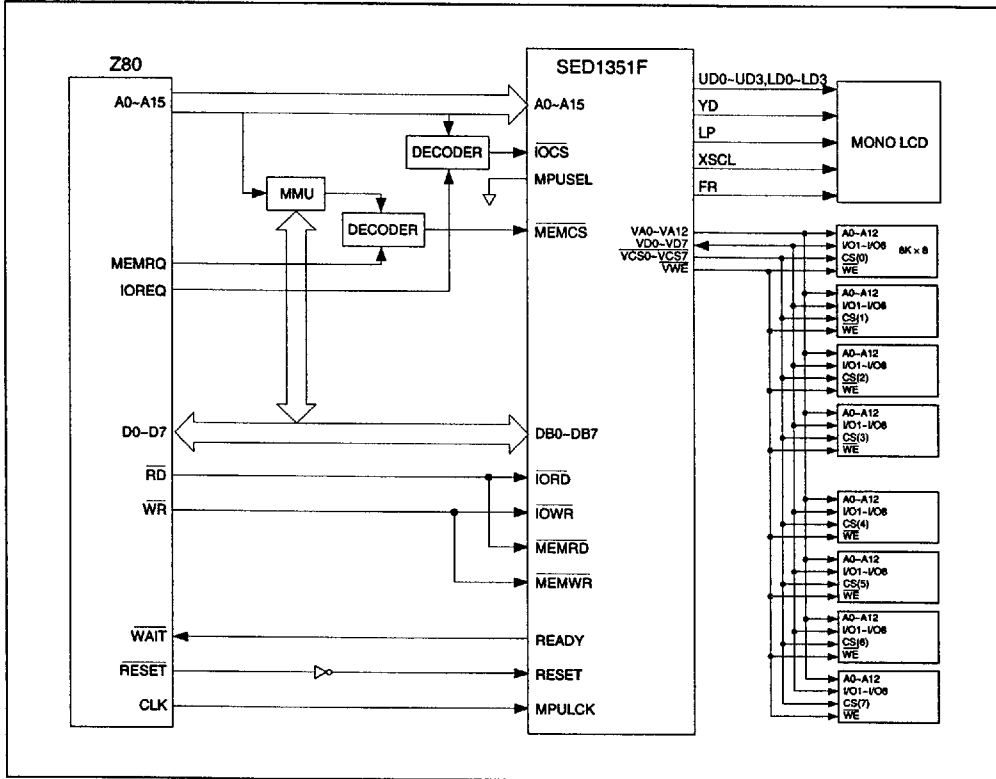
### FEATURES

- Low-power CMOS technology
- 8-bit or 16-bit MPU data interface
- Direct interface with 80xx, Z80 and 68xxx MPU
- 4- or 8-bit panel data bus for single panel and 4-bit bus for dual panel
- Support logical OR of layers and panel division
- Smooth vertical scrolling
- Virtual screen display up to 1024
- Binary mode (on/off only) generates black & white images
- Gray mode (on/off and two gray steps) generates images with 4 gray shades
- Maximum number of rows
  - Binary mode ..... 2048
  - Gray mode ..... 1024
- Maximum number of rows:
  - Single panel ..... 1024
  - Dual panel ..... 2048
- Maximum display sizes when 64K-byte SRAMs are used:
  - Binary mode ..... 2048 × 256 / 1024 × 512
  - Gray mode ..... 1024 × 256 / 512 × 512
- Available models:
  - SED1351F0A ..... 5V, QFP5-100 pin
  - SED1351FLB ..... 3V, QFP15-100 pin

### SYSTEM BLOCK DIAGRAM

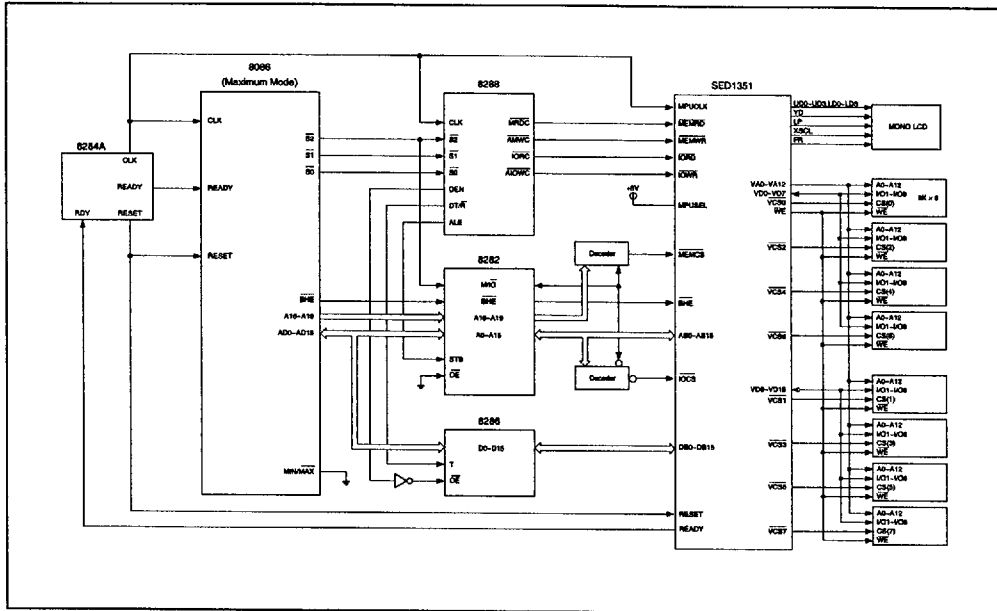


■ INTERFACE WITH 8-BIT MPU (Z-80) AND 64K-BIT SRAM (8 of 8K x 8)



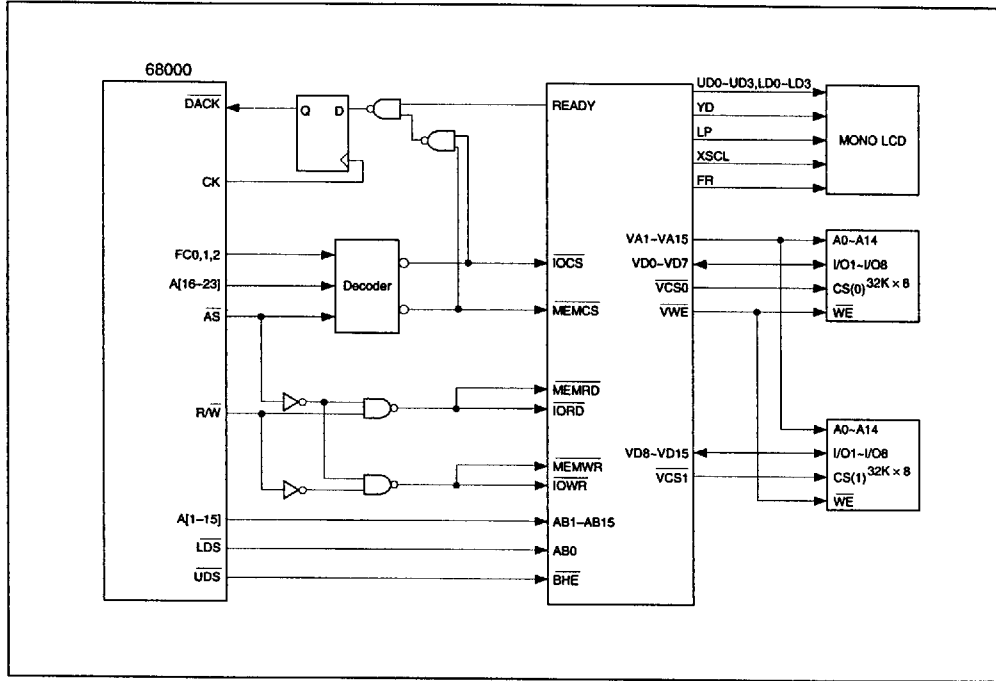
Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (8086) AND 64K-BIT SRAM (8 of 8K x 8)



Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (68000) AND 256K-BIT SRAM (2 of 32K x 8)

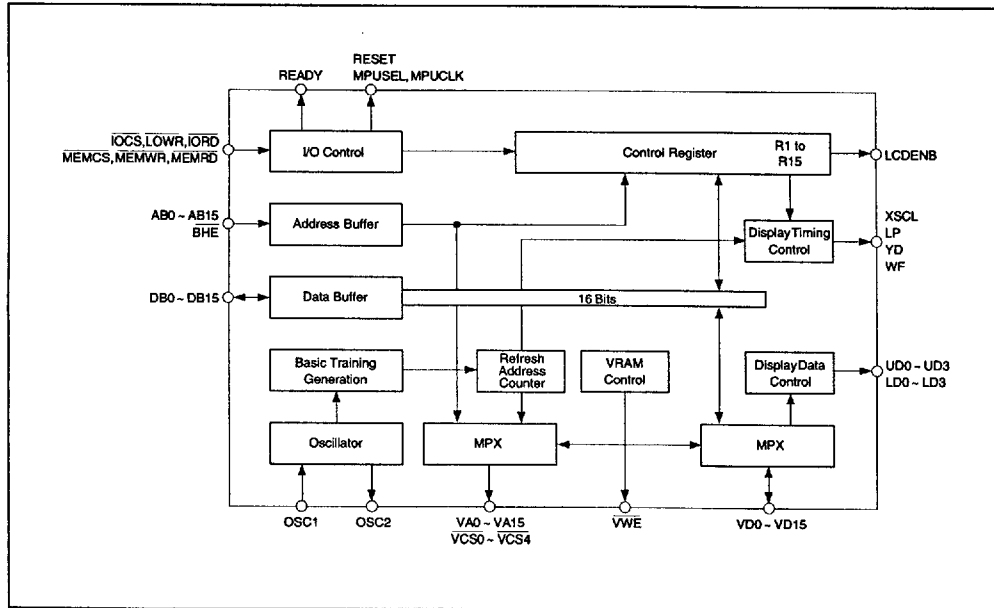


**Note:** Example implementation, actual may vary.

■ SUPPORTED RESOLUTIONS

Display RAM	Maximum Display Size				SRAM Type	CPU Interface	SRAM Interface
	Monochrome		4 Grayscale				
	X	Y	X	Y			
8K	256	× 256	256	× 128	1 of 8K × 8	8 bit	8 bit
16K	512	× 256	256	× 256	2 of 8K × 8	8 bit	8 bit
					16 bit	16 bit	
24K	512	× 384	384	× 256	3 of 8K × 8	8 bit	8 bit
32K	512	× 512	512	× 256	4 of 8K × 8	8 bit	8 bit
					1 of 32K × 8	16 bit	16 bit
48K	768	× 512	512	× 384	6 of 8K × 8	8 bit	8 bit
56K	896	× 512	512	× 448	7 of 8K × 8	8 bit	8 bit
64K	1024	× 512	512	× 512	8 of 8K × 8	8 bit	8 bit
					16 bit	16 bit	
					2 of 32K × 8	8 bit	8 bit
						16 bit	16 bit

■ BLOCK DIAGRAM



**SED1351**

■ **ELECTRICAL CHARACTERISTICS**

● **SED1351F0A**

● **Absolute Maximum Ratings**

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.3 to 7.0	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	V
Output current/pin	I <sub>O</sub>	±10	mA
Power dissipation	P <sub>D</sub>	200	mW
Supply current	I <sub>DD</sub> /I <sub>SS</sub>	±40	mA
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C, 10s (at lead)	—

● **Recommended Operating Conditions**

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>		4.5	5.0	5.5	V
Input voltage	V <sub>I</sub>		V <sub>SS</sub>	—	V <sub>DD</sub>	V
Operating temperature	T <sub>opr</sub>		-20	—	75	°C

◦ DC Characteristics (F0A)

(Ta = -20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	I <sub>DD5</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>DD</sub> = Max, V <sub>SS</sub> , I <sub>OH</sub> = I <sub>OL</sub> = 0	—	—	100	μA
Input leakage current (Type 1)	I <sub>LI</sub>	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = V <sub>SS</sub>	-10	—	10	μA
High level input voltage 1 (OSC1)	V <sub>IH1</sub>	V <sub>DD</sub> = 5.5V	3.5	—	—	V
Low level input voltage 1 (OSC1)	V <sub>IL1</sub>	V <sub>DD</sub> = 4.5V	—	—	1.0	V
High level input voltage 2 (Type 2)	V <sub>IH2</sub>	V <sub>DD</sub> = 5.5V	2.0	—	—	V
Low level input voltage 2 (Type 2)	V <sub>IL2</sub>	V <sub>DD</sub> = 4.5V	—	—	0.8	V
High level input voltage 3 (Type 3)	V <sub>T+</sub>	V <sub>DD</sub> = 5.5V	4.0	—	—	V
Low level input voltage 3 (Type 3)	V <sub>T-</sub>	V <sub>DD</sub> = 4.5V	—	—	0.8	V
Hysteresis voltage (Type 3)	V <sub>H</sub>	V <sub>DD</sub> = 5V	0.3	—	—	V
High level output voltage 1 (Type 4)	V <sub>OH1</sub>	V <sub>DD</sub> = 4.5V I <sub>OH</sub> = -2mA I <sub>OL</sub> = 6mA	V <sub>DD</sub> - 0.4	—	—	V
Low level output voltage 1 (Type 4)	V <sub>OL1</sub>		—	—	V <sub>SS</sub> + 0.4	V
High level output voltage 2 (OSC2)	V <sub>OH2</sub>	V <sub>DD</sub> = 4.5V I <sub>OH</sub> = -50μA I <sub>OL</sub> = 50μA	V <sub>DD</sub> - 0.4	—	—	V
Low level output voltage 2 (OSC2)	V <sub>OL2</sub>		—	—	V <sub>SS</sub> + 0.4	V

**Note:**

- Type 1. MEMCS, MEMWR, MEMRD, IOCS, IOWR, IORD, MPUCLK, AB0 ~ AB15, BHE, MPUSEL, RESET, OSC  
 Type 2. MEMCS, MEMWR, MEMRD, IOCS, IOWR, IORD, MPUCLK, AB0 ~ AB15, BHE, DB0 ~ DB15, VD0 ~ VD15  
 Type 3. MPUSEL, RESET  
 Type 4. DB0 ~ DB15, READY, VA0 ~ VA15, VCS0 ~ VCS4, VD0 ~ VD15, VWE, XSCL, LP, WF, YD, UD0 ~ UD3, LD0 ~ LD3, LCDENB

**SED1351**

- SED1351FLA
- Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.3 to 7.0	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.5	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.5	V
Output current/pin	I <sub>O</sub>	±24	mA
Power dissipation	P <sub>D</sub>	200	mW
Supply current	I <sub>DD</sub> /I <sub>SS</sub>	±40	mA
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

- Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>		2.7	—	3.6	V
Input voltage	V <sub>I</sub>		V <sub>SS</sub>	—	V <sub>DD</sub>	V
Operating temperature	T <sub>opr</sub>		-20	—	75	°C



o DC Characteristics (FLB)

(Ta = -20 to 75°C)

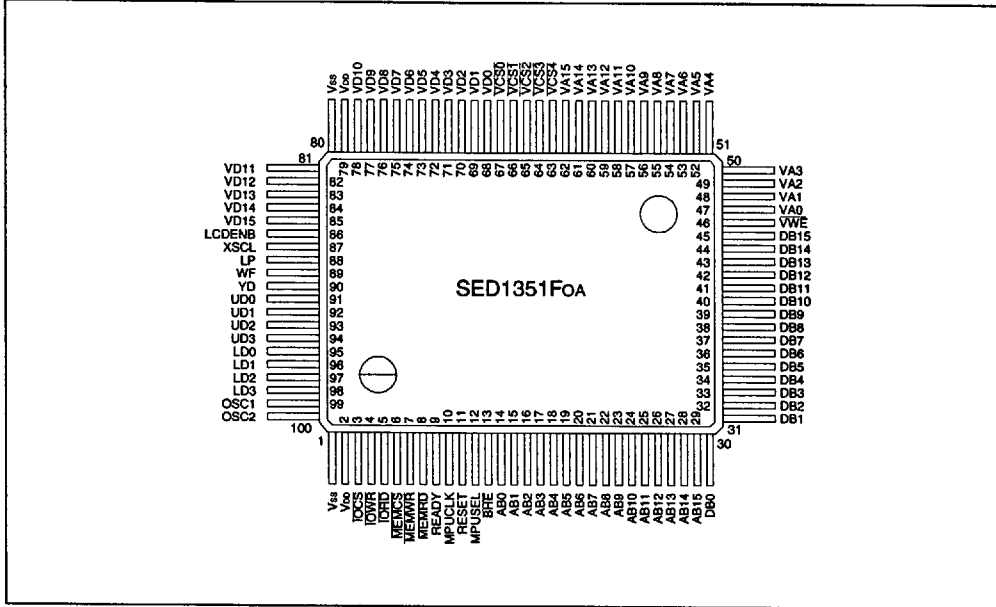
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	I <sub>DD5</sub>	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> , V <sub>DD</sub> = MAX, I <sub>OH</sub> = I <sub>OL</sub> = 0	—	—	30	μA
Input leakage current (Type 1)	I <sub>L</sub>	V <sub>DD</sub> = MAX, V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = V <sub>SS</sub>	-1	—	1	μA
High level input voltage 1 (OSC1)	V <sub>IH1</sub>	V <sub>DD</sub> = MAX	0.7V <sub>DD</sub>	—	—	V
Low level input voltage 1 (OSC1)	V <sub>IL1</sub>	V <sub>DD</sub> = MIN	—	—	0.2V <sub>DD</sub>	V
High level input voltage 2 (Type 2)	V <sub>IH2</sub>	V <sub>DD</sub> = MAX	0.7V <sub>DD</sub>	—	—	V
Low level input voltage 2 (Type 2)	V <sub>IL2</sub>	V <sub>DD</sub> = MIN	—	—	0.2V <sub>DD</sub>	V
High level input voltage 3 (Type 3)	V <sub>T+</sub>	V <sub>DD</sub> = MAX	0.8V <sub>DD</sub>	—	—	V
Low level input voltage 3 (Type 3)	V <sub>T-</sub>	V <sub>DD</sub> = MIN	—	—	0.2V <sub>DD</sub>	V
Hysteresis voltage (Type 3)	V <sub>H</sub>	V <sub>DD</sub> = TYP	0.3	—	—	V
High level output voltage 1 (Type 4)	V <sub>OH1</sub>	V <sub>DD</sub> = MIN I <sub>OH</sub> = -1.5mA I <sub>OL</sub> = 3mA	V <sub>DD</sub> - 0.3	—	—	V
Low level output voltage 1 (Type 4)	V <sub>OL1</sub>		—	—	V <sub>SS</sub> + 0.3	V
High level output voltage 2 (OSC2)	V <sub>OH2</sub>	V <sub>DD</sub> = MIN I <sub>OH</sub> = -50μA I <sub>OL</sub> = 50μA	V <sub>DD</sub> - 0.4	—	—	V
Low level output voltage 2 (OSC2)	V <sub>OL2</sub>		—	—	V <sub>SS</sub> + 0.4	V

Note:

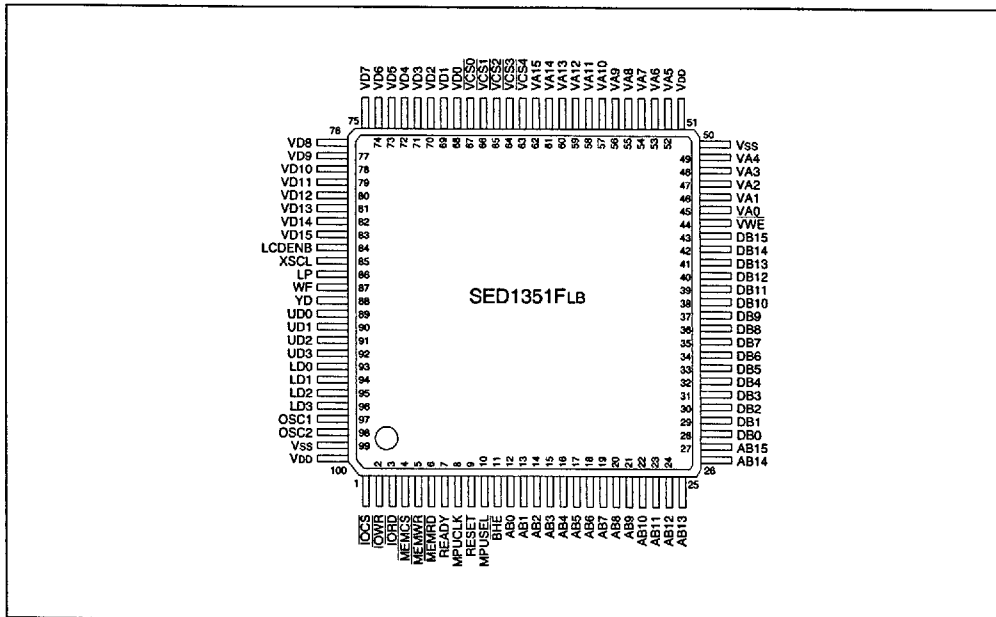
- Type 1. MEMCS, MEMWR, MEMRD, IOCS, IOWR, IORD, MPUCLK, AB0 ~ AB15, BHE, MPUSEL, RESET, OSC
- Type 2. MEMCS, MEMWR, MEMRD, IOCS, IOWR, IORD, MPUCLK, AB0 ~ AB15, BHE, DB0 ~ DB15, VD0 ~ VD15
- Type 3. MPUSEL, RESET
- Type 4. DB0 ~ DB15, READY, VA0 ~ VA15, VCS0 ~ VCS4, VD0 ~ VD15, VWE, XSCL, LP, WF, YD, UD0 ~ UD3, LD0 ~ LD3, LCDENB

**SED1351**

**■ PIN CONFIGURATION (FOA)**



**■ PIN CONFIGURATION (FLB)**



■ PIN DESCRIPTION

1. System Connector Terminals (at MPU)

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
DB0 to DB15	I/O	30 to 45	28 to 43		These pins are interfaced with the MPU data bus. When using an 8-bit MPU, connect DB8 to DB15 to VDD.
AB0 to AB15	I	14 to 29	12 to 27		These pins are interfaced with the MPU address bus. If multiplexed address signals are used, connect them via latch circuits. A control register is selected by AB0 to AB3. Correspondence of the MPU address bus to the VRAM address bus is such that $AB_i = VA_i$ (where $i$ is a pin number).
BHE	I	13	11		This signal is a bus high enable signal where a 16-bit MPU is used. It goes "L" (low) when an odd address is encountered. When using an 8-bit MPU configuration, connect the BHE pin to VDD.
$\overline{IOCS}$	I	3	1		This pin selects a control register contained in the SED1351. It is "L" active, and must be assigned to MPU I/O space.
$\overline{IOWR}$	I	4	2		This signal is used for writing data into a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an OUT instruction from the MPU.
$\overline{IORD}$	I	5	3		This signal is used for reading data from a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an IN instruction from the MPU.
MEMCS	I	6	4		This signal is used for selecting VRAM. It is "L" active, and must be assigned to MPU memory space.
MEMWR	I	7	5		This signal is used for writing data to the VRAM. It is "L" active, and must go "L" when it encounters a memory write instruction from the MPU.
MEMRD	I	8	6		This signal is used for reading data from the VRAM. It is "L" active, and must go "L" when it encounters a memory read instruction from the MPU.
READY	O	9	7		This signal requests the MPU to wait. It goes "L" by the falling edge of $\overline{IOCS}$ or MEMCS. It goes "H" by the rising edge of MPUCLK after completion of the SED1351 internal processing. Since READY is not a tri-state pin, it needed not be pulled up and must be connected directly to the READY (WAIT) terminal of the MPU.
MPUCLK	I	10	8		This pin accepts an MPU clock. The MPU wait state is cleared by the rising edge of MPUCLK.
MPUSEL	I	12	10		This signal is connected to either VDD or VSS for selection of an MPU. MPUSEL = V <sub>SS</sub> 8-bit MPU (e.g., Z80, V20, i8088) MPUSEL = V <sub>DD</sub> 16-bit MPU (e.g., V30, i8086)
RESET	I	11	9		The MPU reset signal comes to this pin. It is "H" active, and initializes a control register.

**Combinations of Control Pins**

IOCS	IOWR	IORD	MEMCS	MEMWR	MEMRD	Operation
1	*	*	1	*	*	Invalid
0	0	1	1	1	1	Write to control register
0	1	0	1	1	1	Read from control register
1	1	1	0	0	1	Write to VRAM
1	1	1	0	1	0	Read from VRAM

**Note:** Any combination other than those listed above will cause a system error.

- 1 = "H" (high)
- 0 = "L" (low)
- \* = Don't care

**2. VRAM Connector Terminals**

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
VD0 to VD15	I/O	68 to 78, 81 to 85	68 to 83		These pins are interfaced with the VRAM data bus. For a 16-bit MPU configuration, VD0 to VD7 must be connected to even addresses, and VD8 to VD15 to odd addresses. For an 8-bit configuration, VD8 to VD15 must be connected to VDD.
VA0 to VA12	O	47 to 59	45 to 49, 52 to 59		These pins are interfaced with the VRAM address bus and chip select pins.
VA13/ $\overline{\text{VCS7}}$ to VA15/ $\overline{\text{VCS5}}$	O	60 to 62	60 to 62		The SED1351 has chip select pins that can directly control eight 64K SRAMs (8K bytes each) or two 256K SRAMs (32K bytes) in the 64K VRAM space. See Technical Manual for details.
$\overline{\text{VCS0}}$ to $\overline{\text{VCS4}}$	O	67 to 63	67 to 63		
$\overline{\text{VWE}}$	O	46	44		This signal is used for writing data to the VRAM. It is "L" active, and must be connected to the WE pin of the VRAM.

**3. Oscillator Terminals**

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
OSC1	I	99	97		The OSC1 (input) and OSC2 (output) pins generate clocks for internal operation. They allow crystal oscillation and external clock input.
OSC2	O	100	98		

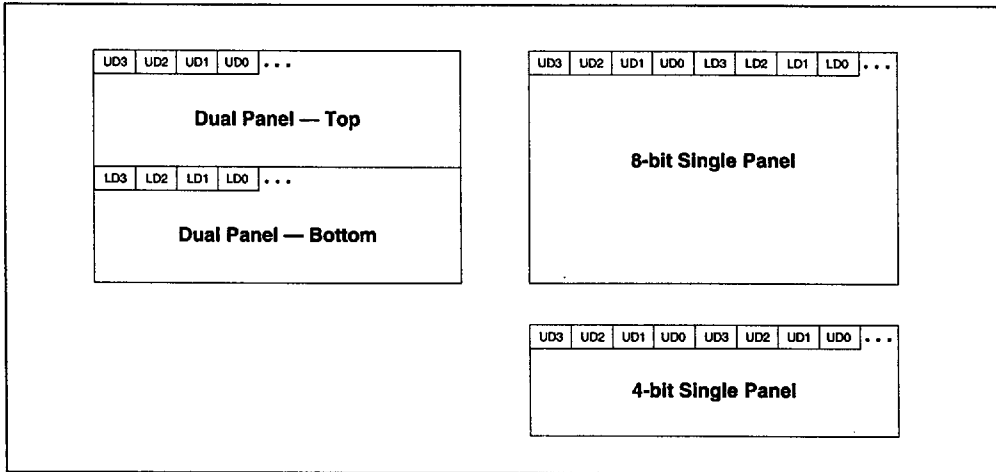
**4. Power Terminals**

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
V <sub>DD</sub>	—	2, 79	51, 100		The power supply pins include two V <sub>DDs</sub> and two V <sub>SSs</sub> . Apply +5V or +3V to V <sub>DD</sub> and 0V to V <sub>SS</sub> . A capacitor (4.7 $\mu$ F or more) must be connected near each pair of V <sub>DD</sub> /V <sub>SS</sub> pins.
V <sub>SS</sub>	—	1, 80	50, 99		

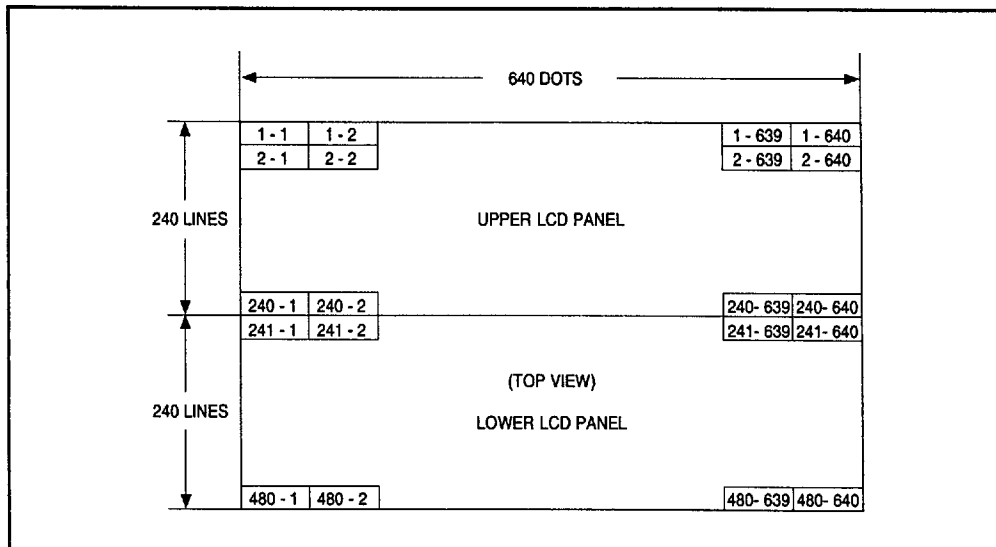
## 5. LCD Connector Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
UD0 to UD3	I/O	91 to 94	89 to 92		LCD display data. UD0 to UD3 are the upper panel display data in the signal panel or double panel drive panel mode. LD0/UD4 to LD3/UD7 are the lower panel display data in the double panel drive mode. UD0 to UD3, and LD0/UD4 to LD3/UD7 are used for 8-bit data transfer in the single panel drive mode.
LD0/UD4 to LD3/UD7	O	95 to 98	93 to 96		
XSCL	O	87	85		This signal is a shift clock for display data transfer. Take the UD0 to UD3, LD0/UD4 to LD3/UD7 display data into LCDs by the falling edge of XSCL.
LP	O	88	86		This pin provides both a display data latch pulse and a scan signal transfer clock. Upon completion of transferring the LCD data on one line, display data can be latched or a scan signal transferred by the falling edge of LP.
WF	O	89	87		This pin provides a frame signal used for LCD AC driving.
YD	O	90	88		This pin provides a scanning line start pulse. The signal is "H" active. Allow the scanning line drive IC to take in YD by the falling edge of LP.  The SED1351 has two lines of retracing; if two scanning line drive ICs are cascade-connected for the upper and lower panels in the double panel drive mode, two lines must be provided between the upper and lower scanning line drive outputs.
LCDENB	O	86	84		This pin provides the data which is set in bit 1 (D1) of the mode register (R1). LCDENB goes "L" when the system is reset; it can be effectively used for LCD power control.

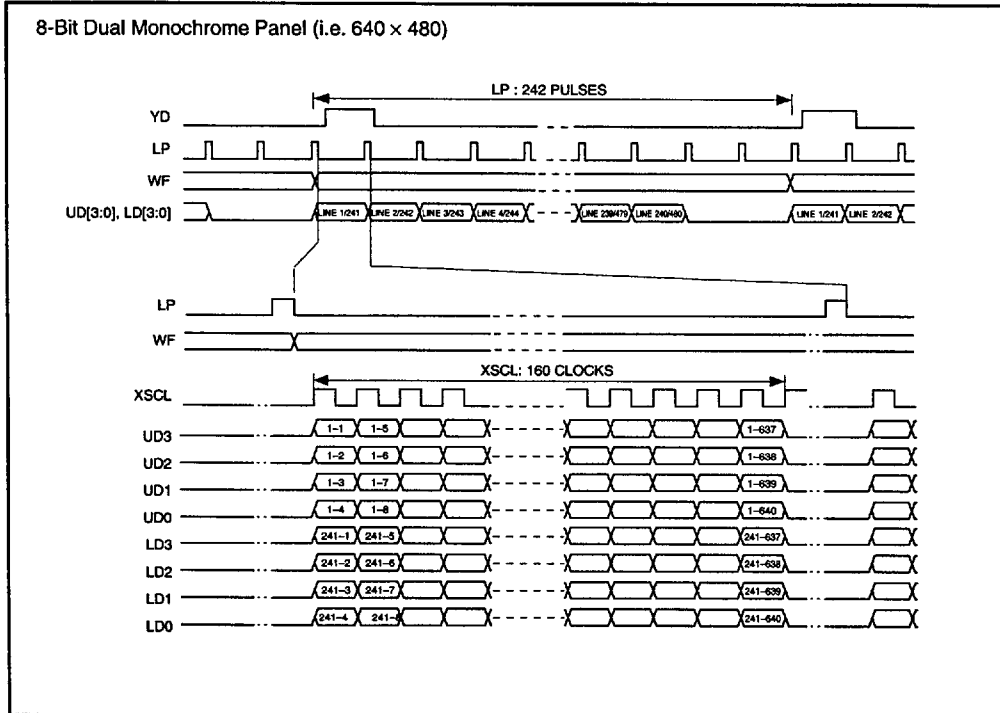
Illustrated below are the display data which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:



■ LCD PANEL PIXELS

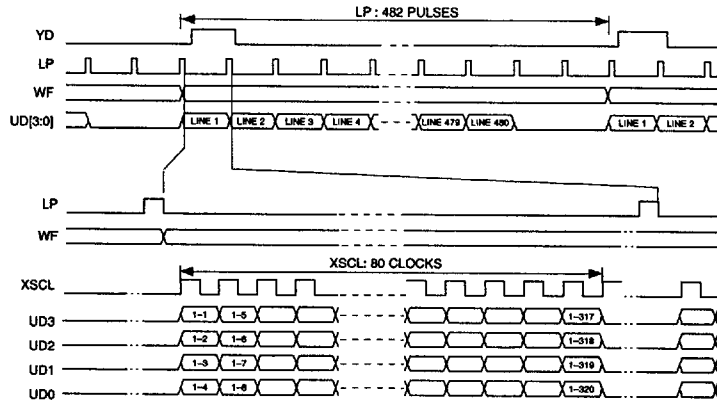


■ MONOCHROME LCD PANEL INTERFACE

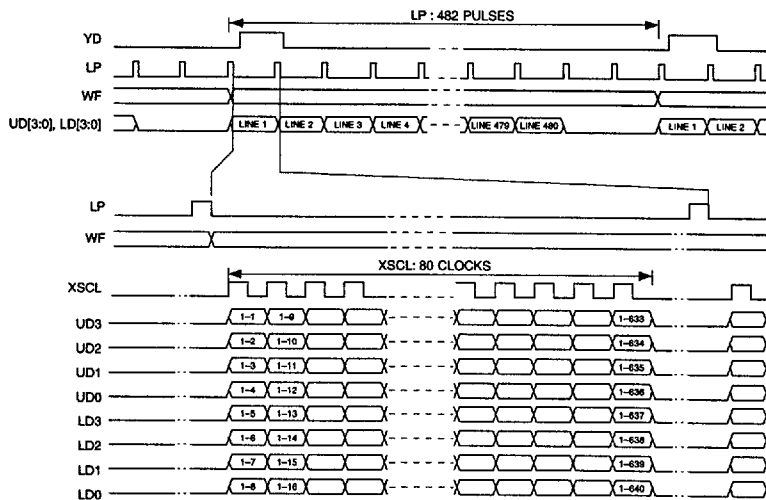


■ MONOCHROME LCD PANEL INTERFACE

4-Bit Single Monochrome Panel (i.e. 320 × 480)



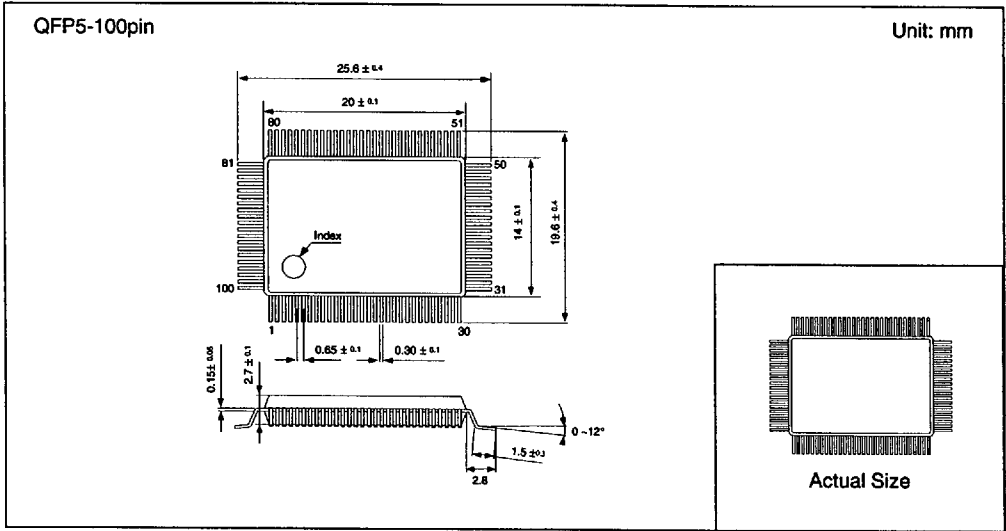
8-Bit Single Monochrome Panel (i.e. 640 × 480)



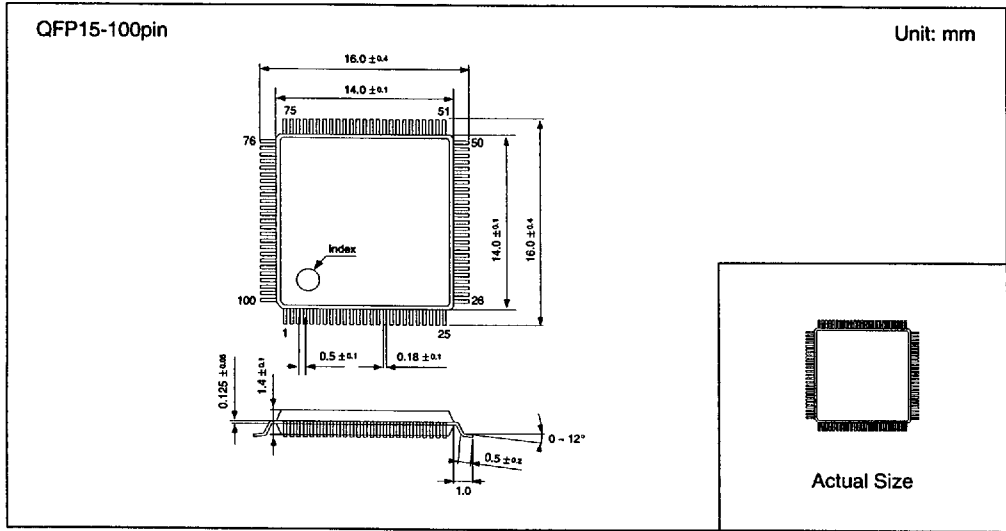


■ PACKAGE DIMENSIONS

● SED1351F0A



● SED1351FLB



***SED1351F<sub>0A/LB</sub>***  
***Graphics LCD Controller (GLC)***  
***Technical Manual***

***S-MOS Systems, Inc.***  
***September, 1995***  
***Version 0.2***

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***1.0***  
***Data Sheet***



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# 1.0 DATA SHEET

## DESCRIPTION

The SED1351F is a graphics LCD controller capable of controlling medium to large resolution displays. It transfers data from MPU to external frame buffer RAM and converts this data to display signals for LCD drivers. The SED1351F can display images with 4 gray shades and support display duty cycle as high as 1/1024.

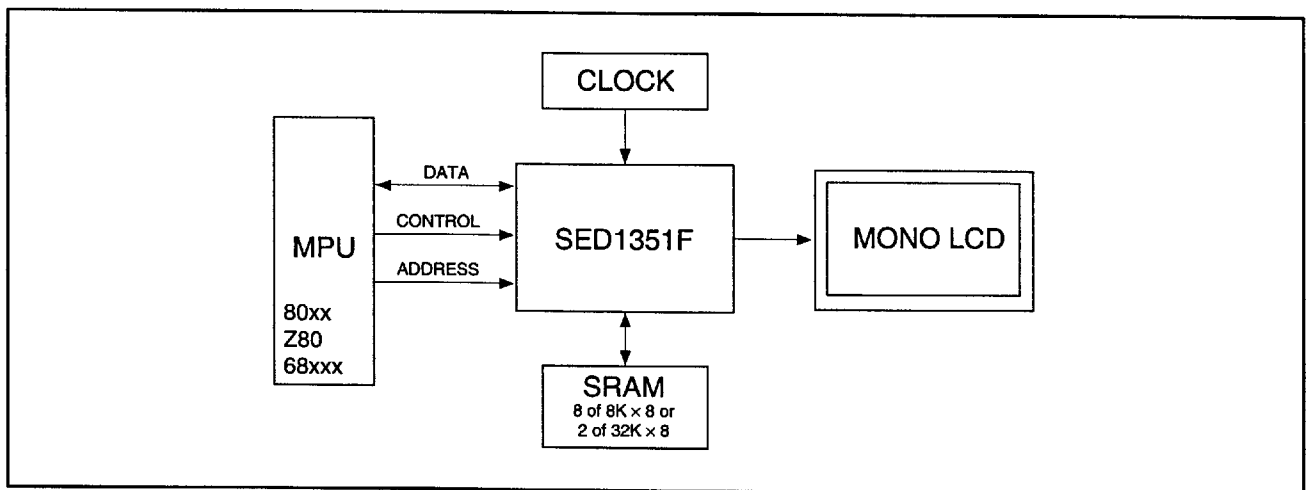
The SED1351F is designed to achieve high efficiency and data throughput to the LCD. It has a cycle steal mode which allows MPU to access frame buffer RAM without interfering with the display operation. The SED1351F can directly interface with up to eight 64K-bit SRAMs or two 256K-bit SRAMs.

The SED1351F can operate with either 5V or 3V power supply. The 5V version chip is the SED1351F0A and the 3V version chip is the SED1351FLB.

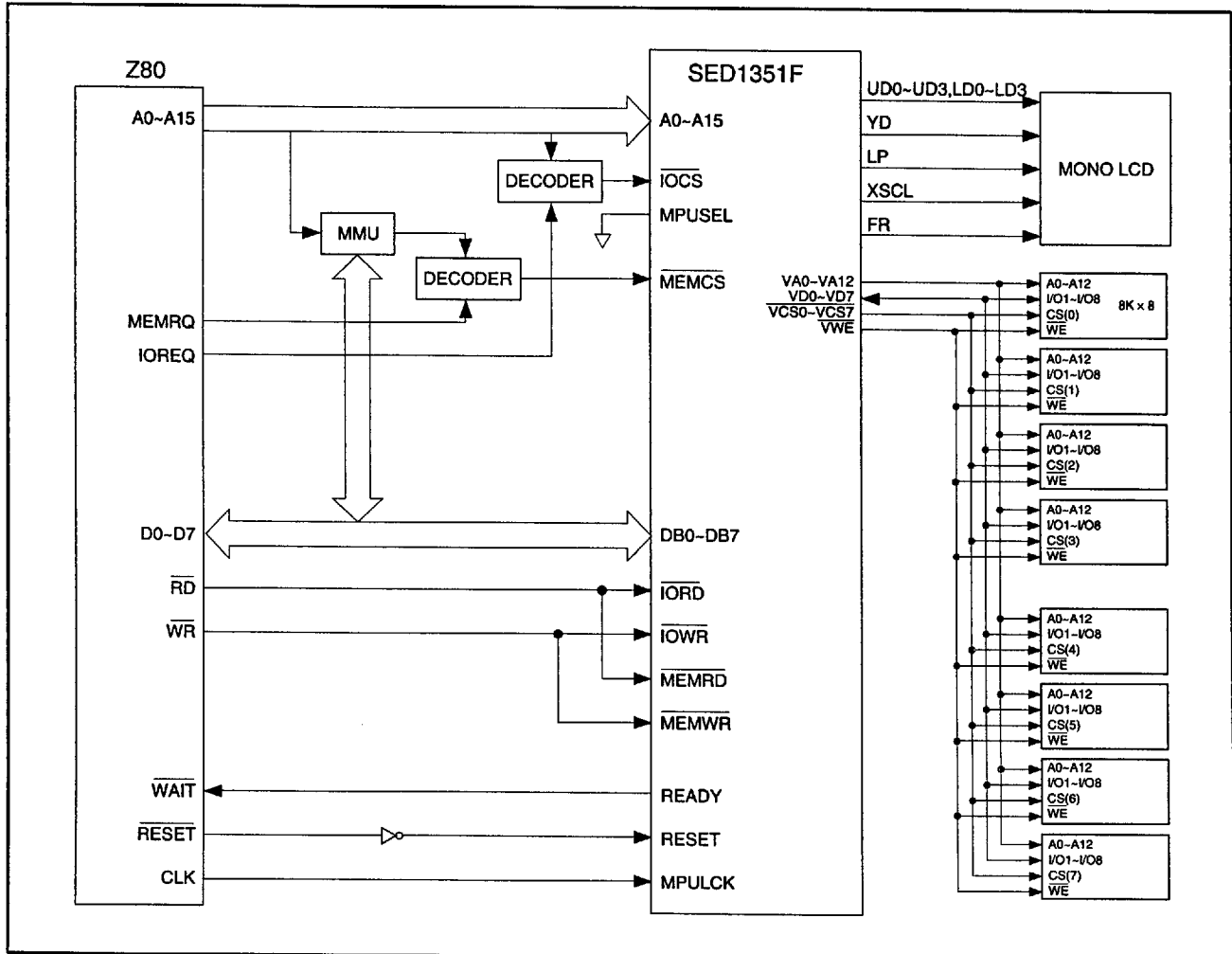
## FEATURES

- Low-power CMOS technology
- 8-bit or 16-bit MPU data interface
- Direct interface with 80xx, Z80 and 68xxx MPU
- 4- or 8-bit panel data bus for single panel and 4-bit bus for dual panel
- Support logical OR of layers and panel division
- Smooth vertical scrolling
- Virtual screen display up to 1024
- Binary mode (on/off only) generates black & white images
- Gray mode (on/off and two gray steps) generates images with 4 gray shades
- Maximum number of rows  
Binary mode ..... 2048  
Gray mode ..... 1024
- Maximum number of rows:  
Single panel ..... 1024  
Dual panel ..... 2048
- Maximum display sizes when 64K-byte SRAMs are used:  
Binary mode ..... 2048 × 256 / 1024 × 512  
Gray mode ..... 1024 × 256 / 512 × 512
- Available models:  
SED1351F0A ..... 5V, QFP5-100 pin  
SED1351FLB ..... 3V, QFP15-100 pin

## SYSTEM BLOCK DIAGRAM

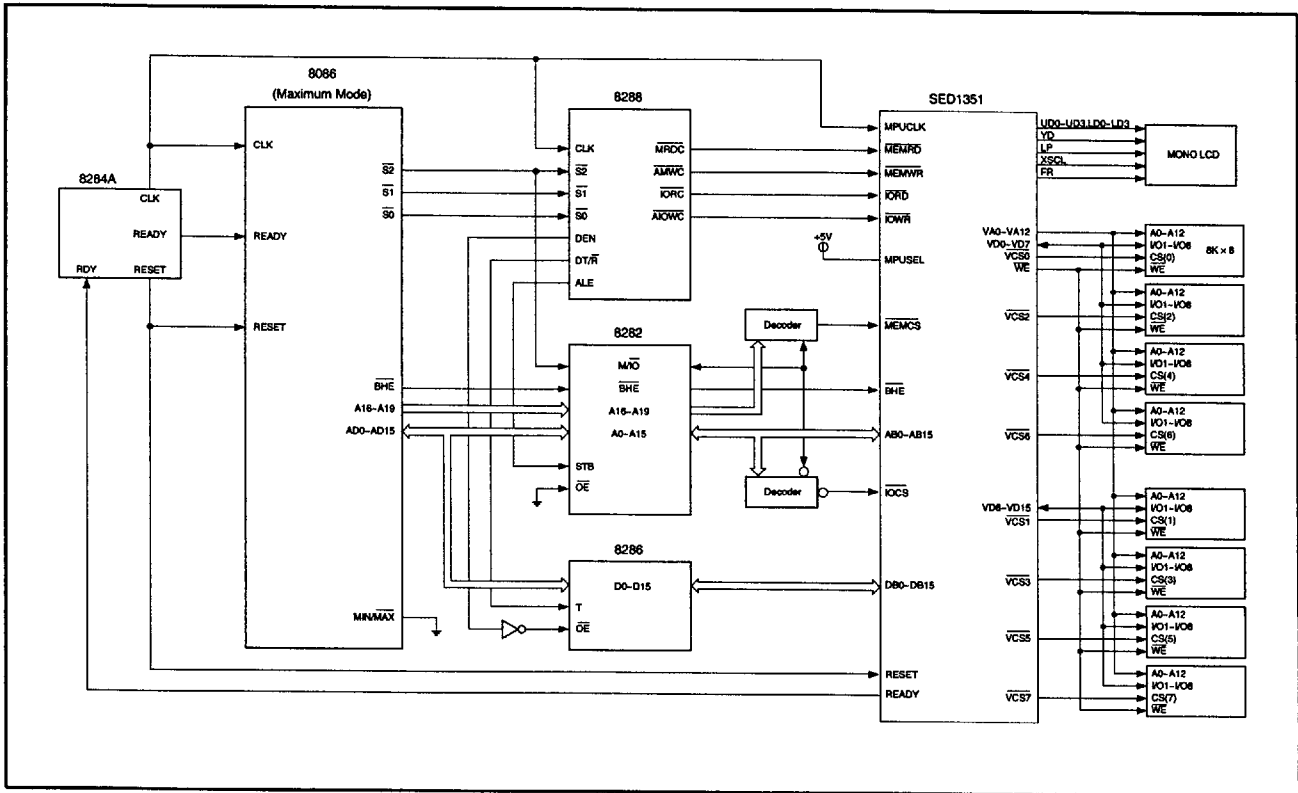


■ INTERFACE WITH 8-BIT MPU (Z-80) AND 64K-BIT SRAM (8 of 8K x 8)



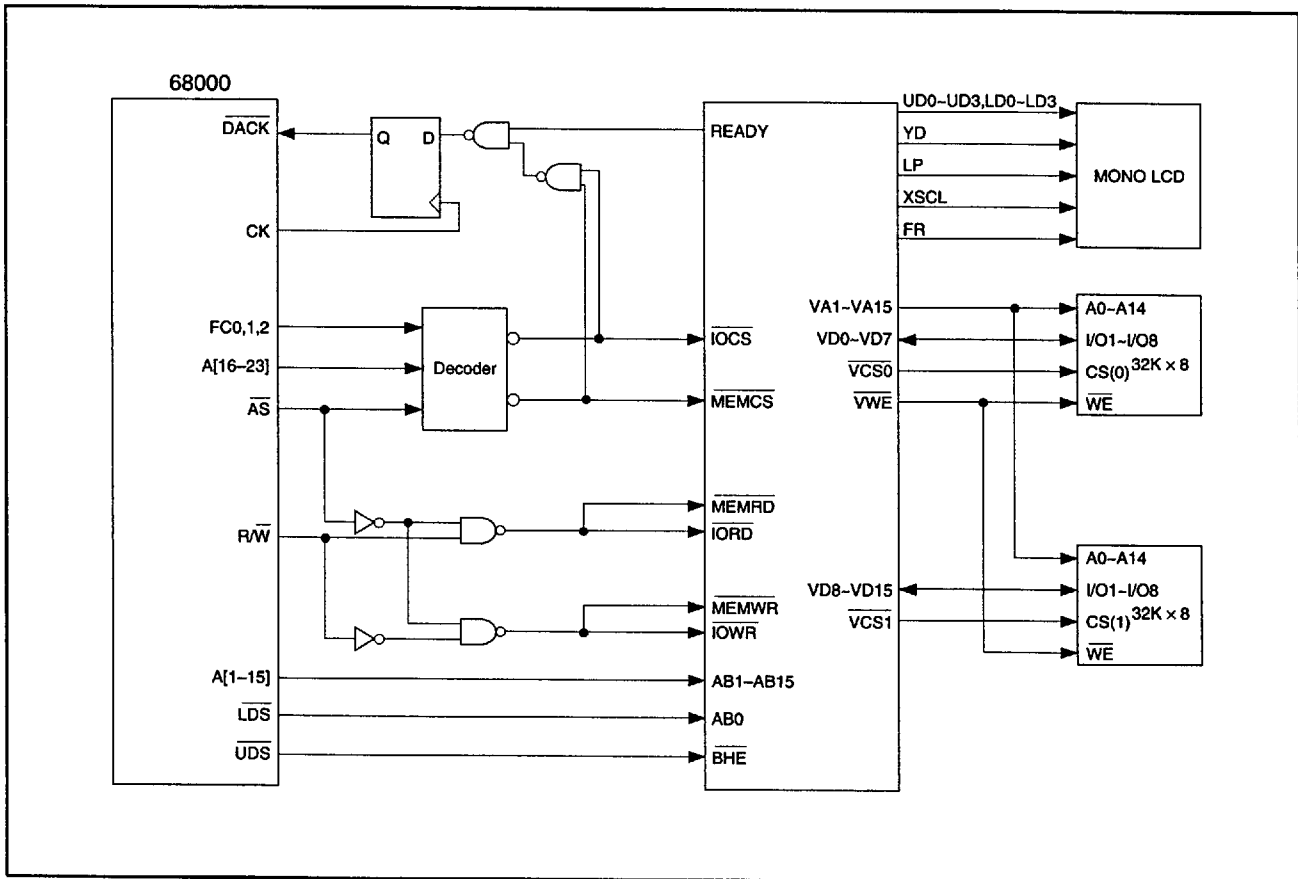
Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (8086) AND 64K-BIT SRAM (8 of 8K x 8)



Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (68000) AND 256K-BIT SRAM (2 of 32K x 8)

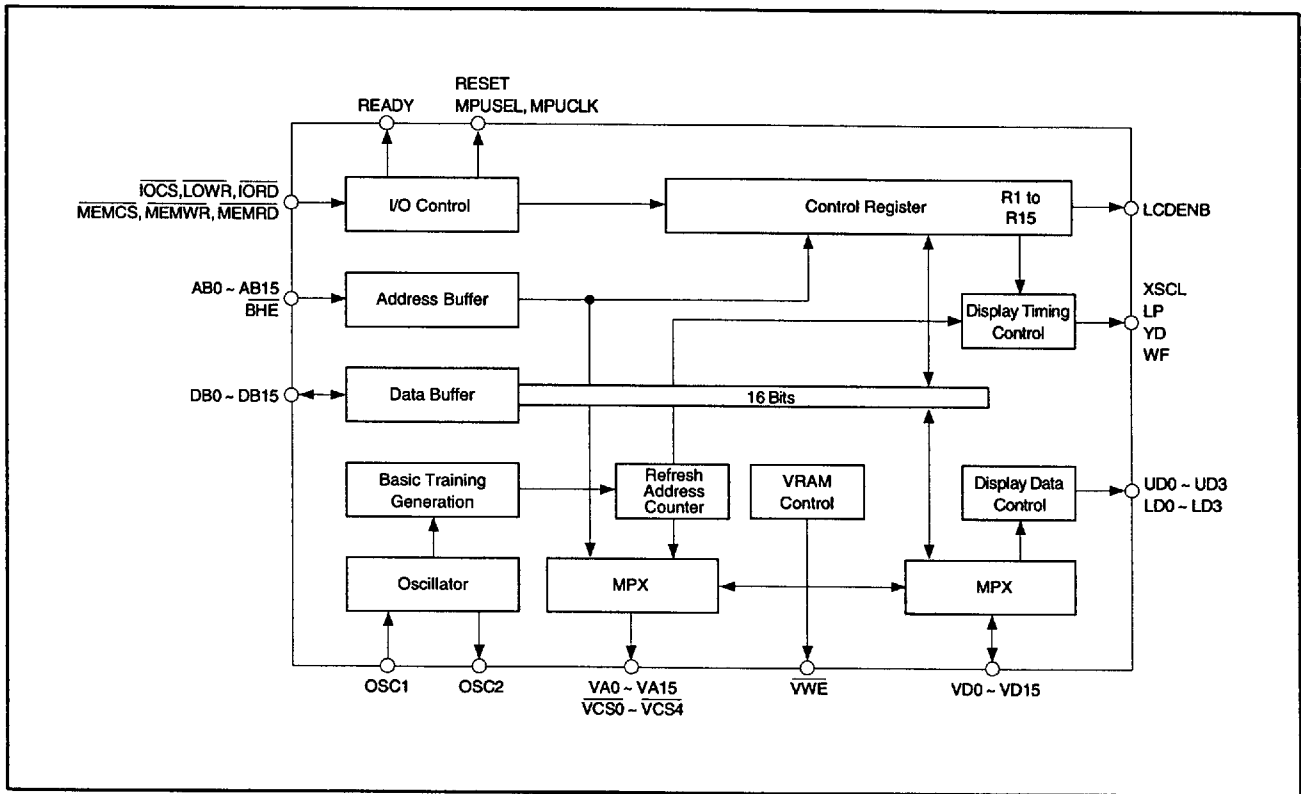


Note: Example implementation, actual may vary.

**■ SUPPORTED RESOLUTIONS**

Display RAM	Maximum Display Size				SRAM Type	CPU Interface	SRAM Interface
	Monochrome		4 Grayscale				
	X	Y	X	Y			
8K	256	× 256	256	× 128	1 of 8K × 8	8 bit	8 bit
16K	512	× 256	256	× 256	2 of 8K × 8	8 bit	8 bit
					16 bit	16 bit	
24K	512	× 384	384	× 256	3 of 8K × 8	8 bit	8 bit
32K	512	× 512	512	× 256	4 of 8K × 8	8 bit	8 bit
					16 bit	16 bit	
					1 of 32K × 8	8 bit	8 bit
48K	768	× 512	512	× 384	6 of 8K × 8	8 bit	8 bit
					16 bit	16 bit	
56K	896	× 512	512	× 448	7 of 8K × 8	8 bit	8 bit
64K	1024	× 512	512	× 512	8 of 8K × 8	8 bit	8 bit
					16 bit	16 bit	
					2 of 32K × 8	8 bit	8 bit
					16 bit	16 bit	

■ BLOCK DIAGRAM



## ■ ELECTRICAL CHARACTERISTICS

### ● SED1351F0A

#### ○ Absolute Maximum Ratings (F0A)

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	V <sub>SS</sub> – 0.3 to 7.0	
Input voltage	V <sub>I</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
Output current/pin	I <sub>O</sub>	±10	mA
Power dissipation	P <sub>D</sub>	200	mW
Supply current	I <sub>DD</sub> /I <sub>SS</sub>	±40	mA
Storage temperature	T <sub>stg</sub>	–65 to 150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C, 10s (at lead)	—

#### ● Recommended Operating Conditions (F0A)

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>		4.5	5.0	5.5	V
Input voltage	V <sub>I</sub>		V <sub>SS</sub>	—	V <sub>DD</sub>	V
Operating temperature	T <sub>opr</sub>		–20	—	75	°C



○ DC Characteristics (FOA)

( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	$I_{DD5}$	$V_{IN} = V_{DD}$ , $V_{DD} = \text{Max}$ , $V_{SS}$ , $I_{OH} = I_{OL} = 0$	—	—	100	$\mu\text{A}$
Input leakage current (Type 1)	$I_{LI}$	$V_{DD} = 5.5\text{V}$ , $V_{IH} = V_{DD}$ , $V_{IL} = V_{SS}$	-10	—	10	$\mu\text{A}$
High level input voltage 1 (OSC1)	$V_{IH1}$	$V_{DD} = 5.5\text{V}$	3.5	—	—	V
Low level input voltage 1 (OSC1)	$V_{IL1}$	$V_{DD} = 4.5\text{V}$	—	—	1.0	V
High level input voltage 2 (Type 2)	$V_{IH2}$	$V_{DD} = 5.5\text{V}$	2.0	—	—	V
Low level input voltage 2 (Type 2)	$V_{IL2}$	$V_{DD} = 4.5\text{V}$	—	—	0.8	V
High level input voltage 3 (Type 3)	$V_{T+}$	$V_{DD} = 5.5\text{V}$	4.0	—	—	V
Low level input voltage 3 (Type 3)	$V_{T-}$	$V_{DD} = 4.5\text{V}$	—	—	0.8	V
Hysteresis voltage (Type 3)	$V_H$	$V_{DD} = 5\text{V}$	0.3	—	—	V
High level output voltage 1 (Type 4)	$V_{OH1}$	$V_{DD} = 4.5\text{V}$ $I_{OH} = -2\text{mA}$ $I_{OL} = 6\text{mA}$	$V_{DD}$ - 0.4	—	—	V
Low level output voltage 1 (Type 4)	$V_{OL1}$		—	—	$V_{SS}$ + 0.4	V
High level output voltage 2 (OSC2)	$V_{OH2}$	$V_{DD} = 4.5\text{V}$ $I_{OH} = -50\mu\text{A}$ $I_{OL} = 50\mu\text{A}$	$V_{DD}$ - 0.4	—	—	V
Low level output voltage 2 (OSC2)	$V_{OL2}$		—	—	$V_{SS}$ + 0.4	V

**Note:**

Type 1.  $\overline{\text{MEMCS}}$ ,  $\overline{\text{MEMWR}}$ ,  $\overline{\text{MEMRD}}$ ,  $\overline{\text{IOCS}}$ ,  $\overline{\text{IOWR}}$ ,  $\overline{\text{IORD}}$ ,  $\text{MPUCLK}$ ,  $\text{AB0} \sim \text{AB15}$ ,  $\overline{\text{BHE}}$ ,  $\text{MPUSEL}$ ,  $\text{RESET}$ ,  $\text{OSC}$

Type 2.  $\overline{\text{MEMCS}}$ ,  $\overline{\text{MEMWR}}$ ,  $\overline{\text{MEMRD}}$ ,  $\overline{\text{IOCS}}$ ,  $\overline{\text{IOWR}}$ ,  $\overline{\text{IORD}}$ ,  $\text{MPUCLK}$ ,  $\text{AB0} \sim \text{AB15}$ ,  $\overline{\text{BHE}}$ ,  $\text{DB0} \sim \text{DB15}$ ,  $\text{VD0} \sim \text{VD15}$

Type 3.  $\text{MPUSEL}$ ,  $\text{RESET}$

Type 4.  $\text{DB0} \sim \text{DB15}$ ,  $\text{READY}$ ,  $\text{VA0} \sim \text{VA15}$ ,  $\overline{\text{VCS0}} \sim \overline{\text{VCS4}}$ ,  $\text{VD0} \sim \text{VD15}$ ,  $\overline{\text{VWE}}$ ,  $\text{XSCL}$ ,  $\text{LP}$ ,  $\text{WF}$ ,  $\text{YD}$ ,  $\text{UD0} \sim \text{UD3}$ ,  $\text{LD0} \sim \text{LD3}$ ,  $\text{LCDENB}$

## ■ ELECTRICAL CHARACTERISTICS

### ● SED1351FLB

#### ○ Absolute Maximum Ratings (FLB)

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	V <sub>SS</sub> – 0.3 to 7.0	
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.5	V
Output voltage	V <sub>OUT</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.5	V
Output current/pin	I <sub>OUT</sub>	±24	mA
Power dissipation	P <sub>D</sub>	200	mW
Supply current	I <sub>DD</sub> /I <sub>SS</sub>	±40	mA
Storage temperature	T <sub>stg</sub>	–65 to 150	°C

#### ● Recommended Operating Conditions (FLB)

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>		2.7	—	3.6	V
Input voltage	V <sub>IN</sub>		V <sub>SS</sub>	—	V <sub>DD</sub>	V
Operating temperature	T <sub>opr</sub>		–20	—	75	°C

o DC Characteristics (FLB)

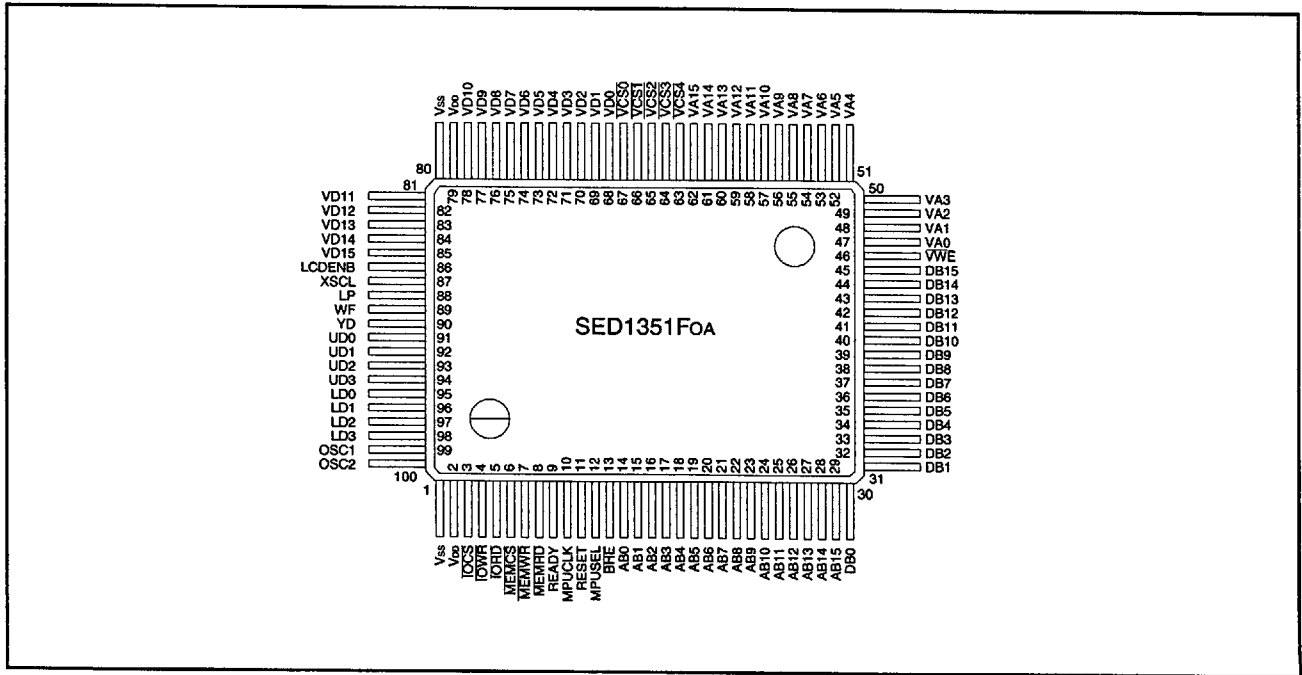
( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	$I_{DD5}$	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = \text{MAX}$ $I_{OH} = I_{OL} = 0$	—	—	30	$\mu\text{A}$
Input leakage current (Type 1)	$I_L$	$V_{DD} = \text{MAX}$ $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	-1	—	1	$\mu\text{A}$
"H" level input voltage (OSC1)	$V_{IH1}$	$V_{DD} = \text{MAX}$	$0.7 V_{DD}$	—	—	V
"L" level input voltage (OSC1)	$V_{IL1}$	$V_{DD} = \text{MIN}$	—	—	$0.2 V_{DD}$	V
"H" level input voltage (Type 2)	$V_{IH2}$	$V_{DD} = \text{MAX}$	$0.7 V_{DD}$	—	—	V
"L" level input voltage (Type 2)	$V_{IL2}$	$V_{DD} = \text{MIN}$	—	—	$0.2 V_{DD}$	V
"H" level input voltage (Type 3)	$V_{T+}$	$V_{DD} = \text{MAX}$	$0.8 V_{DD}$	—	—	V
"L" level input voltage (Type 3)	$V_{T-}$	$V_{DD} = \text{MIN}$	—	—	$0.2 V_{DD}$	V
Hysteresis voltage (Type 3)	$V_H$	$V_{DD} = \text{TYP}$	0.3	—	—	V
"H" level output voltage (Type 4)	$V_{OH1}$	$V_{DD} = \text{MIN}$ $I_{OH} = -1.5\text{mA}$	$V_{DD} - 0.3$	—	—	V
"L" level output voltage (Type 4)	$V_{OL1}$	$I_{OL} = 3\text{mA}$	—	—	$V_{SS} + 0.3$	V
"H" level output voltage (OSC2)	$V_{OH2}$	$V_{DD} = \text{MIN}$ $I_{OH} = -50\mu\text{A}$	$V_{DD} - 0.4$	—	—	V
"L" level output voltage (OSC2)	$V_{OL2}$	$I_{OL} = 50\mu\text{A}$	—	—	$V_{SS} + 0.4$	V

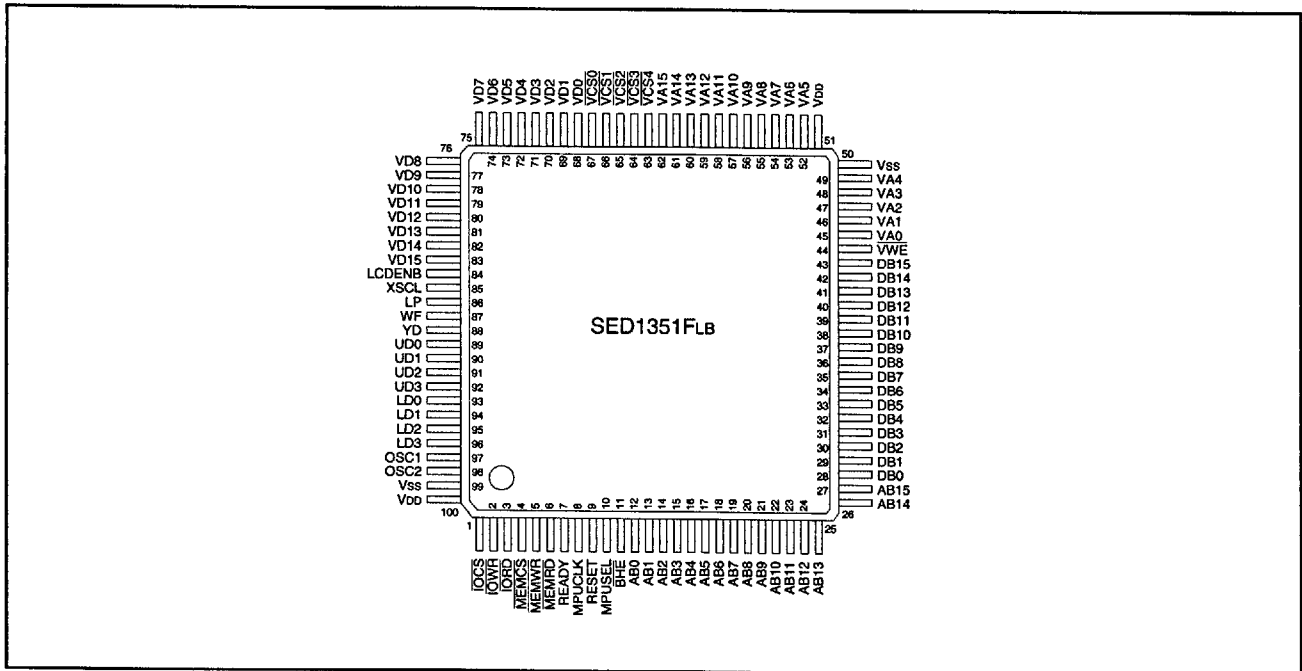
Note:

- Type 1.  $\overline{\text{MEMCS}}$ ,  $\overline{\text{MEMWR}}$ ,  $\overline{\text{MEMRD}}$ ,  $\overline{\text{IOCS}}$ ,  $\overline{\text{IOWR}}$ ,  $\overline{\text{IOR}}$ ,  $\overline{\text{MPUCLK}}$ ,  $\overline{\text{AB0}}$  ~  $\overline{\text{AB15}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{MPUSEL}}$ ,  $\overline{\text{RESET}}$ ,  $\overline{\text{OSC}}$   
Type 2.  $\overline{\text{MEMCS}}$ ,  $\overline{\text{MEMWR}}$ ,  $\overline{\text{MEMRD}}$ ,  $\overline{\text{IOCS}}$ ,  $\overline{\text{IOWR}}$ ,  $\overline{\text{IOR}}$ ,  $\overline{\text{MPUCLK}}$ ,  $\overline{\text{AB0}}$  ~  $\overline{\text{AB15}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{DB0}}$  ~  $\overline{\text{DB15}}$ ,  $\overline{\text{VD0}}$  ~  $\overline{\text{VD15}}$   
Type 3.  $\overline{\text{MPUSEL}}$ ,  $\overline{\text{RESET}}$   
Type 4.  $\overline{\text{DB0}}$  ~  $\overline{\text{DB15}}$ ,  $\overline{\text{READY}}$ ,  $\overline{\text{VA0}}$  ~  $\overline{\text{VA15}}$ ,  $\overline{\text{VCS0}}$  ~  $\overline{\text{VCS4}}$ ,  $\overline{\text{VD0}}$  ~  $\overline{\text{VD15}}$ ,  $\overline{\text{VWE}}$ ,  $\overline{\text{XSCL}}$ ,  $\overline{\text{LP}}$ ,  $\overline{\text{WF}}$ ,  $\overline{\text{YD}}$ ,  $\overline{\text{UD0}}$  ~  $\overline{\text{UD3}}$ ,  $\overline{\text{LD0}}$  ~  $\overline{\text{LD3}}$ ,  $\overline{\text{LCDENB}}$

■ PIN CONFIGURATION (FOA)



■ PIN CONFIGURATION (FLB)



## ■ PIN DESCRIPTION

### 1. System Connector Terminals (at MPU)

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
DB0 to DB15	I/O	30 to 45	28 to 43		These pins are interfaced with the MPU data bus. When using an 8-bit MPU, connect DB8 to DB15 to VDD.
AB0 to AB15	I	14 to 29	12 to 27		These pins are interfaced with the MPU address bus. If multiplexed address signals are used, connect them via latch circuits. A control register is selected by AB0 to AB3. Correspondence of the MPU address bus to the VRAM address bus is such that $AB_i = VA_i$ (where $i$ is a pin number).
$\overline{BHE}$	I	13	11		This signal is a bus high enable signal where a 16-bit MPU is used. It goes "L" (low) when an odd address is encountered. When using an 8-bit MPU configuration, connect the BHE pin to VDD.
$\overline{IOCS}$	I	3	1		This pin selects a control register contained in the SED1351. It is "L" active, and must be assigned to MPU I/O space.
$\overline{IOWR}$	I	4	2		This signal is used for writing data into a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an OUT instruction from the MPU.
$\overline{IORD}$	I	5	3		This signal is used for reading data from a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an IN instruction from the MPU.
$\overline{MEMCS}$	I	6	4		This signal is used for selecting VRAM. It is "L" active, and must be assigned to MPU memory space.
$\overline{MEMWR}$	I	7	5		This signal is used for writing data to the VRAM. It is "L" active, and must go "L" when it encounters a memory write instruction from the MPU.
$\overline{MEMRD}$	I	8	6		This signal is used for reading data from the VRAM. It is "L" active, and must go "L" when it encounters a memory read instruction from the MPU.

## 1. System Connector Terminals (at MPU) (continued)

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
READY	O	9	7		This signal requests the MPU to wait. It goes "L" by the falling edge of IOCS or MEMCS. It goes "H" by the rising edge of MPUCLK after completion of the SED1351 internal processing. Since READY is not a tri-state pin, it needed not be pulled up and must be connected directly to the READY (WAIT) terminal of the MPU.
MPUCLK	I	10	8		This pin accepts an MPU clock. The MPU wait state is cleared by the rising edge of MPUCLK.
MPUSEL	I	12	10		This signal is connected to either VDD or VSS for selection of an MPU. MPUSEL = VSS ..... 8-bit MPU (e.g., Z80, V20, i8088) MPUSEL = VDD ..... 16-bit MPU (e.g., V30, i8086)
RESET	I	11	9		The MPU reset signal comes to this pin. It is "H" active, and initializes a control register.

### Combinations of Control Pins

IOCS	IOWR	IORD	MEMCS	MEMWR	MEMRD	Operation
1	*	*	1	*	*	Invalid
0	0	1	1	1	1	Write to control register
0	1	0	1	1	1	Read from control register
1	1	1	0	0	1	Write to VRAM
1	1	1	0	1	0	Read from VRAM

**Note:** Any combination other than those listed above will cause a system error.

1 = "H" (high)

0 = "L" (low)

\* = Don't care

## 2. VRAM Connector Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
VD0 to VD15	I/O	68 to 78, 81 to 85	68 to 83		These pins are interfaced with the VRAM data bus. For a 16-bit MPU configuration, VD0 to VD7 must be connected to even addresses, and VD8 to VD15 to odd addresses. For an 8-bit configuration, VD8 to VD15 must be connected to VDD.
VA0 to VA12	O	47 to 59	45 to 49, 52 to 59		These pins are interfaced with the VRAM address bus and chip select pins.
VA13/VCS7 to VA15/VCS5	O	60 to 62	60 to 62		The SED1351 has chip select pins that can directly control eight 64K SRAMs (8K bytes each) or two 256K SRAMs (32K bytes) in the 64K VRAM space. See Technical Manual for details.
VCS0 to VCS4	O	67 to 63	67 to 63		
VWE	O	46	44		This signal is used for writing data to the VRAM. It is "L" active, and must be connected to the WE pin of the VRAM.

## 3. Oscillator Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
OSC1	I	99	97		The OSC1 (input) and OSC2 (output) pins generate clocks for internal operation. They allow crystal oscillation and external clock input.
OSC2	O	100	98		

## 4. Power Terminals

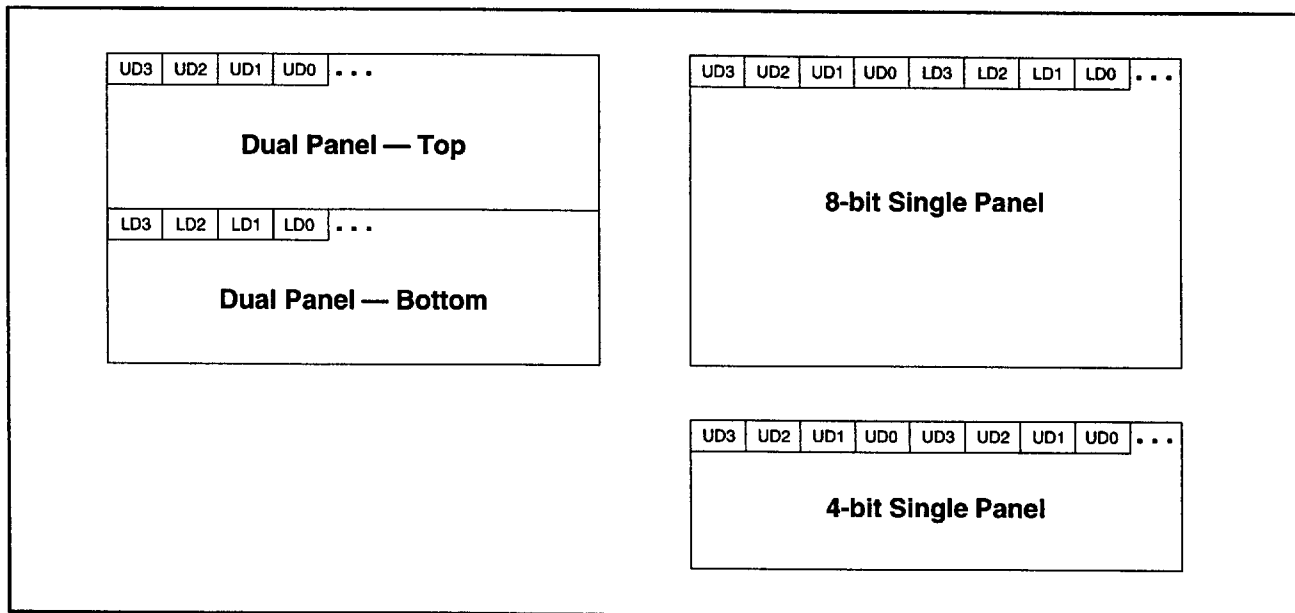
Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
VDD	—	2, 79	51, 100		The power supply pins include two VDDs and two VSSs. Apply +5V or +3V to VDD and 0V to VSS. A capacitor (4.7 $\mu$ F or more) must be connected near each pair of VDD/VSS pins.
VSS	—	1, 80	50, 99		

## 5. LCD Connector Terminals

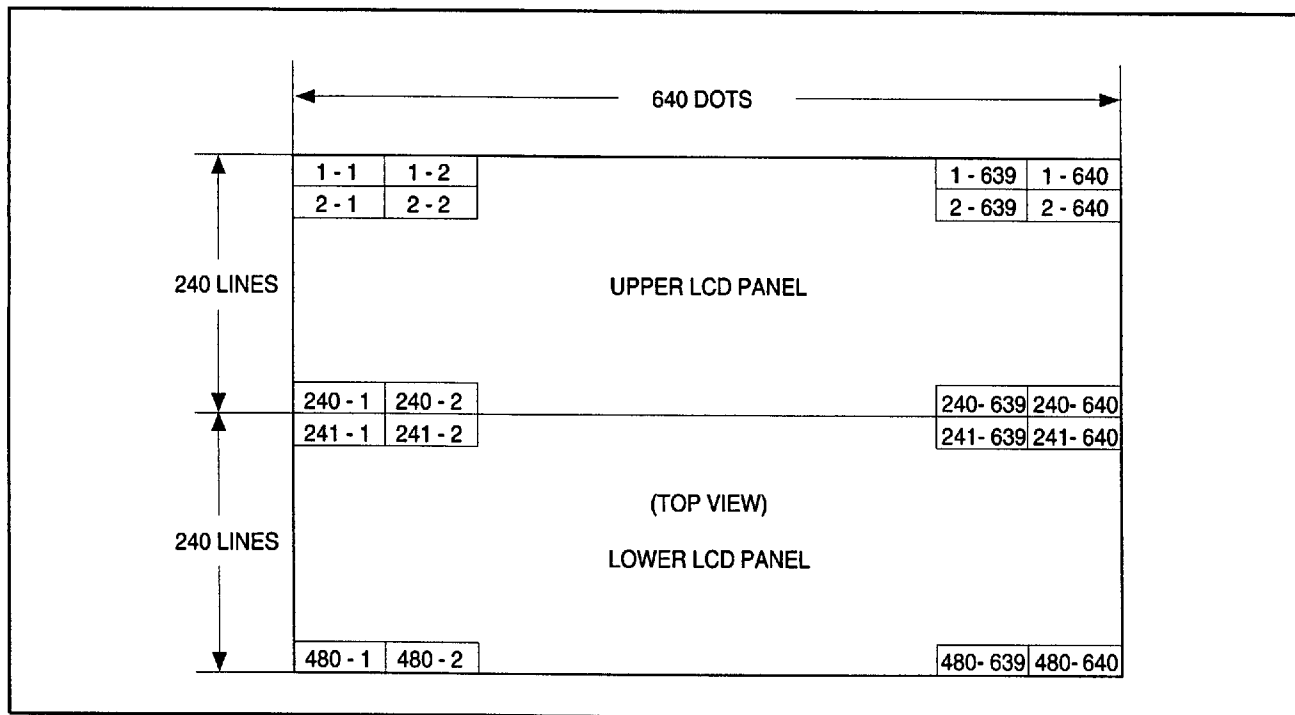
Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
UD0 to UD3	I/O	91 to 94	89 to 92		LCD display data. UD0 to UD3 are the upper panel display data in the signal panel or double panel drive panel mode. LD0/UD4 to LD3/UD7 are the lower panel display data in the double panel drive mode. UD0 to UD3, and LD0/UD4 to LD3/UD7 are used for 8-bit data transfer in the single panel drive mode.
LD0/UD4 to LD3/UD7	O	95 to 98	93 to 96		
XSCL	O	87	85		This signal is a shift clock for display data transfer. Take the UD0 to UD3, LD0/UD4 to LD3/UD7 display data into LCDs by the falling edge of XSCL.
LP	O	88	86		This pin provides both a display data latch pulse and a scan signal transfer clock. Upon completion of transferring the LCD data on one line, display data can be latched or a scan signal transferred by the falling edge of LP.
WF	O	89	87		This pin provides a frame signal used for LCD AC driving.
YD	O	90	88		This pin provides a scanning line start pulse. The signal is "H" active. Allow the scanning line drive IC to take in YD by the falling edge of LP.  The SED1351 has two lines of retracing; if two scanning line drive ICs are cascade-connected for the upper and lower panels in the double panel drive mode, two lines must be provided between the upper and lower scanning line drive outputs.
LCDENB	O	86	84		This pin provides the data which is set in bit 1 (D1) of the mode register (R1). LCDENB goes "L" when the system is reset; it can be effectively used for LCD power control.



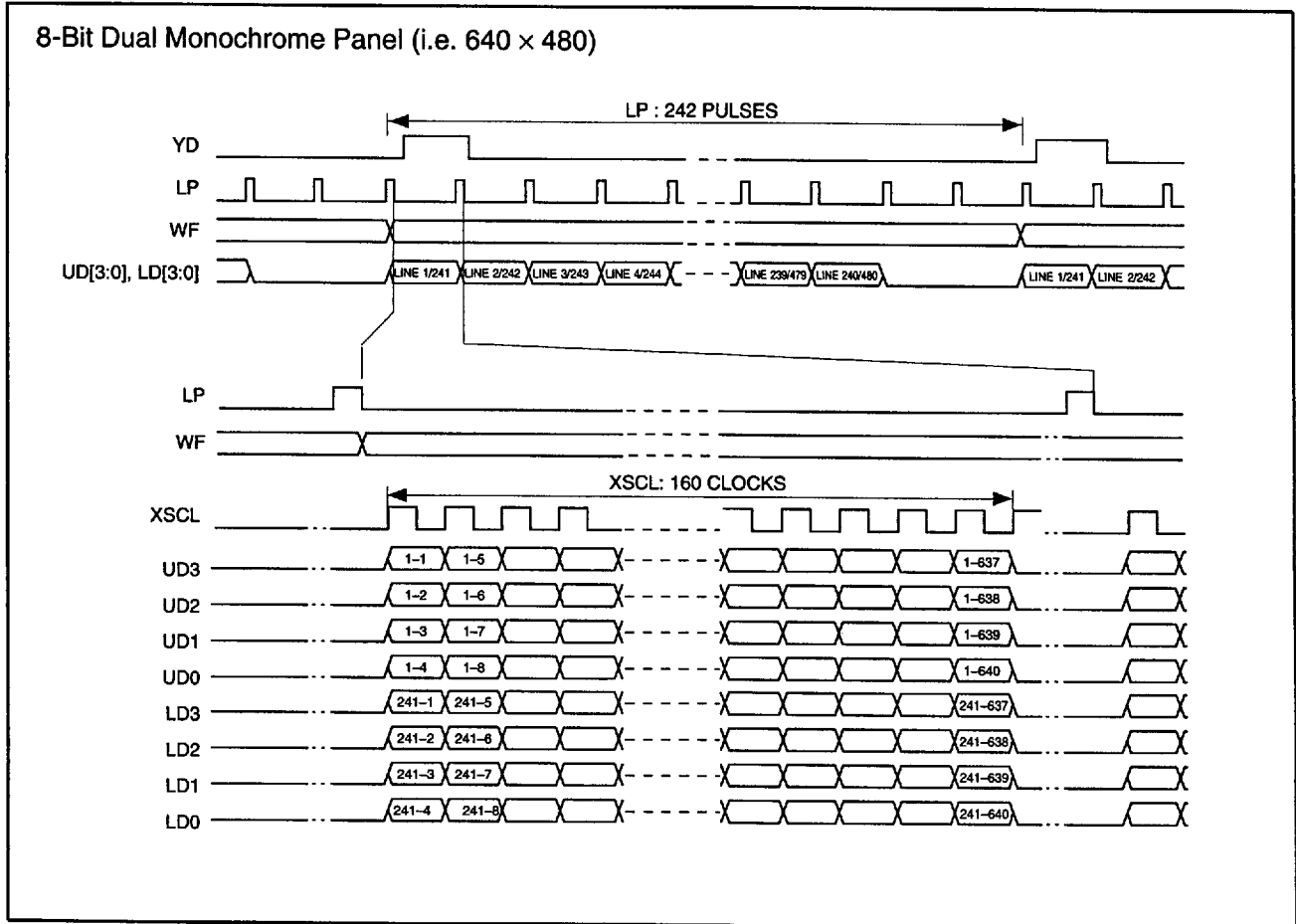
Illustrated below are the display data which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:



■ LCD PANEL PIXELS

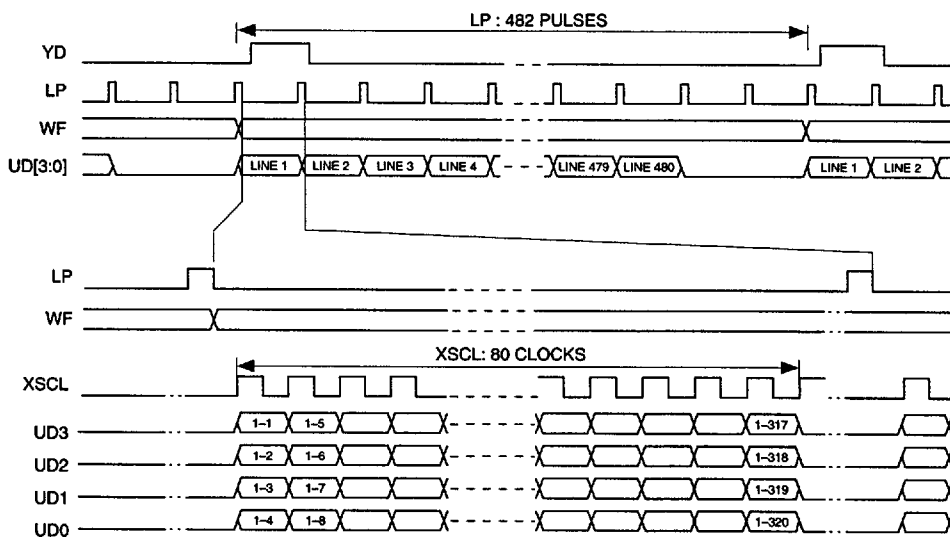


■ MONOCHROME LCD PANEL INTERFACE

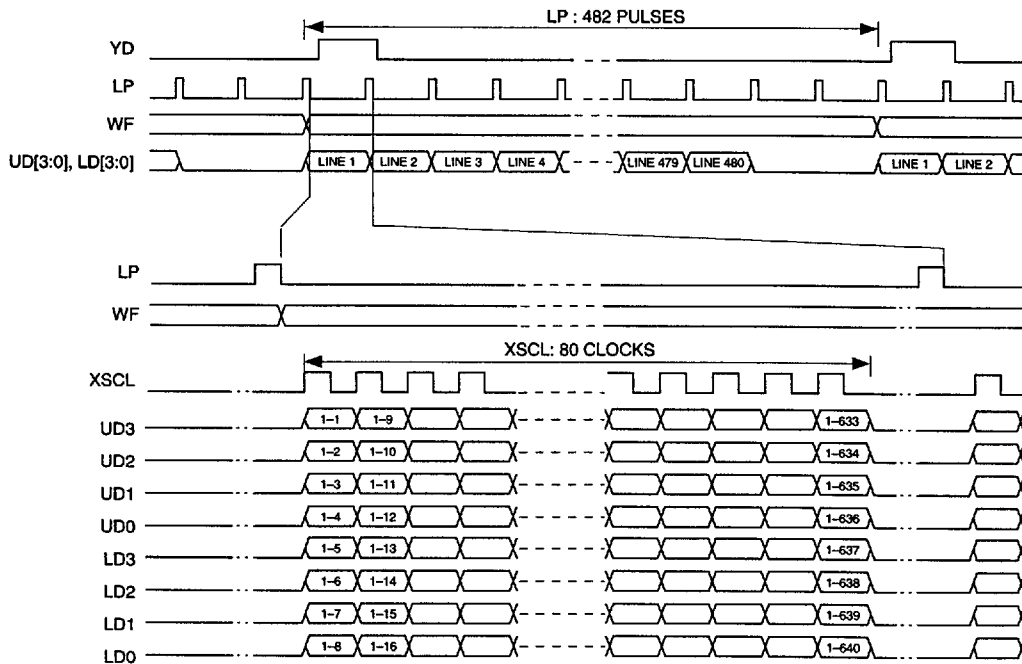


MONOCHROME LCD PANEL INTERFACE

4-Bit Single Monochrome Panel (i.e. 320 x 480)

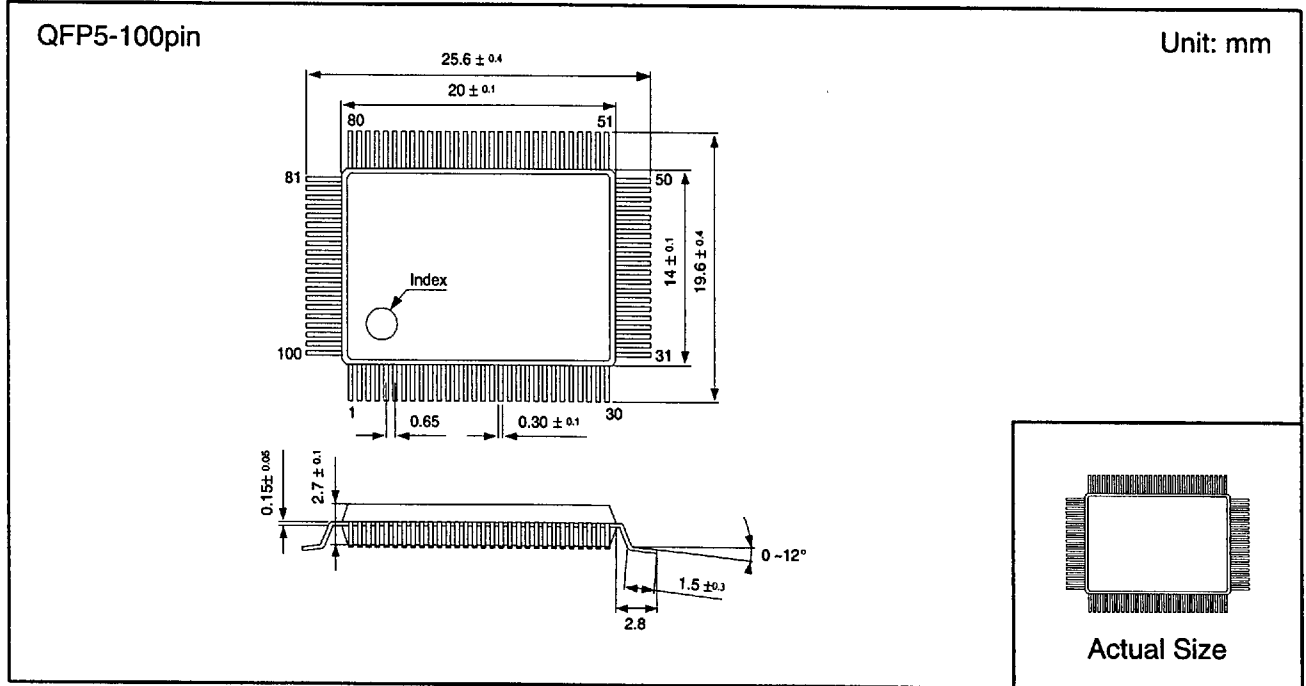


8-Bit Single Monochrome Panel (i.e. 640 x 480)

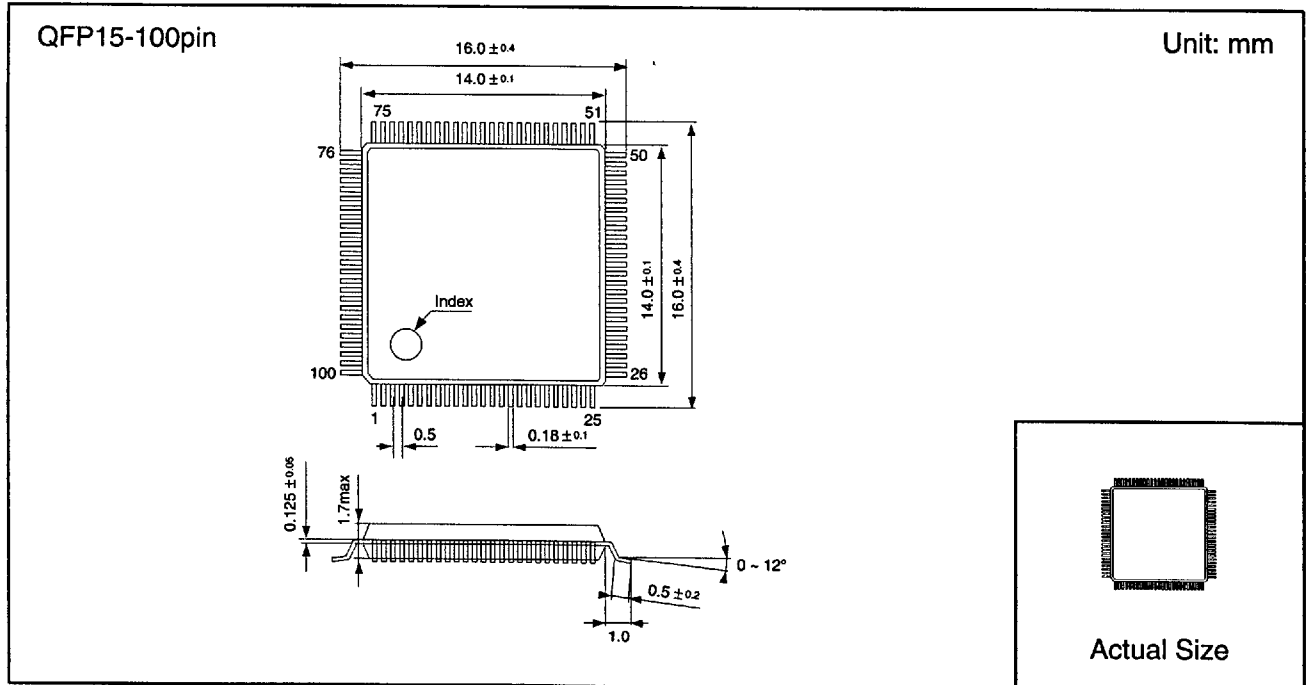


■ PACKAGE DIMENSIONS

● SED1351F0A



● SED1351FLB



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# 2.0

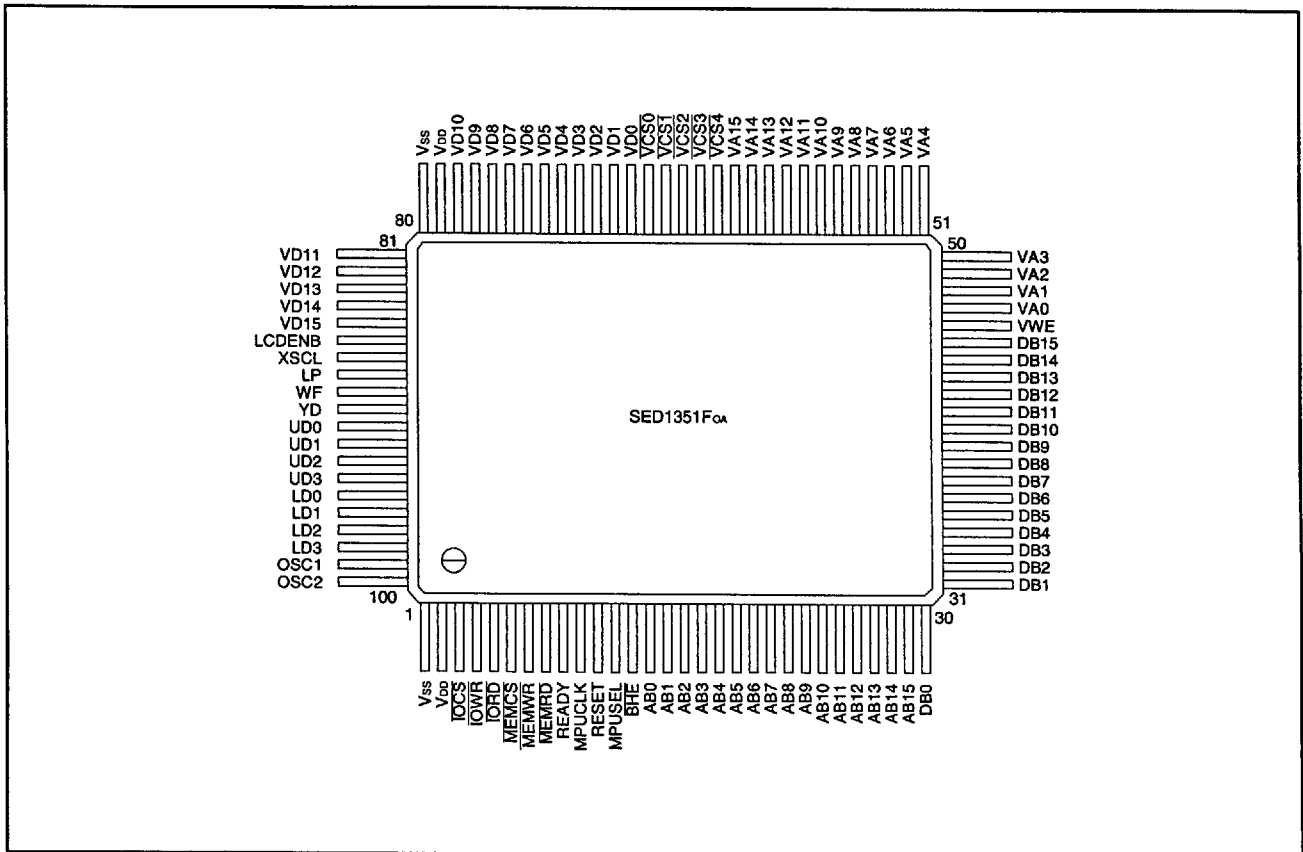
## *Pin Description*

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2.0 PIN DESCRIPTION

2.1 SED1351F<sub>0A</sub>

2.1.1 Pinout Diagram





## 2.1.2

## 2.0 Pin Description

### 2.1.2 SED1351F<sub>0A</sub> Pin Description Table

Pin	Pin Name	I/O
1	V <sub>SS</sub> (GND)	—
2	V <sub>DD</sub>	—
3	$\overline{\text{IOCS}}$	I
4	$\overline{\text{IOWR}}$	I
5	$\overline{\text{IORD}}$	I
6	$\overline{\text{MEMCS}}$	I
7	$\overline{\text{MEMWR}}$	I
8	$\overline{\text{MEMRD}}$	I
9	READY	O
10	MPUCLK	I
11	RESET	I
12	MPUSEL	I
13	$\overline{\text{BHE}}$	I
14	AB0	I
15	AB1	I
16	AB2	I
17	AB3	I
18	AB4	I
19	AB5	I
20	AB6	I
21	AB7	I
22	AB8	I
23	AB9	I
24	AB10	I
25	AB11	I
26	AB12	I
27	AB13	I
28	AB14	I
29	AB15	I
30	DB0	I/O
31	DB1	I/O
32	DB2	I/O
33	DB3	I/O
34	DB4	I/O

Pin	Pin Name	I/O
35	DB5	I/O
36	DB6	I/O
37	DB7	I/O
38	DB8	I/O
39	DB9	I/O
40	DB10	I/O
41	DB11	I/O
42	DB12	I/O
43	DB13	I/O
44	DB14	I/O
45	DB15	I/O
46	$\overline{\text{VWE}}$	O
47	VA0	O
48	VA1	O
49	VA2	O
50	VA3	O
51	VA4	O
52	VA5	O
53	VA6	O
54	VA7	O
55	VA8	O
56	VA9	O
57	VA10	O
58	VA11	O
59	VA12	O
60	VA13	O
61	VA14	O
62	VA15	O
63	$\overline{\text{VCS4}}$	O
64	$\overline{\text{VCS3}}$	O
65	$\overline{\text{VCS2}}$	O
66	$\overline{\text{VCS1}}$	O
67	$\overline{\text{VCS0}}$	O
68	VD0	I/O

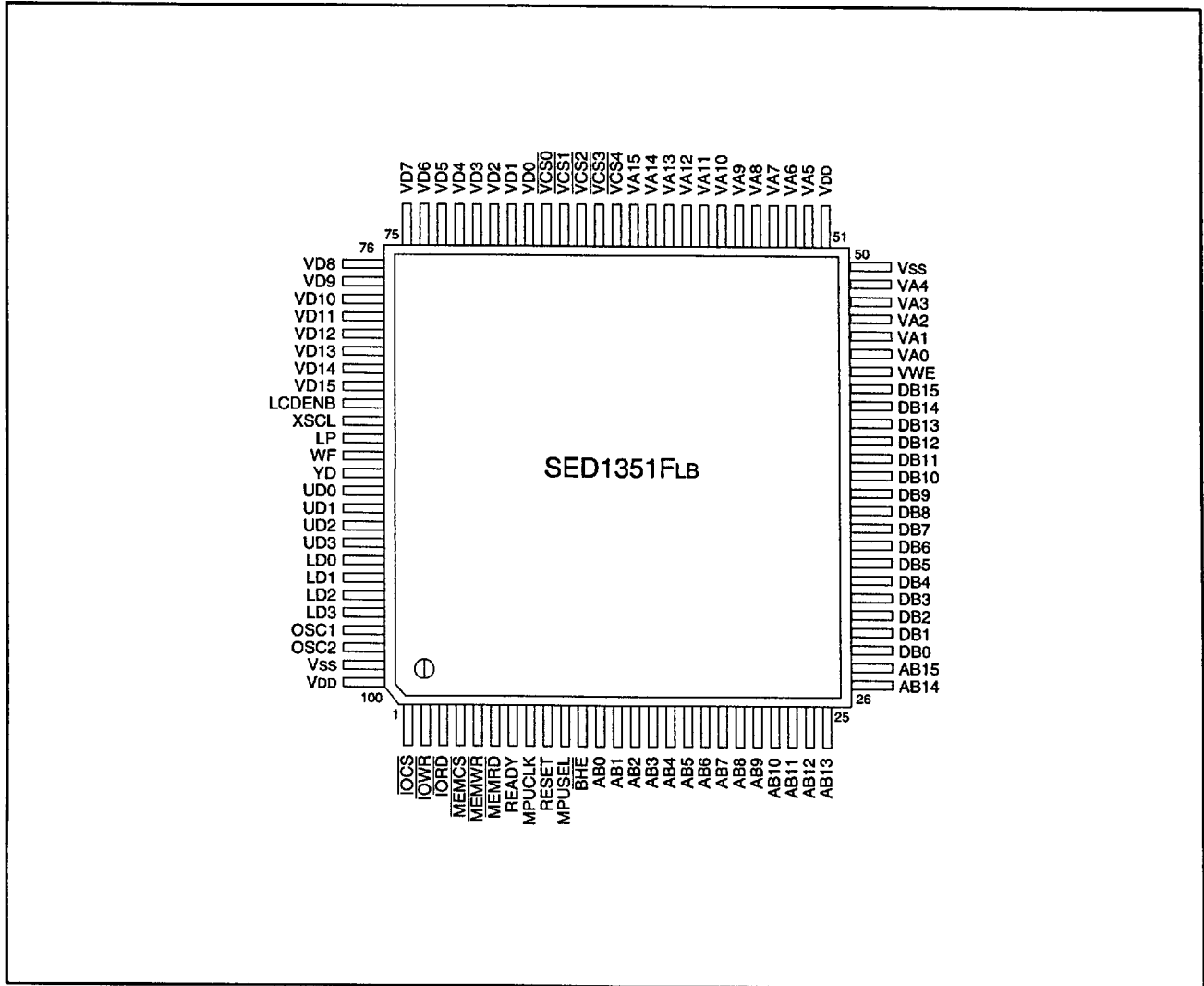
Pin	Pin Name	I/O
69	VD1	I/O
70	VD2	I/O
71	VD3	I/O
72	VD4	I/O
73	VD5	I/O
74	VD6	I/O
75	VD7	I/O
76	VD8	I/O
77	VD9	I/O
78	VD10	I/O
79	V <sub>DD</sub>	—
80	V <sub>SS</sub> (GND)	—
81	VD11	I/O
82	VD12	I/O
83	VD13	I/O
84	VD14	I/O
85	VD15	I/O
86	LCDENB	O
87	XSCL	O
88	LP	O
89	WF	O
90	YD	O
91	UD0	O
92	UD1	O
93	UD2	O
94	UD3	O
95	LD0	O
96	LD1	O
97	LD2	O
98	LD3	O
99	OSC1	I
100	OSC2	O

## 2.0 Pin Description

2.2 – 2.2.1

### 2.2 SED1351FLB

#### 2.2.1 Package Layout



2.2.2 SED1351F<sub>LB</sub> Pin Description Table

Pin	Pin Name	I/O
1	$\overline{\text{IOCS}}$	I
2	$\overline{\text{IOWR}}$	I
3	$\overline{\text{IORD}}$	I
4	$\overline{\text{MEMCS}}$	I
5	$\overline{\text{MEMWR}}$	I
6	$\overline{\text{MEMRD}}$	I
7	READY	O
8	MPUCLK	I
9	RESET	I
10	MPUSEL	I
11	$\overline{\text{BHE}}$	I
12	AB0	I
13	AB1	I
14	AB2	I
15	AB3	I
16	AB4	I
17	AB5	I
18	AB6	I
19	AB7	I
20	AB8	I
21	AB9	I
22	AB10	I
23	AB11	I
24	AB12	I
25	AB13	I
26	AB14	I
27	AB15	I
28	DB0	I/O
29	DB1	I/O
30	DB2	I/O
31	DB3	I/O
32	DB4	I/O
33	DB5	I/O
34	DB6	I/O

Pin	Pin Name	I/O
35	DB7	I/O
36	DB8	I/O
37	DB9	I/O
38	DB10	I/O
39	DB11	I/O
40	DB12	I/O
41	DB13	I/O
42	DB14	I/O
43	DB15	I/O
44	$\overline{\text{VWE}}$	O
45	VA0	O
46	VA1	O
47	VA2	O
48	VA3	O
49	VA4	O
50	V <sub>SS</sub> (GND)	—
51	V <sub>DD</sub>	—
52	VA5	O
53	VA6	O
54	VA7	O
55	VA8	O
56	VA9	O
57	VA10	O
58	VA11	O
59	VA12	O
60	VA13	O
61	VA14	O
62	VA15	O
63	$\overline{\text{VCS4}}$	O
64	$\overline{\text{VCS3}}$	O
65	$\overline{\text{VCS2}}$	O
66	$\overline{\text{VCS1}}$	O
67	$\overline{\text{VCS0}}$	O
68	VD0	I/O

Pin	Pin Name	I/O
69	VD1	I/O
70	VD2	I/O
71	VD3	I/O
72	VD4	I/O
73	VD5	I/O
74	VD6	I/O
75	VD7	I/O
76	VD8	I/O
77	VD9	I/O
78	VD10	I/O
79	VD11	I/O
80	VD12	I/O
81	VD13	I/O
82	VD14	I/O
83	VD15	I/O
84	LCDENB	O
85	XSCL	O
86	LP	O
87	WF	O
88	YD	O
89	UD0	O
90	UD1	O
91	UD2	O
92	UD3	O
93	LD0	O
94	LD1	O
95	LD2	O
96	LD3	O
97	OSC1	I
98	OSC2	O
99	V <sub>SS</sub> (GND)	—
100	V <sub>DD</sub>	—

## 2.3 SYSTEM INTERFACE

Table 1. MPU Interface Control Signal Functions

$\overline{\text{IOCS}}$	$\overline{\text{IOWR}}$	$\overline{\text{IORD}}$	$\overline{\text{MEMCS}}$	$\overline{\text{MEMWR}}$	$\overline{\text{MEMRD}}$	Operation
1	*	*	1	*	*	Invalid
0	0	1	1	1	1	Write to control register
0	1	0	1	1	1	Read from control register
1	1	1	0	0	1	Write to VRAM
1	1	1	0	1	0	Read from VRAM

- **READY**

MPU “wait” request output. It goes “L” on the falling edge of  $\overline{\text{IOCS}}$  or  $\overline{\text{MEMCS}}$ . It goes “H” the on the rising edge of the first MPUCLK after completion of SED1351F internal processing. READY is connected directly to the READY (or WAIT) terminal of the MPU.

- **MPUCLK**

MPU clock input

- **MPUSEL**

This input selects an 8- or 16-bit MPU interface.

- MPUSEL=0: 8-bit MPU interface (Z80, V20,i8088)
- MPUSEL=1: 16-bit MPU interface (V30,i8086)

- **RESET**

MPU reset input. This active high signal initializes R1, the system Mode Register.

## 2.4 VRAM INTERFACE

- **VD0-VD15**

These pins are connected to the VRAM data bus. For 16-bit MPUs VD0-VD7 are connected to the data bus of even byte addresses and VD8-VD15 to the data bus of odd byte addresses. For 8-bit MPUs, VD8-VD15 must be tied to VDD.

- **VA0-VA12,VA13/ $\overline{\text{VCS7}}$ -VA15/ $\overline{\text{VCS5}}$ , $\overline{\text{VCS0}}$ - $\overline{\text{VCS4}}$**

These pins are connected to the VRAM address bus and chip select lines.

The SED1351F provides select signals that can directly control eight 64 Kbit SRAMs (8 Kbytes each) or two 256 Kbit SRAMs (32 Kbytes) in the 64 Kbytes VRAM space.

- **$\overline{\text{VWE}}$**

This output is used for writing data to the VRAM. It is active low and is connected to the  $\overline{\text{WE}}$  input of the SRAMS.

## 2.5 LCD INTERFACE

- **UD0-UD3, LD0/UD4-LD3/UD7**

LCD display data output lines. UD0-UD3 provide the upper panel display data in single- or dual-panel LCD modes. LD0/UD4-LD3/UD7 provide the lower panel display data in dual-panel, dual-drive LCD mode. UD0-UD3, LD0/UD4-LD3/UD7 are used for 8-bit data transfer in single-panel, single-drive LCD mode.

- **XSCL**

Display data shift clock output. Data is shifted into the LCD X-drivers on the falling edge of this signal.

- **LP**

Display data latch clock output. One line of data is latched into the LCD X-drivers on the falling edge of this signal. LP can also be used to shift the Y-drive active line down by one.

- **WF**

LCD AC-drive signal output.

- **YD**

Active high start-of-frame pulse output. If this signal is shifted through the Y-drivers by LP, it provides the Y-drive active line signal.

- **LCDENB**

LCD enable signal output controlled by R1:D1.

## 2.6 OSCILLATOR

- **OSC1**

External clock input or internal oscillator external feed back resistor (Rf) connection.

- **OSC2**

If the internal oscillator is used, connect the external feed back resistor, Rf, to this pin. If an external clock is used, leave open.

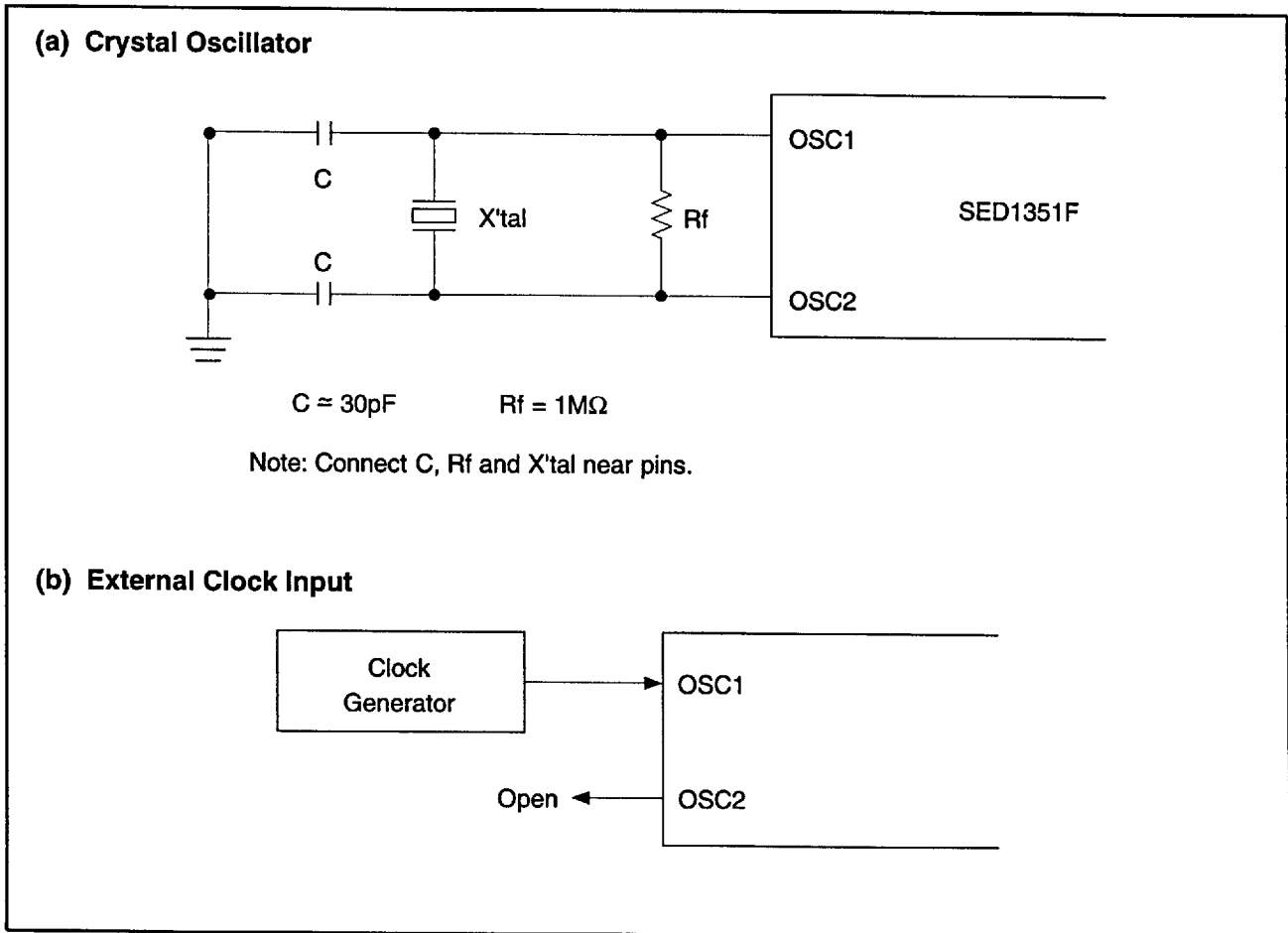


Figure 2. External and Internal Oscillators.

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# 3.0

## *Electrical Characteristics*



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## 3.0 ELECTRICAL CHARACTERISTICS

3.1 SED1351F<sub>0A</sub>3.1.1 SED1351F<sub>0A</sub> Absolute Maximum RatingsV<sub>SS</sub> = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V <sub>DD</sub>	V <sub>SS</sub> – 0.3 to 7.0	
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
Output current/pin	I <sub>OUT</sub>	±10	mA
Power dissipation	PD	200	mW
Supply current	I <sub>DD</sub> /I <sub>SS</sub>	±40	mA
Storage temperature	T <sub>stg</sub>	–65 to 150	°C

Note: Supply current is equivalent to maximum current into or out of a particular power pin.

## 3.1.2 Recommended Operating Conditions

V<sub>SS</sub> = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>	4.5	5.0	5.5	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub>	—	V <sub>DD</sub>	V
Operating temperature	T <sub>opr</sub>	–20	—	75	°C

### 3.1.3

## 3.0 Electrical Characteristics

### 3.1.3 SED1351F<sub>0A</sub> DC Characteristics

(Ta = -20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Pin
Static current	I <sub>DD5</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>SS</sub> V <sub>DD</sub> = MAX I <sub>OH</sub> = I <sub>OL</sub> = 0	—	—	100	μA	
Input leakage current	I <sub>L</sub>	V <sub>DD</sub> = MAX V <sub>IH</sub> = V <sub>DD</sub> V <sub>IL</sub> = V <sub>SS</sub>	-10	—	10	μA	Note 1
"H" level input voltage (1)	V <sub>IH1</sub>	V <sub>DD</sub> = MAX	3.5	—	—	V	OSC1
"L" level input voltage (1)	V <sub>IL1</sub>	V <sub>DD</sub> = MIN	—	—	1.0	V	
"H" level input voltage (2)	V <sub>IH2</sub>	V <sub>DD</sub> = MAX	2.0	—	—	V	
"L" level input voltage (2)	V <sub>IL2</sub>	V <sub>DD</sub> = MIN	—	—	0.8	V	Note 2
"H" level input voltage (3)	V <sub>T+</sub>	V <sub>DD</sub> = MAX	4.0	—	—	V	
"L" level input voltage (3)	V <sub>T-</sub>	V <sub>DD</sub> = MIN	—	—	0.8	V	Note 3
Hysteresis voltage	V <sub>H</sub>	V <sub>DD</sub> = TYP	0.3	—	—	V	
"H" level output voltage (1)	V <sub>OH1</sub>	V <sub>DD</sub> = MIN	V <sub>DD</sub> - 0.4	—	—	V	Note 4
"L" level output voltage (1)	V <sub>OL1</sub>	I <sub>OH</sub> = 1.5mA I <sub>OL</sub> = 3mA	—	—	V <sub>SS</sub> + 0.4	V	
"H" level output voltage (2)	V <sub>OH2</sub>	V <sub>DD</sub> = MIN	V <sub>DD</sub> - 0.4	—	—	V	OSC2
"L" level output voltage (2)	V <sub>OL2</sub>	I <sub>OH</sub> = -50μA I <sub>OL</sub> = 50μA	—	—	V <sub>SS</sub> + 0.4	V	

**Notes:**

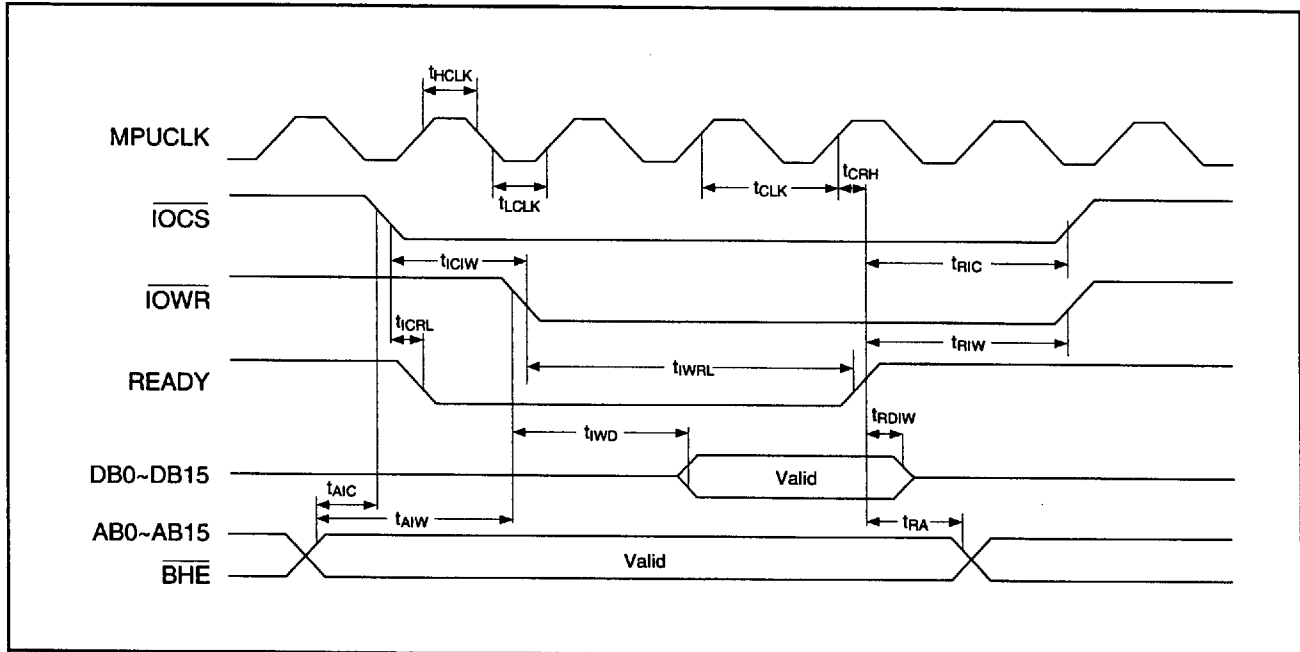
1.  $\overline{\text{MEMCS}}$ ,  $\overline{\text{MEMWR}}$ ,  $\overline{\text{MEMRD}}$ ,  $\overline{\text{IOCS}}$ ,  $\overline{\text{IOWR}}$ ,  $\overline{\text{IORD}}$ ,  $\overline{\text{MPUCLK}}$ , ABO-AB15,  $\overline{\text{BHE}}$ ,  $\overline{\text{MPUSEL}}$ ,  $\overline{\text{RESET}}$ , OSC1
2.  $\overline{\text{MEMCS}}$ ,  $\overline{\text{MEMWR}}$ ,  $\overline{\text{MEMRD}}$ ,  $\overline{\text{IOCS}}$ ,  $\overline{\text{IOWR}}$ ,  $\overline{\text{IORD}}$ ,  $\overline{\text{MPUCLK}}$ , ABO-AB15,  $\overline{\text{BHE}}$ , DBO-DB15, VD0-VD15
3.  $\overline{\text{MPUSEL}}$ ,  $\overline{\text{RESET}}$
4. DBO-DB15,  $\overline{\text{READY}}$ , VA0-VA15,  $\overline{\text{VCS0}}$ ,  $\overline{\text{VCS4}}$ , VD0-VD15,  $\overline{\text{VWE}}$ , XSCL, LP, WF, YD, UD0-UD3, LD0-LD3,  $\overline{\text{LCDENB}}$

## 3.0 Electrical Characteristics

### 3.1.4 – 3.1.4.1

#### 3.1.4 SED1351F<sub>0A</sub> AC Characteristics

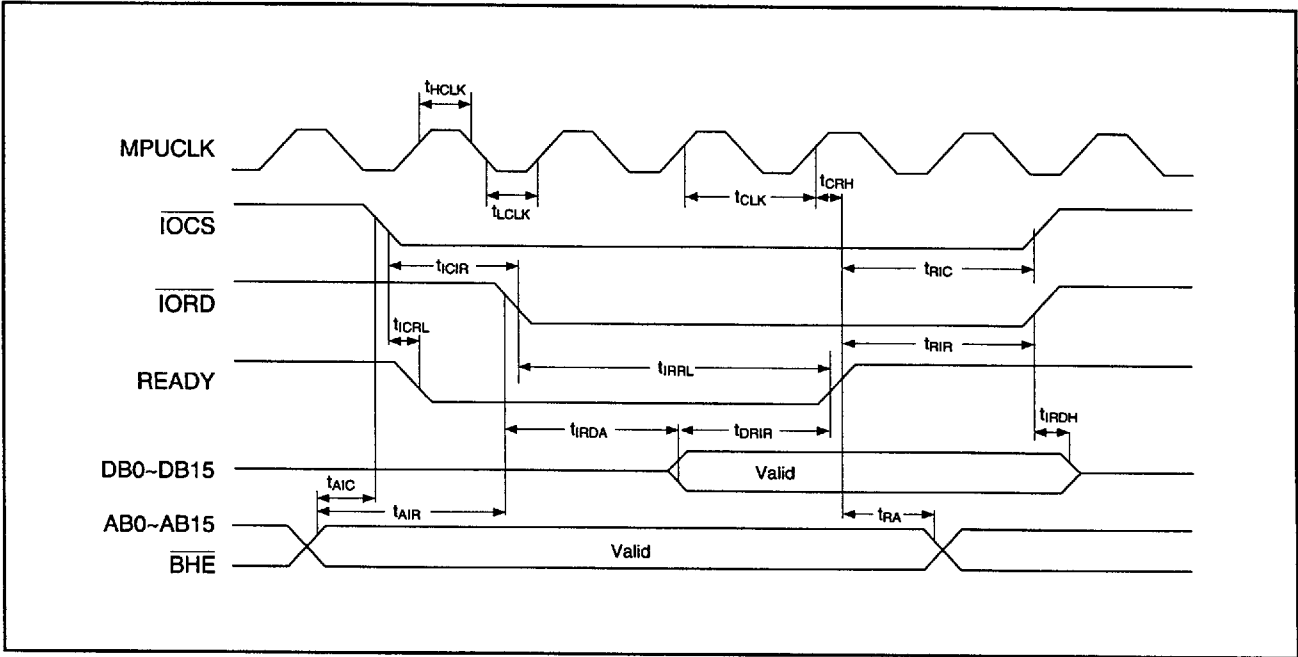
##### 3.1.4.1 IOWR Timing (MPU Write Data to Control Register)



(Ta = -20 to 75°C)

Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK	t <sub>CLK</sub>	80	—	1000	n
MPUCLK "H" pulse width	t <sub>HCLK</sub>	20	1/2 × t <sub>CLK</sub>	—	ns
MPUCLK "L" pulse width	t <sub>LCLK</sub>	20	1/2 × t <sub>CLK</sub>	—	ns
IOCS address setup time	t <sub>AIC</sub>	0	—	—	ns
IOWR address setup time	t <sub>AIW</sub>	0	—	—	ns
IOCS↓ → IOWR↓	t <sub>CIW</sub>	0	—	—	ns
IOWR↓ → data valid	t <sub>IWD</sub>	—	—	1.5 × t <sub>osc</sub>	ns
IOCS↓ → READY↓	t <sub>ICRL</sub>	—	—	30	ns
IOWR↓ → READY↑	t <sub>IWRL</sub>	2 × t <sub>osc</sub>	—	4 × t <sub>osc</sub> + t <sub>CLK</sub>	ns
MPUCLK↑ → READY↑	t <sub>CRH</sub>	—	—	20	ns
READY↑ → IOCS↑ hold time	t <sub>RIC</sub>	0	—	—	ns
READY↑ → IOWR↑ hold time	t <sub>RIW</sub>	0	—	—	ns
Write data hold time	t <sub>RDIW</sub>	0	—	—	ns
Address hold time	t <sub>RA</sub>	0	—	—	ns

3.1.4.2 IORD Timing (MPU Read Data from Control Register)



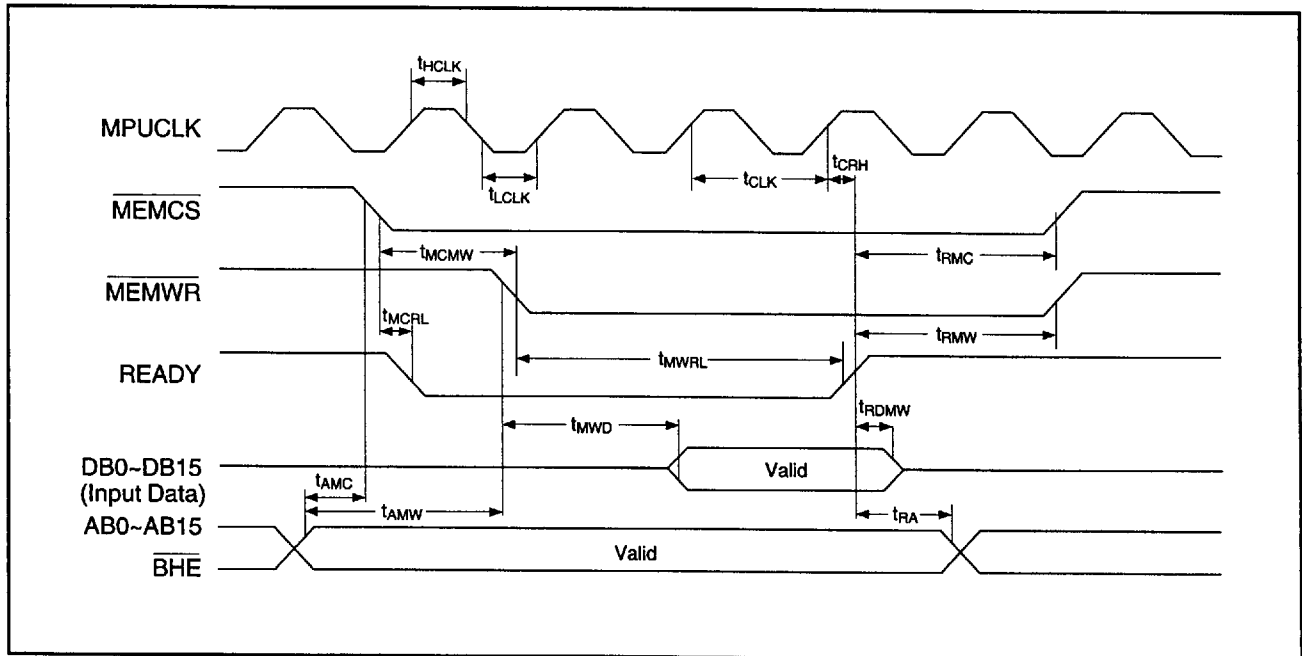
(Ta = -20 to 75°C)

Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK	t <sub>CLK</sub>	80	—	1000	ns
MPUCLK "H" pulse width	t <sub>HCLK</sub>	20	1/2 × t <sub>CLK</sub>	—	ns
MPUCLK "L" pulse width	t <sub>LCLK</sub>	20	1/2 × t <sub>CLK</sub>	—	ns
IOCS address setup time	t <sub>AIC</sub>	0	—	—	ns
IORD address setup time	t <sub>AIR</sub>	0	—	—	ns
IOCS↓ → IORD↓	t <sub>ICIR</sub>	0	—	—	ns
IOCS↓ → READY↓	t <sub>ICRL</sub>	—	—	30	ns
IORD↓ → READY↑	t <sub>IRRL</sub>	2 × t <sub>osc</sub>	—	4 × t <sub>osc</sub> + t <sub>CLK</sub>	ns
MPUCLK↓ → READY↑	t <sub>CRH</sub>	—	—	20	ns
IORD↓ → data valid	t <sub>IRDA</sub>	2 × t <sub>osc</sub>	—	4 × t <sub>osc</sub>	ns
data valid → READY↑	t <sub>DRIR</sub>	0	—	—	ns
Read data hold time	t <sub>IRDH</sub>	0	—	—	ns
READY↑ → IOCS↑ hold time	t <sub>RIC</sub>	0	—	—	ns
READY↑ → IORD↑ hold time	t <sub>RIR</sub>	0	—	—	ns
Address hold time	t <sub>RA</sub>	0	—	—	ns

## 3.0 Electrical Characteristics

### 3.1.4.3

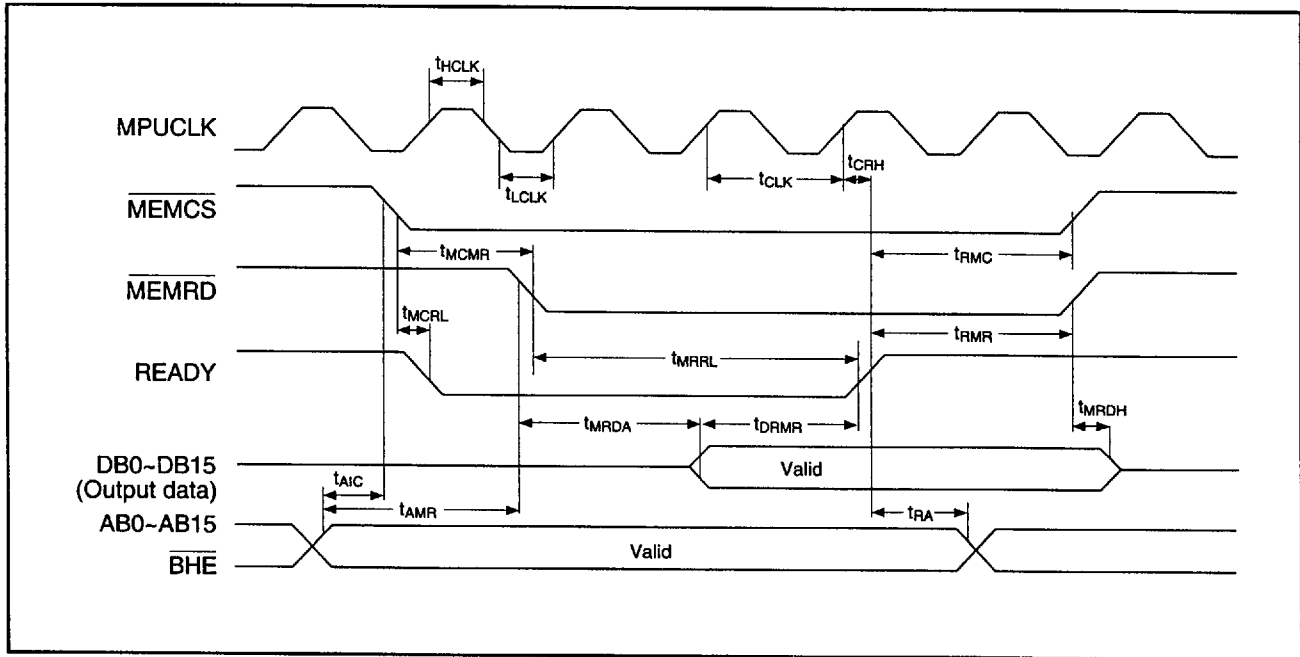
#### 3.1.4.3 MEMWR Timing (MPU Write Data to Video Memory)



( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK	$t_{CLK}$	80	—	1000	n
MPUCLK "H" pulse width	$t_{HCLK}$	20	$1/2 \times t_{CLK}$	—	ns
MPUCLK "L" pulse width	$t_{LCLK}$	20	$1/2 \times t_{CLK}$	—	ns
MEMCS address setup time	$t_{AMC}$	0	—	—	ns
MEMWR address setup time	$t_{AMW}$	0	—	—	ns
MEMCS $\downarrow$ $\rightarrow$ MEMWR $\downarrow$	$t_{MCMW}$	0	—	—	ns
MEMWR $\downarrow$ $\rightarrow$ data valid	$t_{MWD}$	—	—	$1.5 \times t_{osc}$	ns
IOCS $\downarrow$ $\rightarrow$ READY $\downarrow$	$t_{MCRl}$	—	—	30	ns
MEMWR $\uparrow$ $\rightarrow$ READY $\uparrow$	$t_{MWRL}$	$2 \times t_{osc}$	—	$4 \times t_{osc} + t_{CLK}$	ns
MPUCLK $\uparrow$ $\rightarrow$ READY $\uparrow$	$t_{CRH}$	—	—	20	ns
READY $\uparrow$ $\rightarrow$ MEMCS $\uparrow$ hold time	$t_{RMC}$	0	—	—	ns
READY $\uparrow$ $\rightarrow$ MEMWR $\uparrow$ hold time	$t_{RMW}$	0	—	—	ns
Write data hold time	$t_{RDMW}$	0	—	—	ns
Address hold time	$t_{RA}$	0	—	—	ns

3.1.4.4 MEMRD Timing (MPU Read Data from Video Memory)

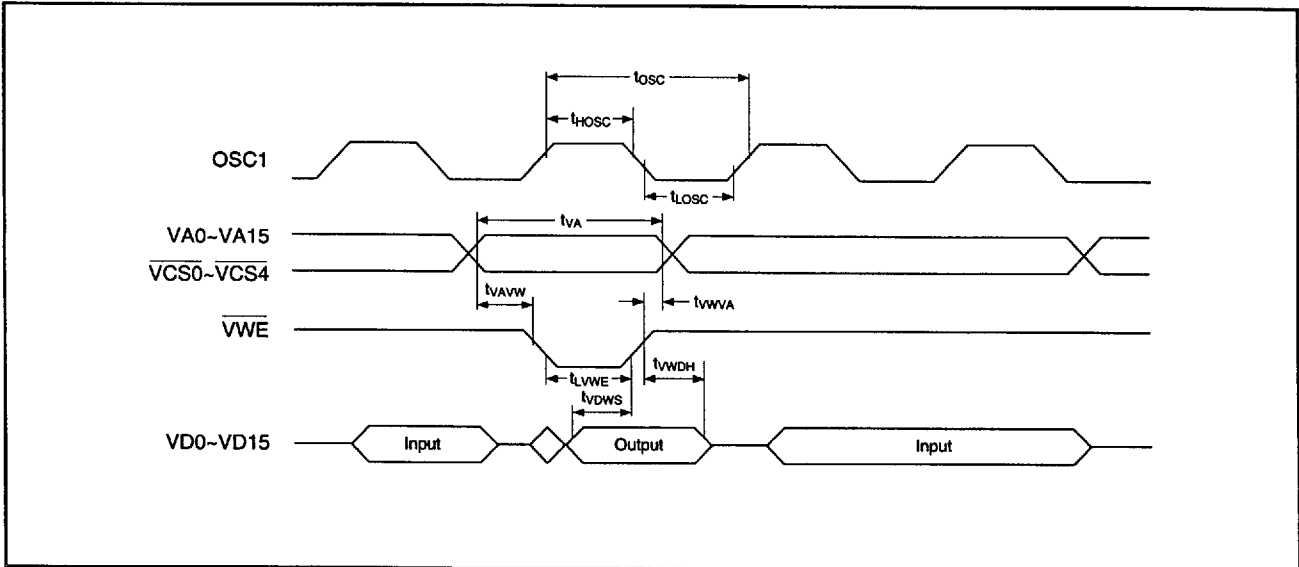


( $T_a = -20$  to  $75^\circ\text{C}$ )

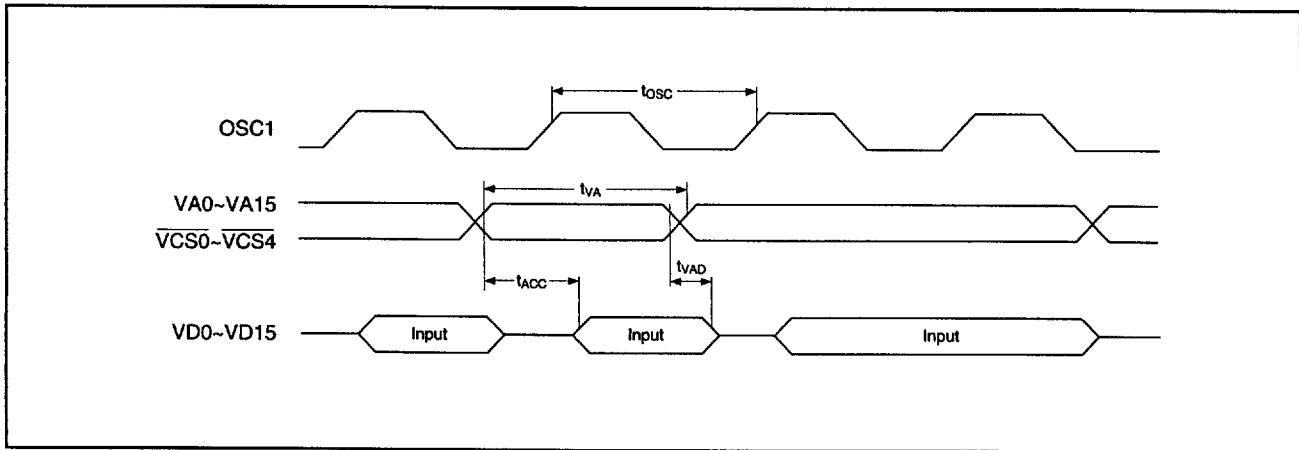
Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK	$t_{CLK}$	80	—	1000	ns
MPUCLK "H" pulse width	$t_{HCLK}$	20	$1/2 \times t_{CLK}$	—	ns
MPUCLK "L" pulse width	$t_{LCLK}$	20	$1/2 \times t_{CLK}$	—	ns
$\overline{MEMCS}$ address setup time	$t_{MCMR}$	0	—	—	ns
$\overline{MEMRD}$ address setup time	$t_{AMR}$	0	—	—	ns
$\overline{MEMCS}\downarrow \rightarrow \overline{MEMRD}\downarrow$	$t_{MCMR}$	0	—	—	ns
$\overline{MEMCS}\downarrow \rightarrow \text{READY}\downarrow$	$t_{MCRL}$	—	—	30	ns
$\overline{MEMRD}\downarrow \rightarrow \text{READY}\uparrow$	$t_{MRRL}$	$2 \times t_{osc}$	—	$4 \times t_{osc} + t_{CLK}$	ns
$\text{MPUCLK}\uparrow \rightarrow \text{READY}\uparrow$	$t_{CRH}$	—	—	20	ns
$\overline{MEMCS}\downarrow \rightarrow$ data valid	$t_{MRDA}$	$2 \times t_{osc}$	—	$4 \times t_{osc}$	ns
Data valid $\rightarrow \text{READY}\uparrow$	$t_{DRMR}$	0	—	—	ns
Read data hold time	$t_{MRDH}$	0	—	—	ns
$\text{READY}\uparrow \rightarrow \overline{MEMCS}\uparrow$ hold time	$t_{RMC}$	0	—	—	ns
$\text{READY}\uparrow \rightarrow \overline{MEMRD}\uparrow$ hold time	$t_{RMR}$	0	—	—	ns
Address hold time	$t_{RA}$	0	—	—	ns

3.1.4.5 VRAM Interface Timing

3.1.4.5.1 Write Data to VRAM



3.1.4.5.2 Read Data From VRAM





### 3.1.4.5.3

## 3.0 Electrical Characteristics

### 3.1.4.5.3 Timing

(Ta = -20 to 75°C)

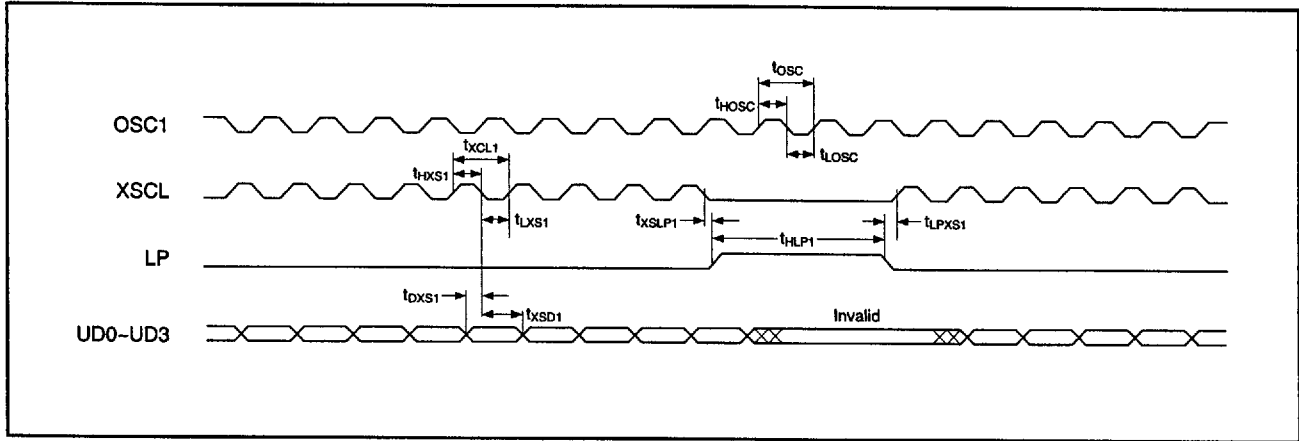
Parameter	Symbol	Min	Typ	Max	Unit
OSC1	t <sub>osc</sub>	80	—	500	ns
OSC1 "H" pulse width	t <sub>HOSC</sub>	—	1/2 × t <sub>osc</sub>	—	ns
OSC1 "L" pulse width	t <sub>LOSC</sub>	—	1/2 × t <sub>osc</sub>	—	ns
VWE address setup time	t <sub>VAVW</sub>	1/2 × t <sub>osc</sub> - 20	1/2 × t <sub>osc</sub>	—	ns
VWE address setup time	t <sub>VWVA</sub>	0	—	—	ns
VWE "L" pulse width	t <sub>LVWE</sub>	1/2 × t <sub>osc</sub> - 10	1/2 × t <sub>osc</sub>	—	ns
VWE data setup time	t <sub>VDWS</sub>	1/2 × t <sub>osc</sub> - 25	1/2 × t <sub>osc</sub>	—	ns
VWE data hold time	t <sub>VWDH</sub>	0	—	20	ns
VRAM address cycle time	t <sub>VA</sub>	t <sub>osc</sub>	—	—	ns
VRAM address access time	t <sub>ACC</sub>	—	—	t <sub>osc</sub> - 20	ns
VRAM read data hold time	t <sub>VAD</sub>	0	—	—	ns

## 3.0 Electrical Characteristics

### 3.1.4.6 – 3.1.4.6.1

#### 3.1.4.6 LCD Interface Timing

##### 3.1.4.6.1 Mode 1 (4-Bit transfer)



( $T_a = -20$  to  $75^\circ\text{C}$ )

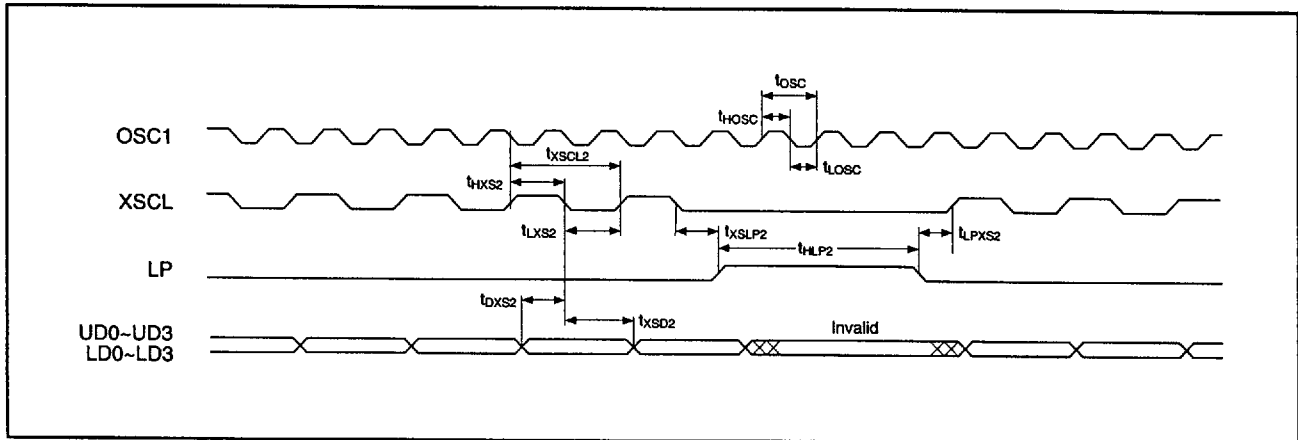
Parameter	Symbol	Min	Typ	Max	Unit
OSC1	$t_{osc}$	80	—	500	ns
OSC1 "H" pulse width	$t_{HOSC}$	$1/2 \times t_{osc} - 10$	—	—	ns
OSC1 "L" pulse width	$t_{LOSC}$	$1/2 \times t_{osc} - 10$	—	—	ns
XSCL	$t_{XSCL1}$	—	—	—	ns
XSCL "H" pulse width	$t_{HXS1}$	$1/2 \times t_{osc} - 10$	—	—	ns
XSCL "L" pulse width	$t_{LXS1}$	$1/2 \times t_{osc} - 10$	—	—	ns
XSCL $\downarrow$ $\rightarrow$ LP $\uparrow$	$t_{XSLP1}$	-10			
LP $\downarrow$ $\rightarrow$ XSCL $\uparrow$	$t_{LPXS1}$	$t_{osc} - 10$			
Data setup time	$t_{DXS1}$	$1/2 \times t_{osc} - 10$	—	—	ns
Data hold time	$t_{XSD1}$	$1/2 \times t_{osc} - 20$	—	—	ns
LP "H" pulse width (Note 1)	$t_{HLP1}$	$(2n - 1/2) \times t_{osc} - 20$	—	—	ns

**Note 1:** "n" is the value of LWP

### 3.1.4.6.2

## 3.0 Electrical Characteristics

### 3.1.4.6.2 Mode 1 (8-bit transfer), Mode 2, Mode 3 (4-bit transfer), Mode 5



( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
OSC1	$t_{osc}$	80	—	500	ns
OSC1 "H" pulse width	$t_{hosc}$	$1/2 \times t_{osc} - 10$	—	—	ns
OSC1 "L" pulse width	$t_{losc}$	$1/2 \times t_{osc} - 10$	—	—	ns
XSCL	$t_{xscl1}$	$2 \times t_{osc} - 20$	—	—	ns
XSCL "H" pulse width	$t_{hxs2}$	$t_{osc} - 10$	—	—	ns
XSCL "L" pulse width	$t_{lxs2}$	$t_{osc} - 10$	—	—	ns
XSCL $\downarrow$ $\rightarrow$ LP $\uparrow$	$t_{xslp2}$	$1/2 \times t_{osc} - 10$	—	—	ns
LP $\downarrow$ $\rightarrow$ XSCL $\uparrow$	$t_{lpxs2}$	$t_{osc} - 10$	—	—	ns
Data setup time	$t_{dxs2}$	$t_{osc} - 10$	—	—	ns
Data hold time	$t_{xsd2}$	$t_{osc} - 20$	—	—	ns
LP "H" pulse width (Note 1)	$t_{hlp2}$	$(2n - 1/2 \times t_{osc} - 20)$	—	—	ns
LP "H" pulse width (Note 2)		$(4n - 1/2) \times t_{osc} - 20$	—	—	ns

- "n" is the value of LWP

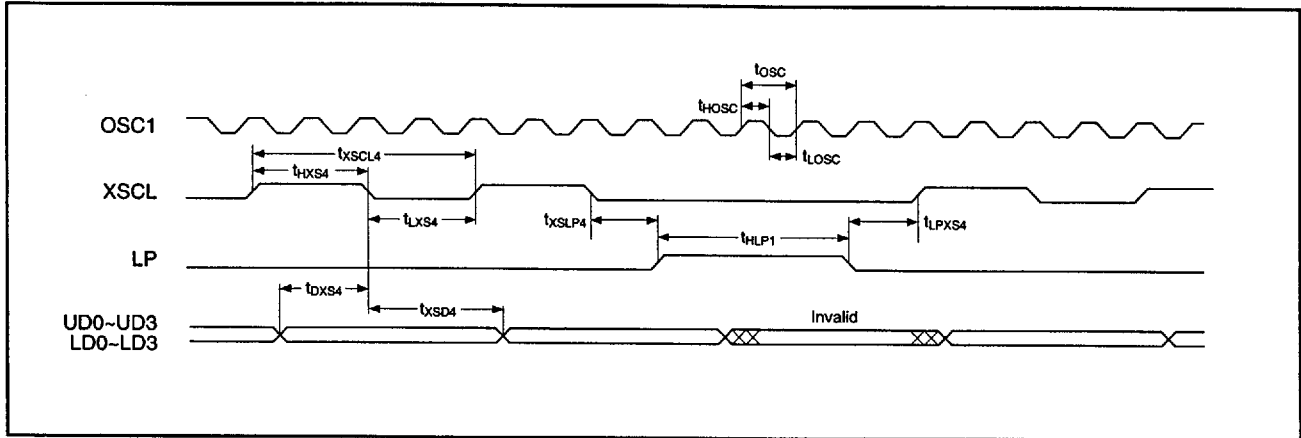
**Note 1.** Mode 1 (8-bit transfer) and Mode 2

**Note 2.** Mode 3 (4-bit transfer) and Mode 5

### 3.0 Electrical Characteristics

### 3.1.4.6.3

#### 3.1.4.6.3 Mode 3 (8-bit transfer, Mode 4, Mode 6

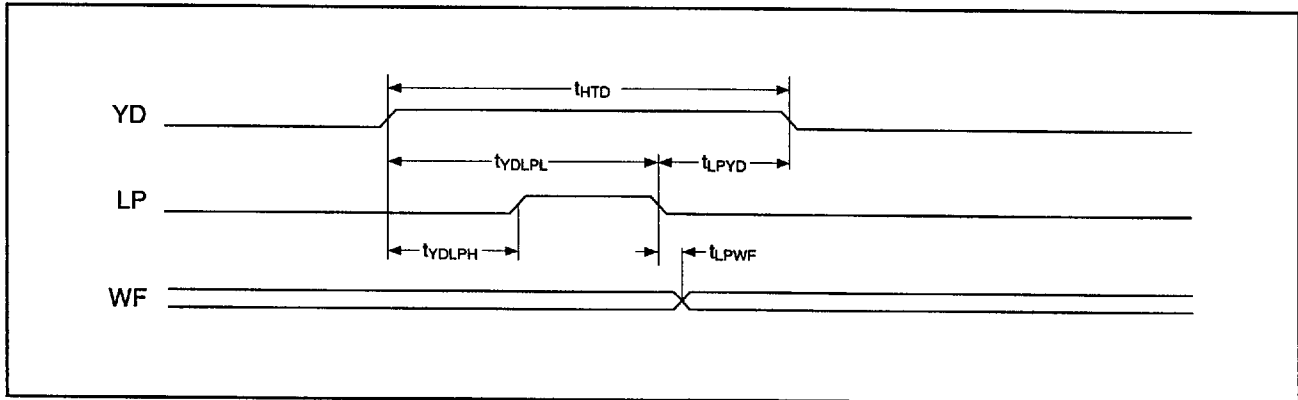


(Ta = -20 to 75°C)

Parameter	Symbol	Min	Typ	Max	Unit
OSC1	t <sub>osc</sub>	80	—	500	ns
OSC1 "H" pulse width	t <sub>hosc</sub>	1/2 × t <sub>osc</sub> - 10	—	—	ns
OSC1 "L" pulse width	t <sub>losc</sub>	1/2 × t <sub>osc</sub> - 10	—	—	ns
XSCL	t <sub>xscl4</sub>	4 × t <sub>osc</sub> - 20	—	—	ns
XSCL "H" pulse width	t <sub>hxs4</sub>	2 × t <sub>osc</sub> - 20	—	—	ns
XSCL "L" pulse width	t <sub>lxs4</sub>	2 × t <sub>osc</sub> - 20	—	—	ns
XSCL↓ → LP↑	t <sub>xslp4</sub>	1.5 × t <sub>osc</sub> - 10	—	—	ns
LP↓ → XSCL↑	t <sub>lpxs4</sub>	t <sub>osc</sub> - 10	—	—	ns
Data setup time	t <sub>dxs4</sub>	2 × t <sub>osc</sub> - 20	—	—	ns
Data hold time	t <sub>xsd4</sub>	2 × t <sub>osc</sub> - 20	—	—	ns
LP "H" pulse width (Note 1)	t <sub>hlp4</sub>	(4n - 1/2) × t <sub>osc</sub> - 20	—	—	ns

Note 1. "n" is the value of LWP.

3.1.4.6.4 Sync Timing



(Ta = -20 to 75°C)

Parameter	Symbol	Min	Typ	Max	Unit
YD "H" pulse width	(Note 1)	$(m + n) 2 \times t_{osc} - 20$	—	—	ms
	(Note 2)	$(m + n) 4 \times t_{osc} - 20$	—	—	ms
YD↑ → LP↑	(Note 1)	$4.5 \times t_{osc} - 20$	—	—	ms
	(Note 2)	$5.5 \times t_{osc} - 20$	—	—	ms
YD↑ → LP↓	(Note 1)	$(n + 2) 2 \times t_{osc} - 20$	—	—	ms
	(Note 2)	$(n + 5/4) 4 \times t_{osc} - 20$	—	—	ms
LP↓ → YD↓	(Note 1)	$(m - 2) 2 \times t_{osc} - 20$	—	—	ms
	(Note 2)	$(m - 5/4) 4 t_{osc} - 20$	—	—	ms
LP↓ WF↑↓	tLPWRF	-100	—	—	ms

- "m" is the value of C/R
- "n" is the value of LPW
  1. Mode 1, Mode 2
  2. Mode 3, Mode 4, Mode 5, Mode 6.

## 3.0 Electrical Characteristics

3.2 – 3.2.2

### 3.2 SED1351F<sub>LB</sub>

#### 3.2.1 SED1351F<sub>LB</sub> Absolute Maximum Ratings

V<sub>SS</sub> = 0V

Parameter	Symbol	Rating	Unit
Power voltage	V <sub>DD</sub>	V <sub>SS</sub> – 0.3 to 7.0	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.5	V
Output voltage	V <sub>OUT</sub>	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.5	V
Output current/pin	I <sub>OUT</sub>	±24	mA
Allowable loss	P <sub>D</sub>	200	mW
Power current	I <sub>DD</sub> /I <sub>SS</sub>	±40	mA
Storage temperature	T <sub>STG</sub>	–65 to 150	°C

Note: Power current: Allowable current input to or output from power terminal V<sub>DD</sub> or V<sub>SS</sub>.

#### 3.2.2 Recommended Operating Conditions

V<sub>SS</sub> = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Power voltage	V <sub>DD</sub>	2.7	—	3.6	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub>	—	V <sub>DD</sub>	V
Operating temperature	T <sub>OPR</sub>	–20	—	75	°C

### 3.2.3

## 3.0 Electrical Characteristics

### 3.2.3 SED1351F<sub>LB</sub> DC Characteristics

(T<sub>a</sub> = -20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Pin
Static current	I <sub>DD5</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>SS</sub> V <sub>DD</sub> = MAX I <sub>OH</sub> = I <sub>OL</sub> = 0	—	—	30	μA	
Input leakage current	I <sub>L</sub>	V <sub>DD</sub> = MAX V <sub>IH</sub> = V <sub>DD</sub> V <sub>IL</sub> = V <sub>SS</sub>	-1	—	1	μA	Note 1
"H" level input voltage (1)	V <sub>IH1</sub>	V <sub>DD</sub> = MAX	0.7 V <sub>DD</sub>	—	—	V	OSC1
"L" level input voltage (1)	V <sub>IL1</sub>	V <sub>DD</sub> = MIN	—	—	0.2 V <sub>DD</sub>	V	
"H" level input voltage (2)	V <sub>IH2</sub>	V <sub>DD</sub> = MAX	0.7 V <sub>DD</sub>	—	—	V	Note 2
"L" level input voltage (2)	V <sub>IL2</sub>	V <sub>DD</sub> = MIN	—	—	0.2 V <sub>DD</sub>	V	
"H" level input voltage (3)	V <sub>T+</sub>	V <sub>DD</sub> = MAX	0.8 V <sub>DD</sub>	—	—	V	Note 3
"L" level input voltage (3)	V <sub>T-</sub>	V <sub>DD</sub> = MIN	—	—	0.2 V <sub>DD</sub>	V	
Hysteresis voltage	V <sub>H</sub>	V <sub>DD</sub> = TYP	0.3	—	—	V	
"H" level output voltage (1)	V <sub>OH1</sub>	V <sub>DD</sub> = MIN	V <sub>DD</sub> - 0.3	—	—	V	Note 4
"L" level output voltage (1)	V <sub>OL1</sub>	I <sub>OH</sub> = -1.5mA I <sub>OL</sub> = 3mA	—	—	V <sub>SS</sub> + 0.3	V	
"H" level output voltage (2)	V <sub>OH2</sub>	V <sub>DD</sub> = MIN	V <sub>DD</sub> - 0.4	—	—	V	OSC2
"L" level output voltage (2)	V <sub>OL2</sub>	I <sub>OH</sub> = -50μA I <sub>OL</sub> = 50μA	—	—	V <sub>SS</sub> + 0.4	V	

**Notes:**

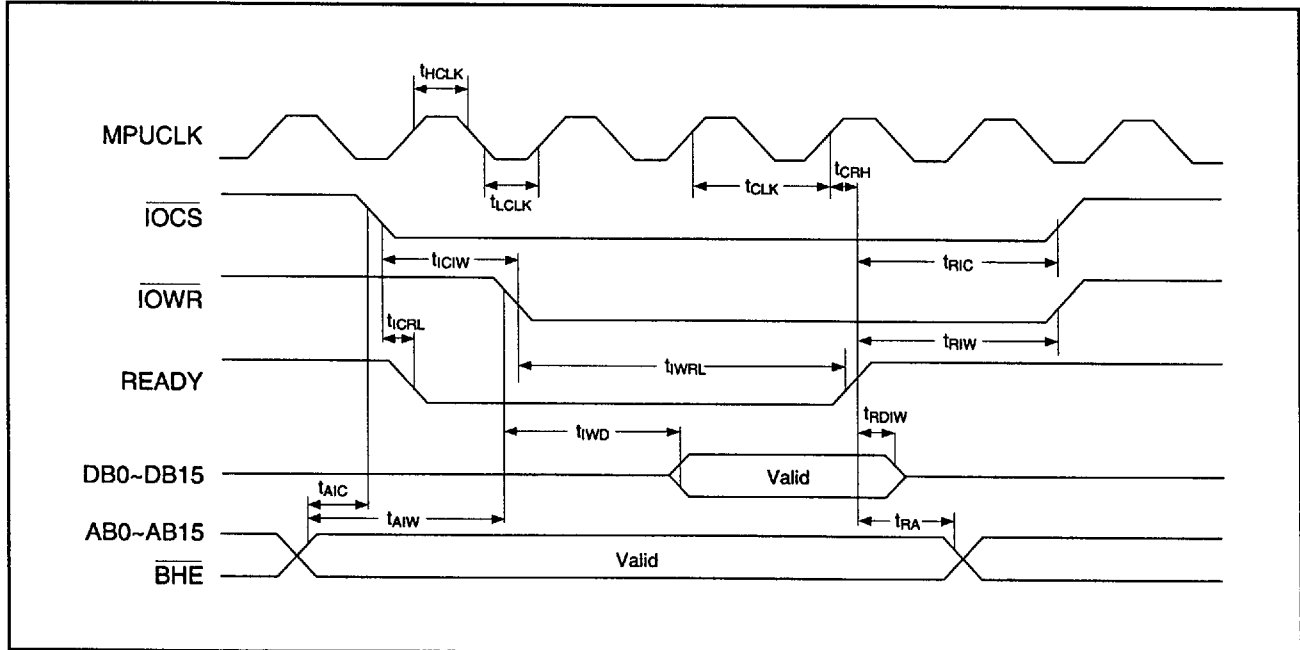
- MEMCS, MEMWR, MEMRD, IOCS, IOWR, IORD, MPUCLK, ABO-AB15, BHE, MPUSEL, RESET, OSC1
- MEMCS, MEMWR, MEMRD, IOCS, IOWR, IORD, MPUCLK, ABO-AB15, BHE, DBO-DB15, VD0-VD15
- MPUSEL, RESET
- DB0-DB15, READY, VA0-VA15, VCS0-VCS4, VD0-VD15, VWE, XSCL, LP, WF, YD, UD0-UD3, LD0-LD3, LCDENB

## 3.0 Electrical Characteristics

### 3.2.4 – 3.2.4.1

#### 3.2.4 SED1351F<sub>LB</sub> AC Characteristics

##### 3.2.4.1 IOWR Timing (Write to the Control Register)

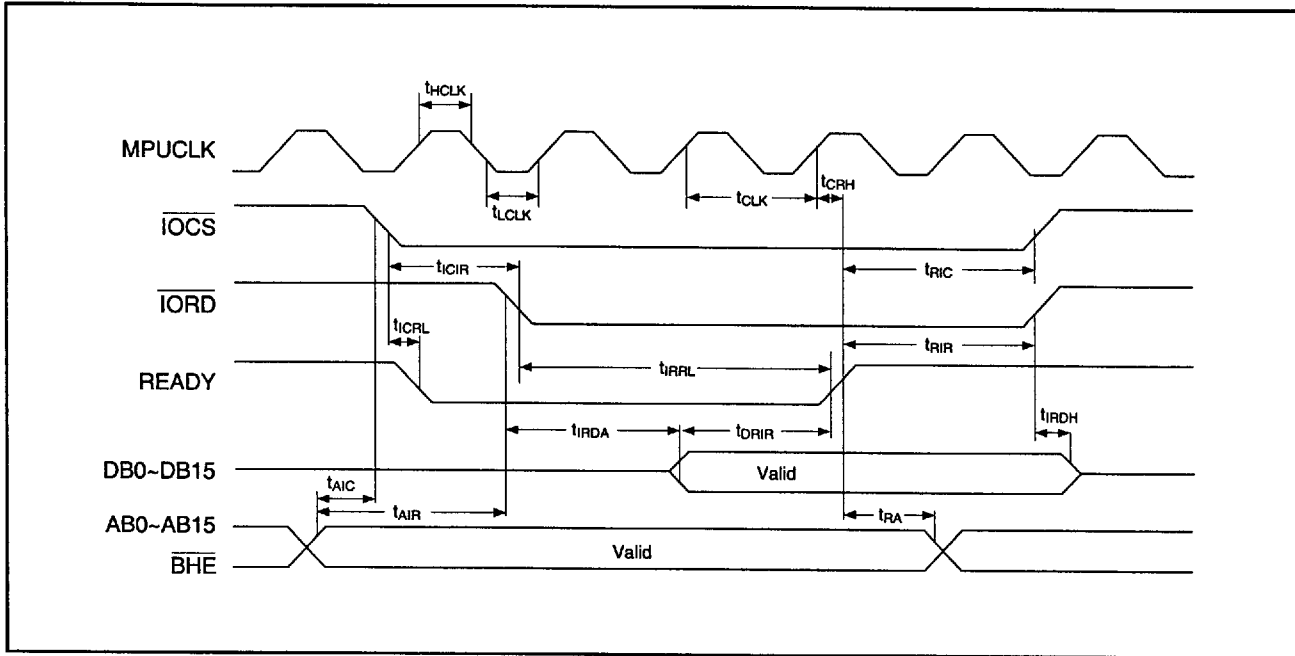


( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK cycle	$t_{CLK}$	100	—	1000	ns
MPUCLK "H" pulse width	$t_{HCLK}$	20	$1/2 \times t_{CLK}$	—	ns
MPUCLK "L" pulse width	$t_{LCLK}$	20	$1/2 \times t_{CLK}$	—	ns
$\overline{IOCS}$ address setup time	$t_{AIC}$	0	—	—	ns
$\overline{IOWR}$ address setup time	$t_{AIW}$	0	—	—	ns
$\overline{IOCS}\downarrow \rightarrow \overline{IOWR}\downarrow$	$t_{ICRW}$	0	—	—	ns
$\overline{IOWR}\downarrow \rightarrow$ written data determination	$t_{IWD}$	—	—	$1.5 \times t_{osc}$	ns
$\overline{IOCS}\downarrow \rightarrow$ Not Ready	$t_{ICRL}$	8	—	39	ns
$\overline{IORD}\downarrow \rightarrow$ Not Ready period	$t_{IWRL}$	$2 \times t_{osc}$ $+ 17$	—	$4 \times t_{osc}$ $+ 85 + t_{CLK}$	ns
MPUCLK $\uparrow \rightarrow$ READY	$t_{CRH}$	7	—	20	n
READY $\uparrow \rightarrow \overline{IOCS}$ hold time	$t_{RIC}$	0	—	—	ns
READY $\uparrow \rightarrow \overline{IOWR}$ hold time	$t_{RIW}$	0	—	—	ns
READY $\uparrow \rightarrow$ Written data hold time	$t_{RDIW}$	0	—	—	ns
READY $\uparrow \rightarrow$ Address hold time	$t_{RA}$	0	—	—	ns



3.2.4.2 IORD Timing (Read from Control Register)



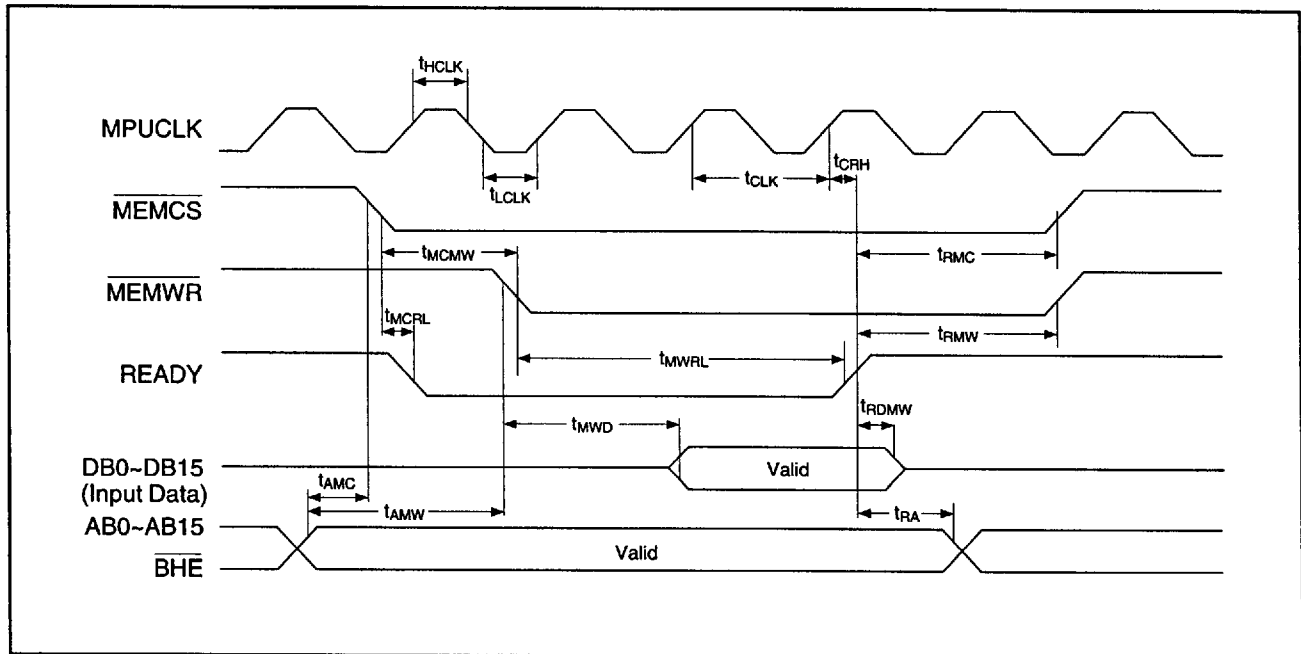
(Ta = -20 to 75°C)

Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK cycle	$t_{CLK}$	100	—	1000	ns
MPUCLK "H" pulse width	$t_{HCLK}$	20	$1/2 \times t_{CLK}$	—	ns
MPUCLK "L" pulse width	$t_{LCLK}$	20	$1/2 \times t_{CLK}$	—	ns
IOCS address setup time	$t_{AIC}$	0	—	—	ns
IORD address setup time	$t_{AIR}$	0	—	—	ns
IOCS↓ → IORD↓	$t_{ICIR}$	0	—	—	ns
IOCS↓ → Not Ready	$t_{ICRL}$	8	—	39	ns
IORD↓ → Not Ready period	$t_{IRRL}$	$2 \times t_{osc} + 17$	—	$4 \times t_{osc} + 85 + t_{CLK}$	ns
MPUCLK↑ → Ready	$t_{CRH}$	7	—	36	ns
IORD↓ → Read data determination	$t_{IRDA}$	$2 \times t_{osc}$	—	$4 \times t_{osc} + 50$	ns
Read data determination → READY↑	$t_{DRIR}$	0	—	—	ns
IORD↓ → Read data hold time	$t_{IRDH}$	0	—	—	ns
READY↑ → IOCS hold time	$t_{RIC}$	0	—	—	ns
READY↑ → IORD hold time	$t_{RIR}$	0	—	—	ns
READY↑ → Address hold time	$t_{RA}$	0	—	—	ns

## 3.0 Electrical Characteristics

### 3.2.4.3

#### 3.2.4.3 MEMWR Timing (Write to the VRAM)



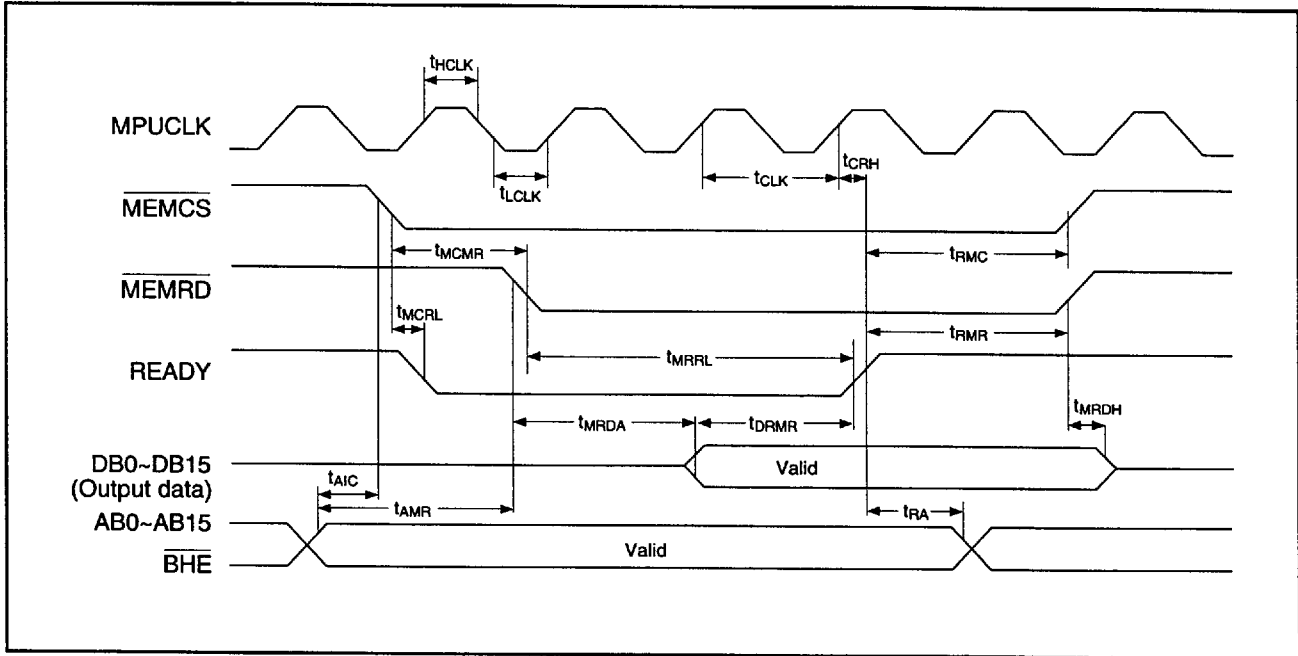
( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK cycle	$t_{CLK}$	100	—	1000	ns
MPUCLK "H" pulse width	$t_{HCLK}$	20	$1/2 \times t_{CLK}$	—	ns
MPUCLK "L" pulse width	$t_{LCLK}$	20	$1/2 \times t_{CLK}$	—	ns
$\overline{\text{MEMCS}}$ address setup time	$t_{AMC}$	0	—	—	ns
$\overline{\text{MEMWR}}$ address setup time	$t_{AMW}$	0	—	—	ns
$\overline{\text{MEMCS}} \downarrow \rightarrow \overline{\text{MEMWR}} \downarrow$	$t_{MCMW}$	0	—	—	ns
$\overline{\text{MEMWR}} \downarrow \rightarrow$ Written data determination	$t_{MWD}$	—	—	$1.5 \times t_{osc}$	ns
$\overline{\text{MEMCS}} \downarrow \rightarrow$ Not Ready	$t_{MCR L}$	8	—	39	ns
$\overline{\text{MEMWR}} \downarrow \rightarrow$ Not Ready period	$t_{MWRL}$	$2 \times t_{osc} + 17$	—	$4 \times t_{osc} + 85 + t_{CLK}$	ns
MPUCLK $\uparrow \rightarrow$ READY	$t_{CRH}$	7	—	36	ns
READY $\uparrow \rightarrow$ $\overline{\text{MEMCS}}$ hold time	$t_{RMC}$	0	—	—	ns
READY $\uparrow \rightarrow$ $\overline{\text{MEMWR}}$ hold time	$t_{RMW}$	0	—	—	ns
READY $\uparrow \rightarrow$ Written data hold time	$t_{RDMW}$	0	—	—	ns
READY $\uparrow \rightarrow$ Address hold time	$t_{RA}$	0	—	—	ns

### 3.2.4.4

## 3.0 Electrical Characteristics

### 3.2.4.4 MEMRD Timing (Read from the VRAM)

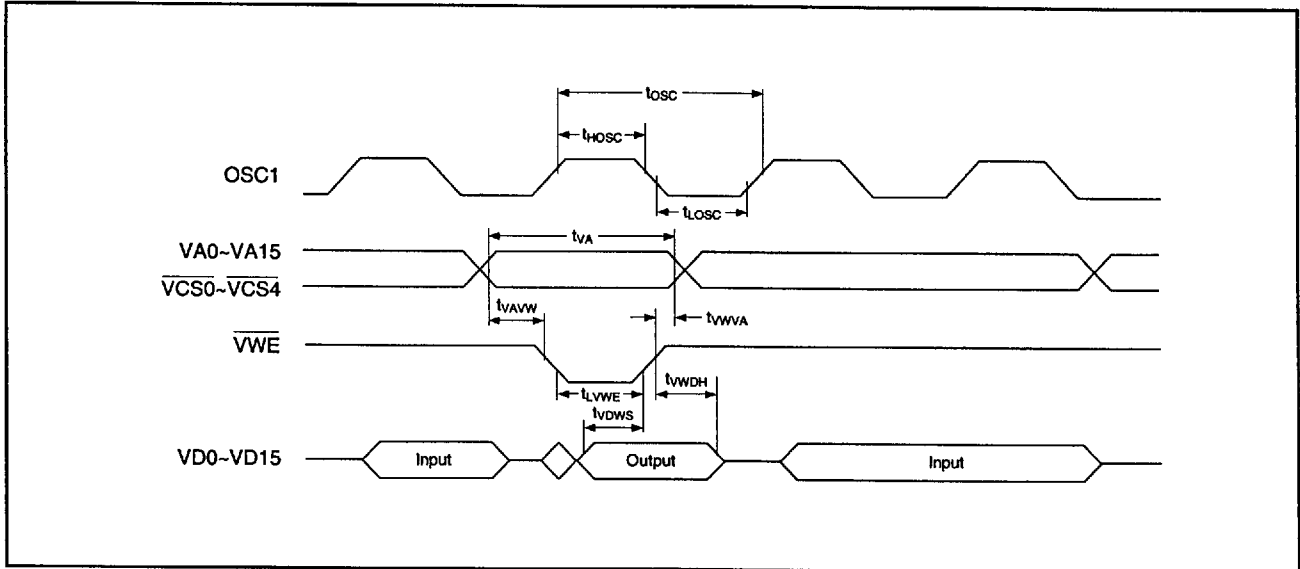


( $T_a = -20$  to  $75^\circ\text{C}$ )

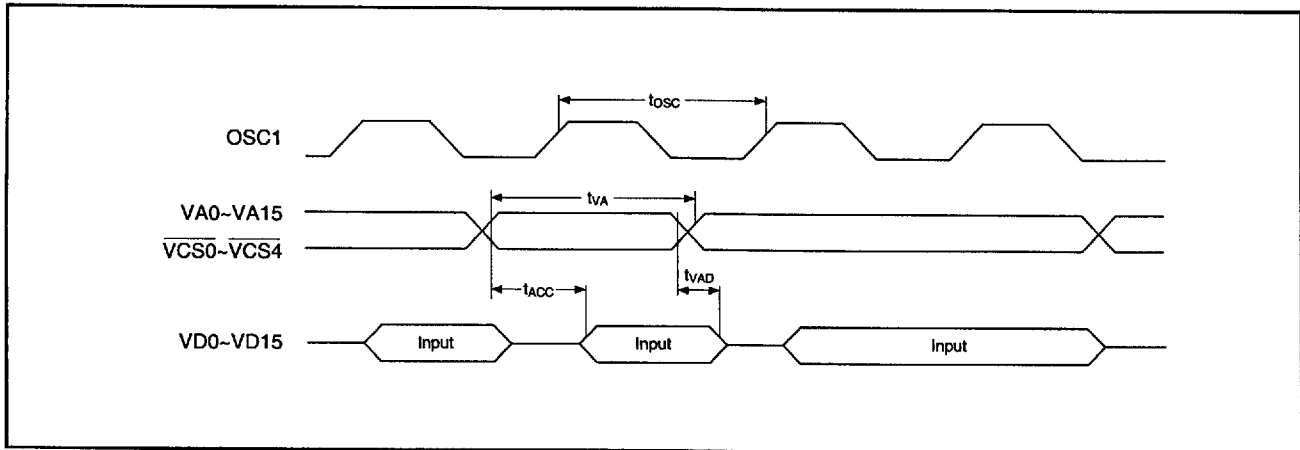
Parameter	Symbol	Min	Typ	Max	Unit
MPUCLK cycle	$t_{CLK}$	100	—	1000	ns
MPUCLK "H" pulse width	$t_{HCLK}$	20	$1/2 \times t_{CLK}$	—	ns
MPUCLK "L" pulse width	$t_{LCLK}$	20	$1/2 \times t_{CLK}$	—	ns
$\overline{MEMCS}$ address setup time	$t_{AMC}$	0	—	—	ns
$\overline{MEMRD}$ address setup time	$t_{AMR}$	0	—	—	ns
$\overline{MEMCS}\downarrow \rightarrow \overline{MEMRD}\downarrow$	$t_{MCMR}$	0	—	—	ns
$\overline{MEMCS}\downarrow \rightarrow$ Not Ready	$t_{MCRL}$	8	—	39	ns
$\overline{MEMRD}\downarrow \rightarrow$ Not Ready period	$t_{MRRL}$	$2 \times t_{osc} + 17$	—	$4 \times t_{osc} + 85 + t_{CLK}$	ns
MPUCLK $\uparrow \rightarrow$ Ready	$t_{CRH}$	7	—	36	ns
$\overline{MEMRD}\downarrow \rightarrow$ Read data determination	$t_{MRDA}$	$2 \times t_{osc}$	—	$4 \times t_{osc} + 76$	ns
Read data determination $\rightarrow$ READY $\uparrow$	$t_{DRMR}$	0	—	—	ns
$\overline{MEMRD}\uparrow \rightarrow$ Read data hold time	$t_{MRDH}$	0	—	—	ns
READY $\uparrow \rightarrow \overline{MEMCS}$ hold time	$t_{RMC}$	0	—	—	ns
READY $\uparrow \rightarrow \overline{MEMRD}$ hold time	$t_{RMR}$	0	—	—	ns
READY $\uparrow \rightarrow$ Address hold time	$t_{RA}$	0	—	—	ns

3.2.4.5 Timing of Interface with VRAM

3.2.4.5.1 Write to the VRAM



3.2.4.5.2 Read from the VRAM



### 3.2.4.5.3

## 3.0 Electrical Characteristics

### 3.2.4.5.3 Timing

(Ta = -20 to 75°C)

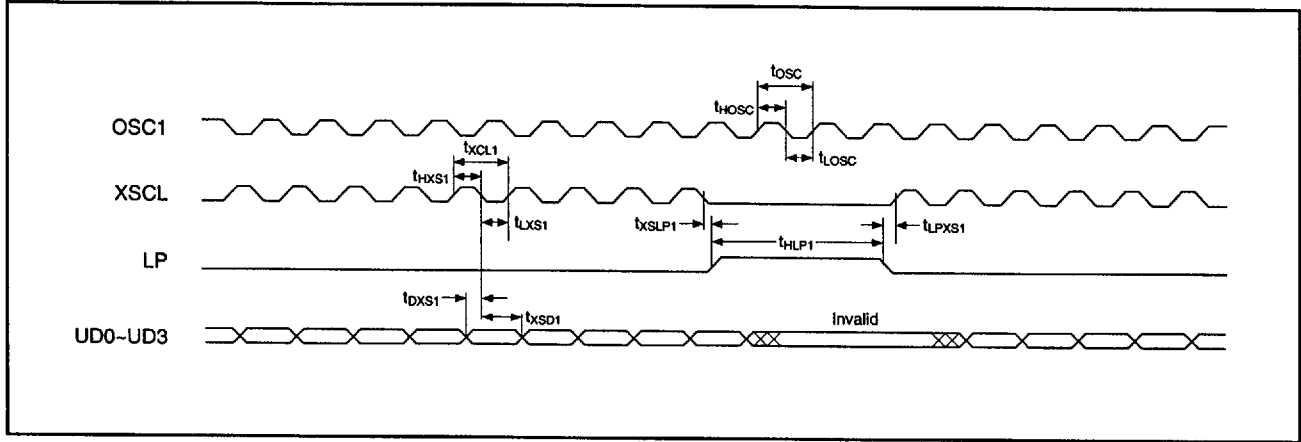
Parameter	Symbol	Min	Typ	Max	Unit
OSC1 cycle	t <sub>osc</sub>	100	—	500	ns
OSC1 "H" pulse width	t <sub>HOSC</sub>	—	1/2 × t <sub>osc</sub>	—	ns
OSC1 "L" pulse width	t <sub>LOSC</sub>	—	1/2 × t <sub>osc</sub>	—	ns
VWE address setup time	t <sub>VAVW</sub>	1/2 × t <sub>osc</sub> - 20	1/2 × t <sub>osc</sub>	—	ns
VWE address hold time	t <sub>VWVA</sub>	0	—	—	ns
VWE "L" pulse width	t <sub>LWVE</sub>	1/2 × t <sub>osc</sub> - 10	1/2 × t <sub>osc</sub>	—	ns
VWE data setup time	t <sub>VDWS</sub>	1/2 × t <sub>osc</sub> - 25	1/2 × t <sub>osc</sub>	—	ns
VWE data hold time	t <sub>VWDH</sub>	0	—	20	ns
VRAM address cycle time	t <sub>VA</sub>	t <sub>osc</sub>	—	—	ns
VRAM address access time	t <sub>ACC</sub>	—	—	t <sub>osc</sub> - 20	ns
VRAM read data hold time	t <sub>VAD</sub>	0	—	—	ns

## 3.0 Electrical Characteristics

### 3.2.4.6 – 3.2.4.6.1

#### 3.2.4.6 LCD Interface Timing

##### 3.2.4.6.1 Mode 1 (4-Bit transfer)



(Ta = -20 to 75°C)

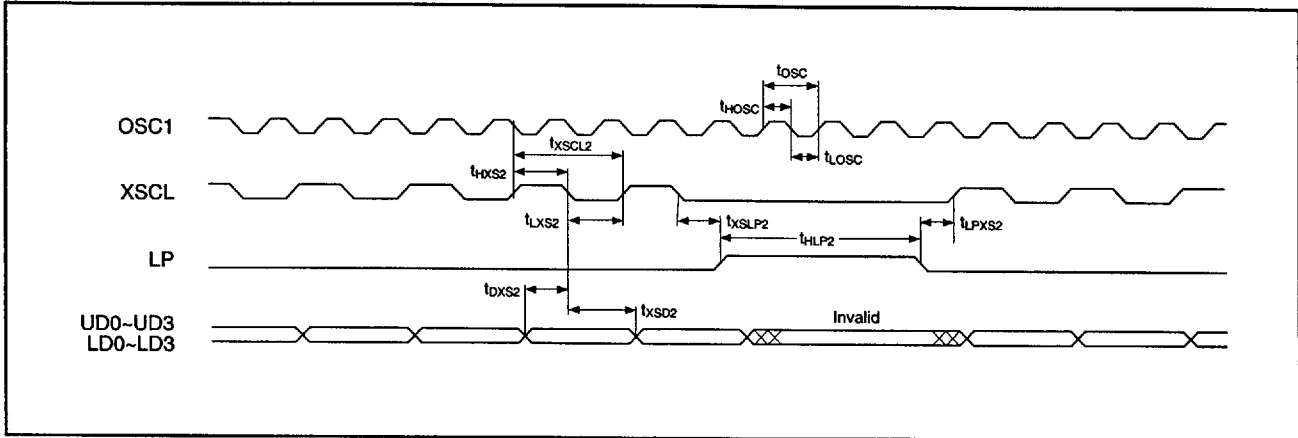
Parameter	Symbol	Min	Typ	Max	Unit
OSC1 clock cycle	$t_{OSC}$	1000	—	500	ns
OSC1 "H" pulse width	$t_{HOSC}$	$1/2 \times t_{OSC} - 10$	—	—	ns
OSC1 "L" pulse width	$t_{LOSC}$	$1/2 \times t_{OSC} - 10$	—	—	ns
XSCL cycle	$t_{XSCL1}$	—	—	—	ns
XSCL "H" pulse width	$t_{HXS1}$	$1/2 \times t_{OSC} - 10$	—	—	ns
XSCL "L" pulse width	$t_{LXS1}$	$1/2 \times t_{OSC} - 10$	—	—	ns
XSCL↓ → LP↑	$t_{XSCLP1}$	-10			
LP↓ → XSCL↑	$t_{LPXS1}$	$t_{OSC} - 10$			
Data determination → XSCL↓	$t_{DXS1}$	$1/2 \times t_{OSC} - 10$	—	—	ns
XSCL↓ → Data hold time	$t_{XSD1}$	$1/2 \times t_{OSC} - 20$	—	—	ns
LP "H" pulse width (Note 1)	$t_{HLP1}$	$(2n - 1/2) \times t_{OSC} - 20$	—	—	ns

**Note 1:** "n" indicates the LPW value (unit: number of characters)

### 3.2.4.6.2

## 3.0 Electrical Characteristics

### 3.2.4.6.2 Mode 1 (8-bit transfer), Mode 2, Mode 3 (4-bit transfer), Mode 5



( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
OSC1 clock cycle	$t_{osc}$	100	—	500	ns
OSC1 "H" pulse width	$t_{hosc}$	$1/2 \times t_{osc} - 10$	—	—	ns
OSC1 "L" pulse width	$t_{losc}$	$1/2 \times t_{osc} - 10$	—	—	ns
XSCL cycle	$t_{xscl2}$	$2 \times t_{osc} - 20$	—	—	ns
XSCL "H" pulse width	$t_{hxs2}$	$t_{osc} - 10$	—	—	ns
XSCL "L" pulse width	$t_{lxs2}$	$t_{osc} - 10$	—	—	ns
XSCL $\downarrow$ $\rightarrow$ LP $\uparrow$	$t_{xslp2}$	$1/2 \times t_{osc} - 10$	—	—	ns
LP $\downarrow$ $\rightarrow$ XSCL $\uparrow$	$t_{lpxs2}$	$t_{osc} - 10$	—	—	ns
Data determination $\rightarrow$ XSCL $\downarrow$	$t_{dxs2}$	$t_{osc} - 10$	—	—	ns
XSCL $\downarrow$ $\rightarrow$ data hold time	$t_{xsd2}$	$t_{osc} - 20$	—	—	ns
LP "H" pulse width (Note 1)	$t_{hlp2}$	$(2n - 1/2) \times t_{osc} - 20$	—	—	ns
LP "H" pulse width (Note 2)		$(4n - 1/2) \times t_{osc} - 20$	—	—	ns

Notes 1 and 2: "n" is the LPW value (unit: number of characters).

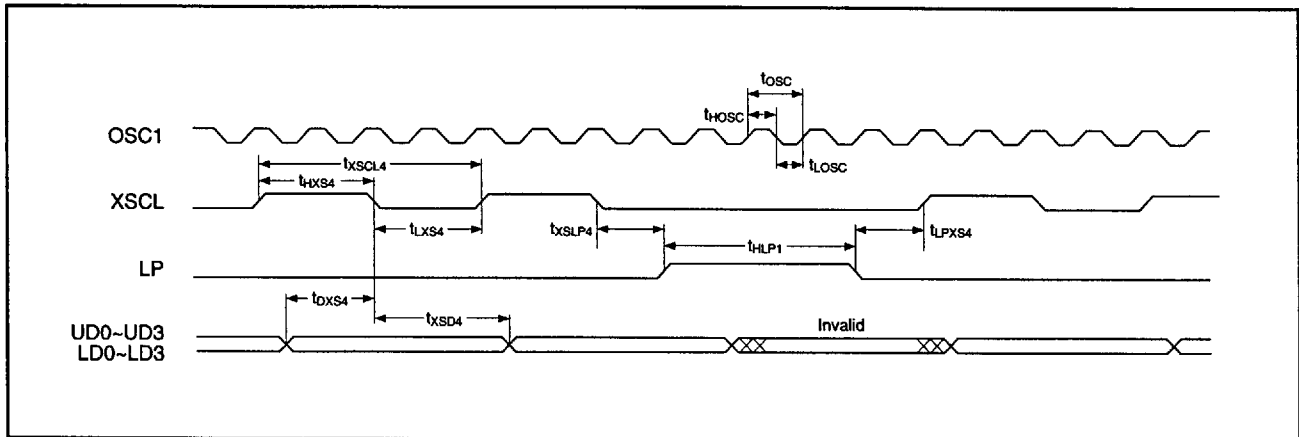
Note 1: Applies to display mode Nos. 1 (8-bit transfer) and 2.

Note 2: Applies to display mode Nos. 3 (4-bit transfer) and 5.

## 3.0 Electrical Characteristics

### 3.2.4.6.3

#### 3.2.4.6.3 Mode 3 (6-bit transfer), Mode 4, Mode 6



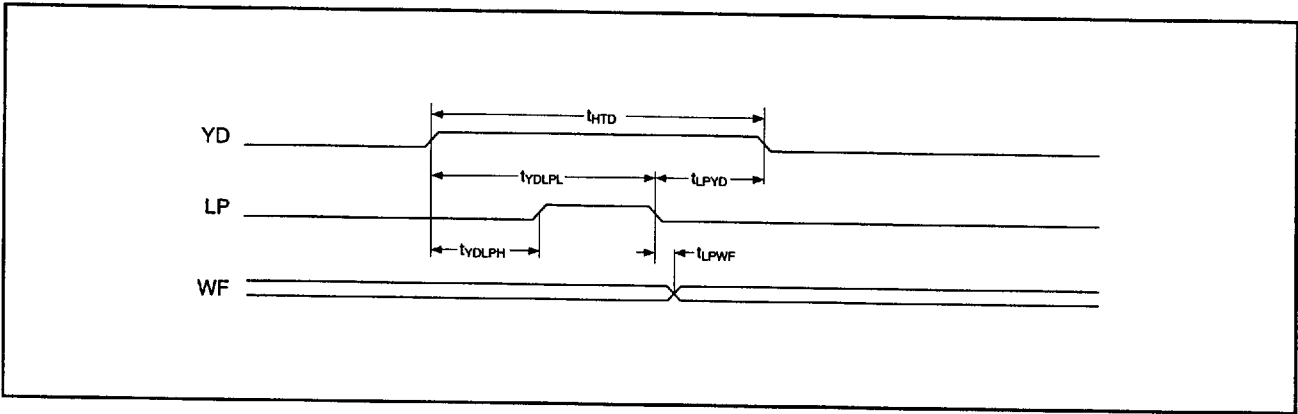
( $T_a = -20$  to  $75^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
OSC1 clock cycle	$t_{osc}$	100	—	500	ns
OSC1 "H" pulse width	$t_{hosc}$	$1/2 \times t_{osc} - 10$	—	—	ns
OSC1 "L" pulse width	$t_{losc}$	$1/2 \times t_{osc} - 10$	—	—	ns
XSCL cycle	$t_{xscl4}$	$4 \times t_{osc} - 20$	—	—	ns
XSCL "H" pulse width	$t_{hxs4}$	$2 \times t_{osc} - 20$	—	—	ns
XSCL "L" pulse width	$t_{lxs4}$	$2 \times t_{osc} - 20$	—	—	ns
XSCL $\downarrow$ $\rightarrow$ LP $\uparrow$	$t_{xslp4}$	$1.5 \times t_{osc} - 10$	—	—	ns
LP $\downarrow$ $\rightarrow$ XSCL $\uparrow$	$t_{lpxs4}$	$t_{osc} - 10$	—	—	ns
Data determination $\rightarrow$ XSCL $\downarrow$	$t_{dxs4}$	$2 \times t_{osc} - 20$	—	—	ns
XSCL $\downarrow$ $\rightarrow$ data hold time	$t_{xsd4}$	$2 \times t_{osc} - 20$	—	—	ns
LP "H" pulse width (Note 1)	$t_{hlp4}$	$(4n - 1/2) \times t_{osc} - 20$	—	—	ns

**Note 1.** "n" indicates the LPW value (unit: number of characters).



3.2.4.6.4 Sync Timing



(Ta = -20 to 75°C)

Parameter	Symbol	Min	Typ	Max	Unit
YD "H" pulse width	(Note 1)	$t_{HYD}$	—	—	ns
	(Note 2)				
YD↑ → LP↑	(Note 1)	$(m + n) 2 \times t_{osc} - 20$	—	—	ns
	(Note 2)	$(m + n) 4 \times t_{osc} - 20$	—	—	ns
YD↑ → LP↓	(Note 1)	$4.5 \times t_{osc} - 20$	—	—	ns
	(Note 2)	$5.5 \times t_{osc} - 20$	—	—	ns
YD↑ → LP↓	(Note 1)	$(n + 2) 2 \times t_{osc} - 20$	—	—	ns
	(Note 2)	$(n + 5/4) 4 \times t_{osc} - 20$	—	—	ns
LP↓ → YD↓	(Note 1)	$(m - 2) 2 \times t_{osc} - 20$	—	—	ns
	(Note 2)	$(m - 5/4) 4 t_{osc} - 20$	—	—	ns
LP↓ → WF↑↓	$t_{LPWF}$	-100	—	100	ns

"m" indicates the C/R value (unit: number of characters)

"n" indicates the LPW value (unit: number of characters)

1. Applies to display mode Nos. 1 and 2.
2. Applies to display mode Nos. 3, 4, 5 and 6.

# 4.0

## *Internal Registers*

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4.0 INTERNAL REGISTERS

The SED1351F is configured and controlled via an internal 14-register set, mapped into the MPU's I/O space. The address of each register is defined by AB0-AB3.

4.1 SUMMARY

Table 3. Control Registers

Type of Register		I/O Address				Data								R/W	Function
No.	Name	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
R1	Mode register	0	0	0	1	DISP	REV	PANEL	OR	GRAY	4/8	LCDE	RAMS	W	Sets SED1351 basic operational mode.
R2	Line Byte Count register	0	0	1	0	C/R								W	Sets number of horizontal display characters per line.
R3	Horizontal sync pulse width register	0	0	1	1	LPW								W	Sets width of LP pulse.
R4	Total display	0	1	0	0	SLTL								W	Sets total number of displayed lines (the low-order 8 bits in SLTL and the high-order 2 bits in SLTH).
R5	line count register	0	1	0	1	*	*	*	*	*	*	SLTH		W	
R6	Screen 1 display start address register	0	1	1	0	SAD1L								R/W	Sets start address of screen 1 (the low-order 8 bits in SAD1L and the high-order 8 bits in SAD1H).
R7	register	0	1	1	1	SAD1H								R/W	
R8	Screen 2 display start address register	1	0	0	0	SAD2L								R/W	Sets start address of screen 2 (the low-order 8 bits in SAD2L and the high-order 8 bits in SAD2H).
R9	register	1	0	0	1	SAD2H								R/W	
R10	Screen 1 display	1	0	1	0	SL1L								W	Sets number of displayed lines in screen 1 (the low-order 8 bits in SL1L and the high-order 4 bits in SL1H).
R11	line count register	1	0	1	1	*	*	*	*	*	*	SL1H		W	
R13	Address pitch adjustment register	1	1	0	1	APADJ								W	Set when a virtual screen is configured.
R14	Gray scale registers conversion	1	1	1	0	GS1								W	Sets gray level for gray-scale display. (C1, C0) = (0, 1) → GS1 (C1, C0) = (1, 0) → GS2
R15		1	1	1	1	GS2								W	

## 4.2 REGISTER DESCRIPTION

### 4.2.1 R1 Mode Register

This register determines the basic configuration of the SED1351F.

Table 4. R1: Mode Register

I/O Address				Data								R/W
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	DISP	REV	PANEL	OR	GRAY	4/8	LCDE	RAMS	W

- **DISP**

- DISP = 0: Display OFF
- DISP = 1: Display ON

Selects display on/off. DISP goes to 0 on RESET. If inverse video is selected (R1:D6=1) then setting the display OFF causes data 1's to be output to the LCD.

- **REV**

- REV = 0: Normal display
- REV = 1: Inverse display

Selects normal/inverse display. REV goes to 0 on RESET. If back lit LCDs are used in the system REV should be set to 1.

- **PANEL**

- PANEL = 1: Dual LCD panel drive
- PANEL = 0: Single LCD panel drive

Selects the LCD panel configuration. PANEL goes to 0 on RESET.

- **OR**

- OR = 1: Single display of ORed data
- OR = 0: Display split into two screens

Selects one of two display modes in a single LCD system (PANEL = 0).

- The display is split into two screens, with each screen being allocated a block of data in display memory (Set by SAD1 and SAD2. See description of R6, R7, R8 and R9).
- A single screen is generated, made up of a bit-wise OR of the data in block 1 with that in block 2.

OR goes to 0 on RESET. If PANEL = 1, the contents of OR are ignored.

- **GRAY**

- GRAY = 1: Gray scale display
- GRAY = 0: "B&W" display

Selects between 2-level "B&W" or 4-level gray-scale display. GRAY goes to 0 on RESET. When a gray-scale display is selected, two bits of video memory data are used for the display of each pixel, using the conversion specification set by the contents of R14 and R15.

- **$\bar{4}/8$**

- $\bar{4}/8$  = 1: 8 bit data transfer
- $\bar{4}/8$  = 0: 4 bit data transfer

Selects between 4- and 8-bit display data widths for the LCD, in "B&W", single LCD mode. Gray-scale or dual LCD modes force 4-bit data width, irrespective of the contents of  $\bar{4}/8$ .  $\bar{4}/8$  goes to 0 on RESET.

- **LCDE**

- LCDE = 0: LCDENB =  $V_{SS}$ , and the LCD power is off.
- LCDE = 1: LCDENB =  $V_{DD}$ , and the LCD power is on.

This bit sets the output of the LCD control line, LCDENB. LCDE goes to 0 on RESET. This control bit, and its associated line, are intended for use in systems that implement LCD DC voltage protection, but LCDE can be used for other purposes if required.

- **RAMS**

- RAMS = 0: Addressing for  $8K \times 8$  SRAM's
- RAMS = 1: Addressing for  $32K \times 8$  SRAM's

Configure the video memory address lines. RAMS goes to 0 on RESET.

### 4.2.2 R2 Line Byte Count Register

This register sets the number of bytes per display line.

**Table 5. Line Byte Count Register**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R2	0	0	1	0	C/R								W

The contents of R2 are given by  $C/R = (\text{No. of bytes}) - 1$

Since the maximum value of C/R is FFH, the maximum number of pixels in one display line is

- $256 \times 8 = 2048$  in "B&W" mode
- or  $256 \times 4 = 1024$  in gray-scale mode

### 4.2.3 R3 Horizontal Sync Pulse Width Register

This register sets LPW, the width of the horizontal sync pulse (LP), which is output at the end of every line. LPW has units of "time per byte",  $t_b$ , and the contents of R3 are given by  $LPW = (\text{Pulsewidth}) - 1$ . "time per byte" is  $2/f_{osc}$  for single LCD, single screen configurations, and  $4/f_{osc}$  for all other configurations.

Note that LPW partially determines the period of one line, and hence affects the frame period.

**Table 6. Horizontal Sync Pulse Width Register**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R3	0	0	1	0	LPW								W

### 4.2.4 R4, R5 Total Display Line Count Registers

This register sets the number of display lines on an LCD panel. The data is 10 bits long. The low order 8 bits are contained in R4, the high order 2 bits in R5.

**Table 7. Total Display Line Count Register**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R4	0	1	0	0	SLTL								W
R5	0	1	0	1	*	*	*	*	*	*	SLTH		W

The contents of R4 and R5 are given by  $SLT = (\text{No. of lines}) - 1$ . Since SLT sets the number of display lines on one LCD, in dual panel mode the actual number of display lines is twice the value of (SLT). Note that SLT partially determines the frame period, and hence affects the display duty cycle. The display duty cycle is  $1 / (SLT + VR)$  where VR, the vertical retrace period, is equal to 2. It is during the vertical retrace period that the polarity of the LCD drive waveforms are inverted.

### 4.2.5 R6, R7 Screen 1 Display Start Address Registers

These registers set SAD1, the start address in video memory, of screen 1. The data width is 16 bits. The low-order byte is contained in R6, the high-order byte in R7.

**Table 8. Screen 1 Display Start Address Registers**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R6	0	1	1	0	SAD1L								R/W
R7	0	1	1	1	SAD1H								R/W

Screen 1 is the upper screen in 2-screen and dual-panel, dual-drive LCD mode, or the top layer in ORed mode.

### 4.2.6 R8, R9 Screen 2 Display Start Address Registers

These registers set SAD2 the start address, in video memory, of screen 2. The data width is 16 bits. The low-order word is contained in R8, the high-order word in R9.

**Table 9. Screen 2 Display Start Address Registers**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R8	1	0	0	0	SAD2L								R/W
R8	0	1	1	1	SAD2H								R/W

Screen 2 is the lower screen in split screen and dual LCD-panel modes, or the bottom layer in ORed mode.



### 4.2.7 R10, R11 Screen 1 Display Line Count Registers

These registers set the number of display lines on screen 1. The data width is 10 bits. The lower 8 bits are contained in R10, the upper 2 bits in R11.

**Table 10. Screen 1 Display Line Count Register**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R10	1	0	1	0	SL1L								W
R11	1	0	1	1	*	*	*	*	*	*	SL1H		W

The contents of R10 and R11 are given by  $SL1 = (\text{No. of lines}) - 1$ . The contents of these registers are only meaningful in single-panel, single-drive LCD mode and when  $R1:OR=0$ , being otherwise ignored. Note that single screen mode can be forced by setting  $SL1=SLT$  in single LCD-panel mode, as well as by setting  $R1:OR=1$ .

### 4.2.8 R13 Address Pitch Adjustment Register

The contents of this register set the numerical difference between the last address of a display line, and the first address in the following display line.

**Table 11. Address Pitch Adjustment Register**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R13	1	1	0	0	APADJ								W

If APADJ is not equal to zero, then a virtual screen with a line length of  $(C/R + APADJ)$  bytes is created, with the display reflecting the contents of a window  $(C/R + 1)$  bytes wide. The position of the window on the virtual screen is determined by SAD1 and SAD2.

## 4.2.9 R14, R15 Gray-Scale Conversion Registers

The contents of these registers determine the two intermediate gray levels, GS1 and GS2, associated with the bit patterns (0,1) and (1,0) respectively, when the display is in 4-level gray-scale mode.

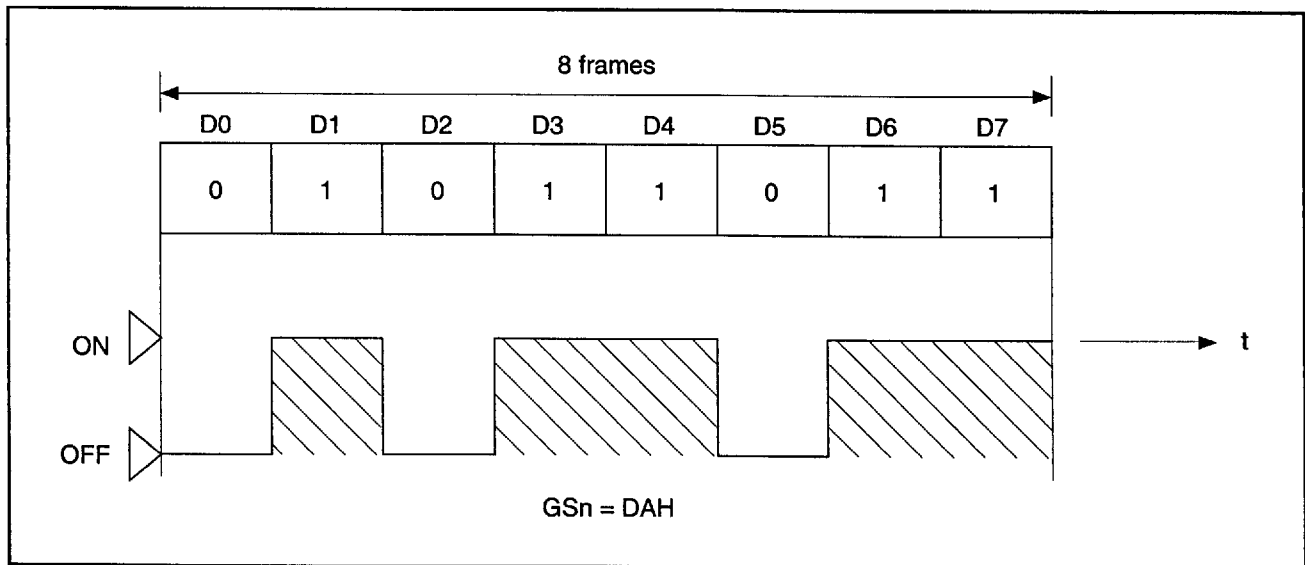
**Table 12. Gray-Scale Conversion Register**

R No.	I/O Address				Data								R/W
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R14	1	1	1	0	GS1								W
R15	1	1	1	1	GS2								W

**Table 13. Gray Scale Display**

C1	C0	Contents of Display
0	0	Display off
0	1	Gray display based on GS1 conversion code
1	0	Gray display based on GS2 conversion code
1	1	Display on

Note that intensity differences are produced by turning off a particular pixel during selected frames in an 8 frame cycle. Each bit in GS1 and GS2 corresponds to 1 frame in this 8 frame cycle, and if the bit is zero, the pixel will be off for that frame.



**Figure 3. Gray Scale Display Implementation**

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# 5.0

## *Display Modes*

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## 5.0 DISPLAY MODES

The SED1351F has six basic operational modes, Mode 1 to 6, which are configured by the contents of R1, the Mode Register.

Table 14. Display Modes

Mode No.	Mode Register (R1)								Configuration				
	D7	D6	D5	D4	D3	D2	D1	D0	N = LCD's	Screen	Video	Output Data Width	
1	*	*	0	0	0	0	*	*	1	Split	B&W	4 bit	
	*	*	0	0	0	1	*	*				8 bit	
2	*	*	0	0	1	X	*	*			OR	Gray	4 bit
3	*	*	0	1	0	0	*	*				B&W	4 bit
	*	*	0	1	0	1	*	*		8 bit			
4	*	*	0	1	1	X	*	*		Gray	4 bit		
5	*	*	1	X	0	X	*	*	2	1 per LCD	B&W	4 bit	
6	*	*	1	X	1	X	*	*			Gray		

\* : Don't care

X : Ignored

### 5.1 MODE 1

- Single-panel, single-drive LCD
- Split display
- B&W display

Table 15. Display Mode 1

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	PANEL	OR	GRAY	4/8	LCDE	RAMS
*	*	0	0	0	*	*	*

An example setting for a 640 pixel × 200 line LCD panel is:

- C/R = 4FH
- LPW = 75H
- SLT = 00C7H
- SAD1 = 0000H
- SAD2 = 3E80H
- SL1 = 0063H
- APADJ = 00H

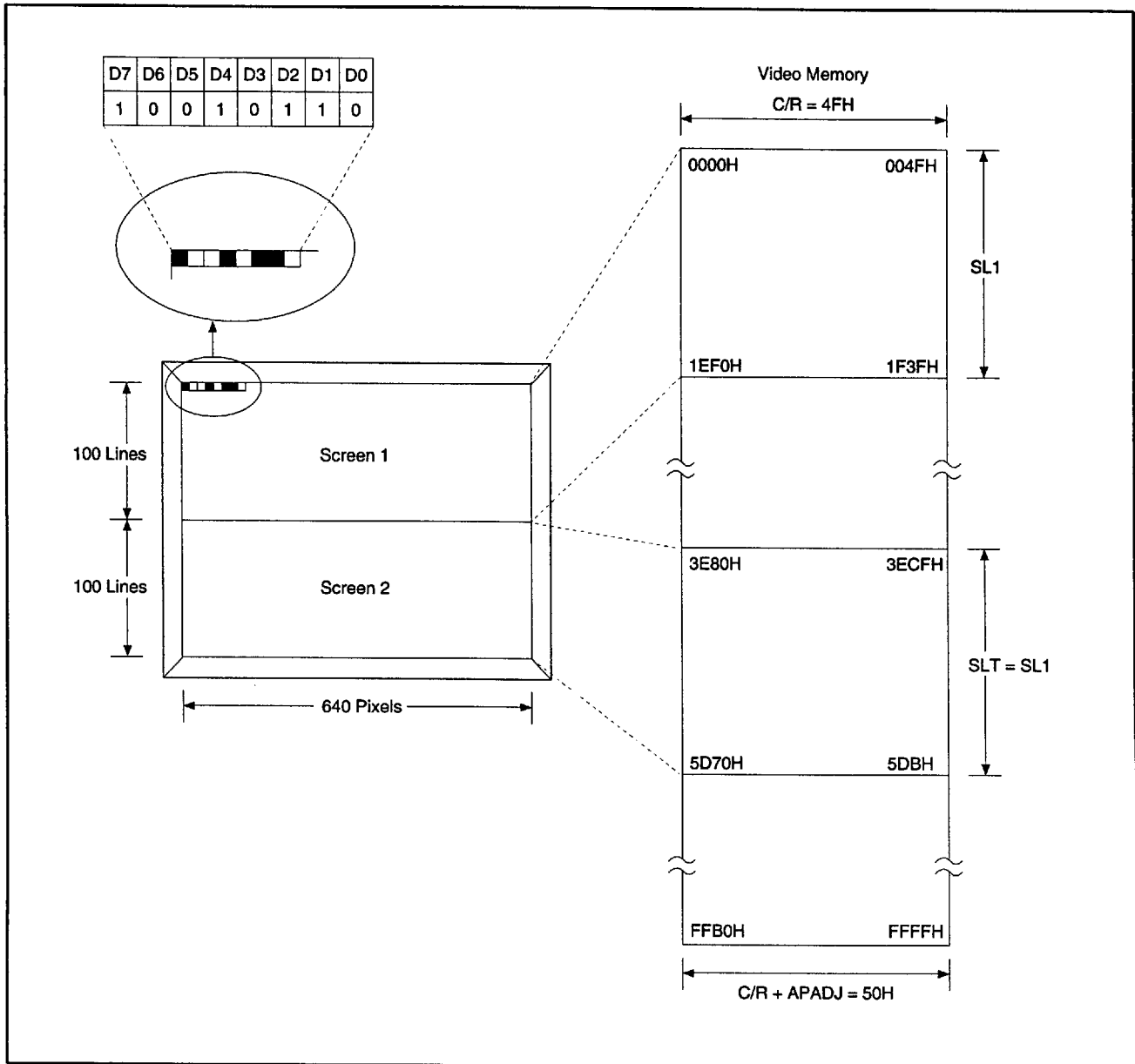
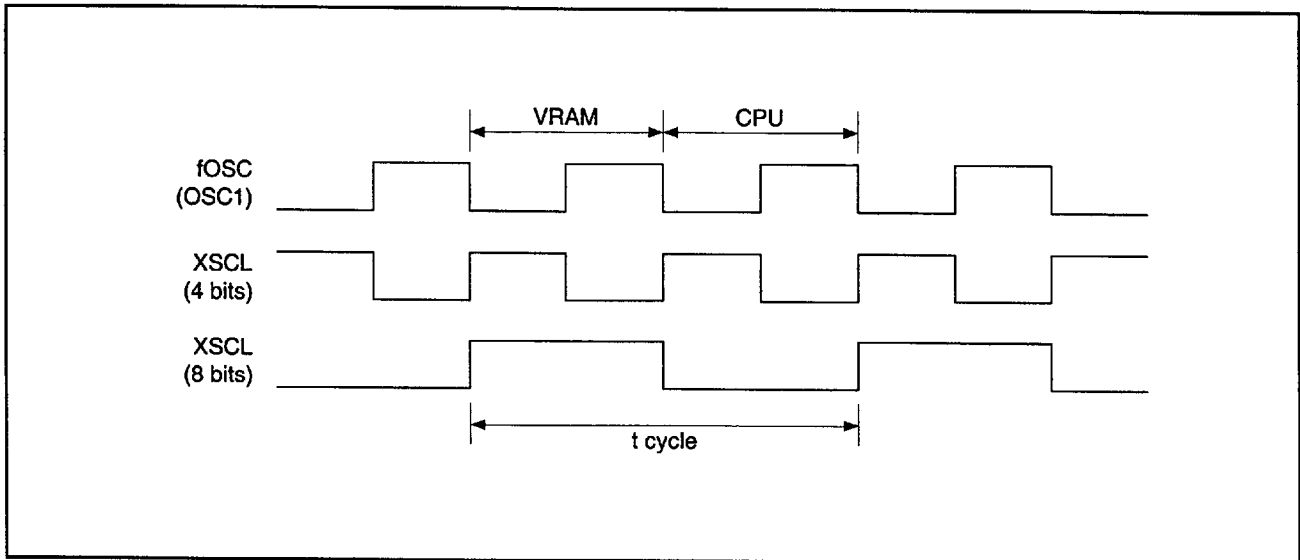


Figure 4. Display vs. VRAM: Mode 1

**Mode 1 basic timing:**



**Figure 5. Basic Timing: Mode 1**

A basic cycle consists of two cycles of  $f_{osc}$ ; during the first cycle data is read from video memory by the controller, during the second cycle data is prepared for CPU access to VRAM.

The period of 1 horizontal line is given by  $t_H = 2 / f_{osc} \times (C/R + LPW)$  and the period of 1 frame is given by  $t_{FR} = t_H \times (SLT + 2)$ .

For example:

- $t_{FR} = 16$  msec ( $f_{FR} = 62.5$  Hz)
- $f_{osc} = 5$  Hz

then

$$16 \times 10^{-3} = t_H \times (200 + 2)$$

$$\therefore t_H = 7.92 \times 10^{-5} \text{s}$$

$$7.92 \times 10^{-5} = \frac{2}{5 \times 10^6} \times (80 + LPW)$$

$$\therefore LPW \approx 118 \text{ characters (75H)}$$

Note that it is possible to fix LPW and then calculate  $f_{osc}$ . If this is done the relationship below, between  $f_{osc}$  and the VRAM access time, must hold.

$$t_{acc} \leq \frac{1}{f_{osc} \text{ (MHz)}} - 20\text{ns}$$



### 5.2 MODE 2

- Single-panel, single-drive LCD
- Split display
- Gray-scale display

**Table 16. Display Mode 2**

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	PANEL	OR	GRAY	4/8	LCDE	RAMS
*	*	0	0	1	*	*	*

An example setting for a 640 pixel by 200 line LCD panel is:

- C/R = 9FH
- LPW = 19H
- SLT = 00C7
- SAD1 = 1350H
- SAD2 = XXXX
- SL1 = 00C7H
- APADJ = 60H
- GS1 = 29H
- GS2 = DAH

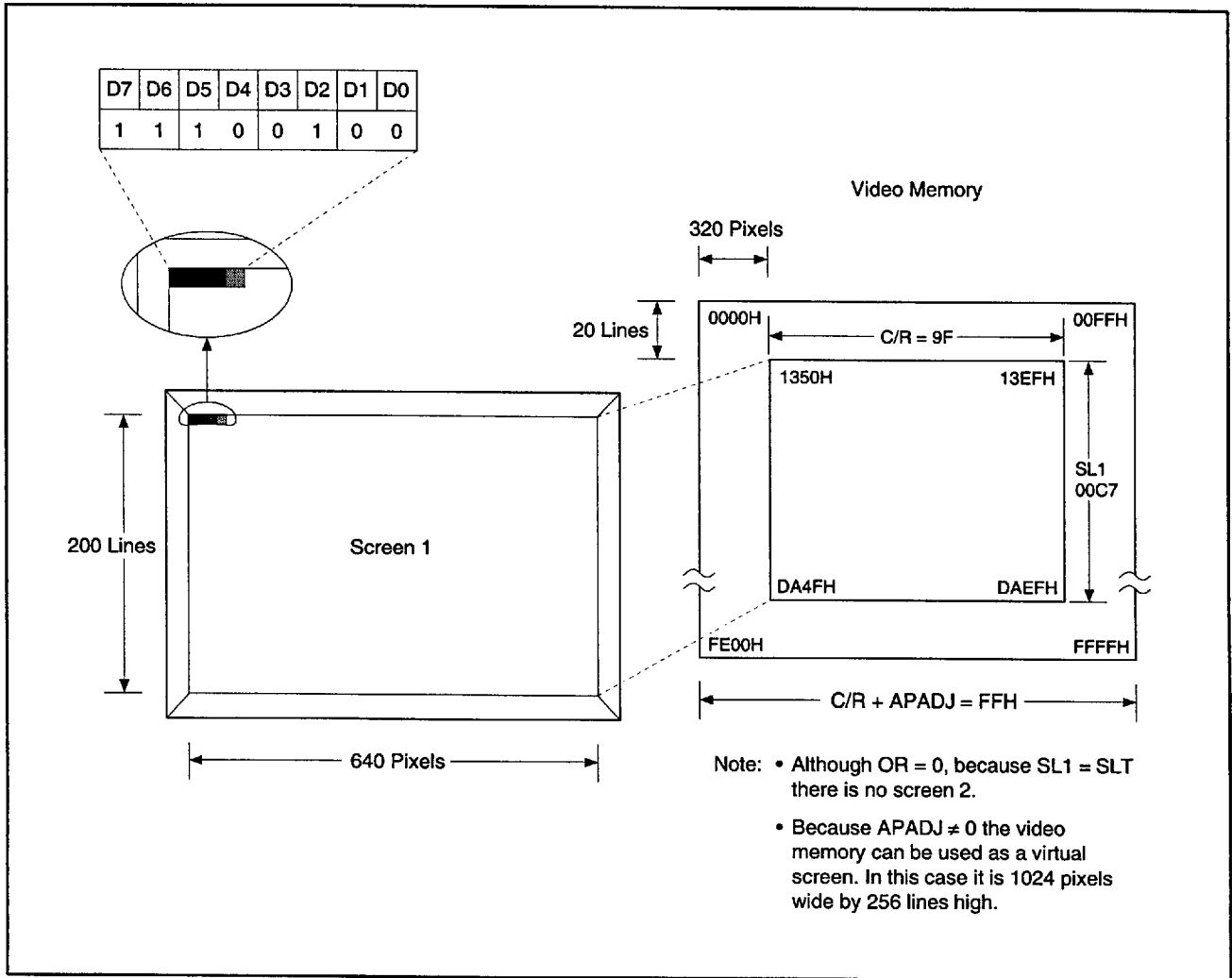


Figure 6. Display vs. VRAM: Mode 2

Mode 2 basic timing: See mode 1

For example:

- $t_{FR} = 12.5 \text{ msec}$  ( $f_{FR} = 80 \text{ Hz}$ )
- $f_{OSC} = 6 \text{ MHz}$

$$12.5 \times 10^{-3} = t_H \times (200 + 2)$$

$$\therefore t_H = 6.19 \times 10^{-5} \text{ s}$$

$$6.19 \times 10^{-5} = \frac{2}{6 \times 10^6} \times (160 + LPW)$$

$$\therefore LPW \approx 26 \text{ characters (19H)}$$

### 5.3 MODE 3

- Single-panel, single-drive LCD
- ORed layer display
- B&W display

**Table 17. Display Mode 3**

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	PANEL	OR	GRAY	$\bar{4}/8$	LCDE	RAMS
*	*	0	1	0	*	*	*

An example setting for a 640 pixel by 200 line LCD panel is:

- C/R = 4F
- LPW = 12H
- SLT = 00C7
- SAD1 = 0000H
- SAD2 = 3E80H
- APADJ = 00H

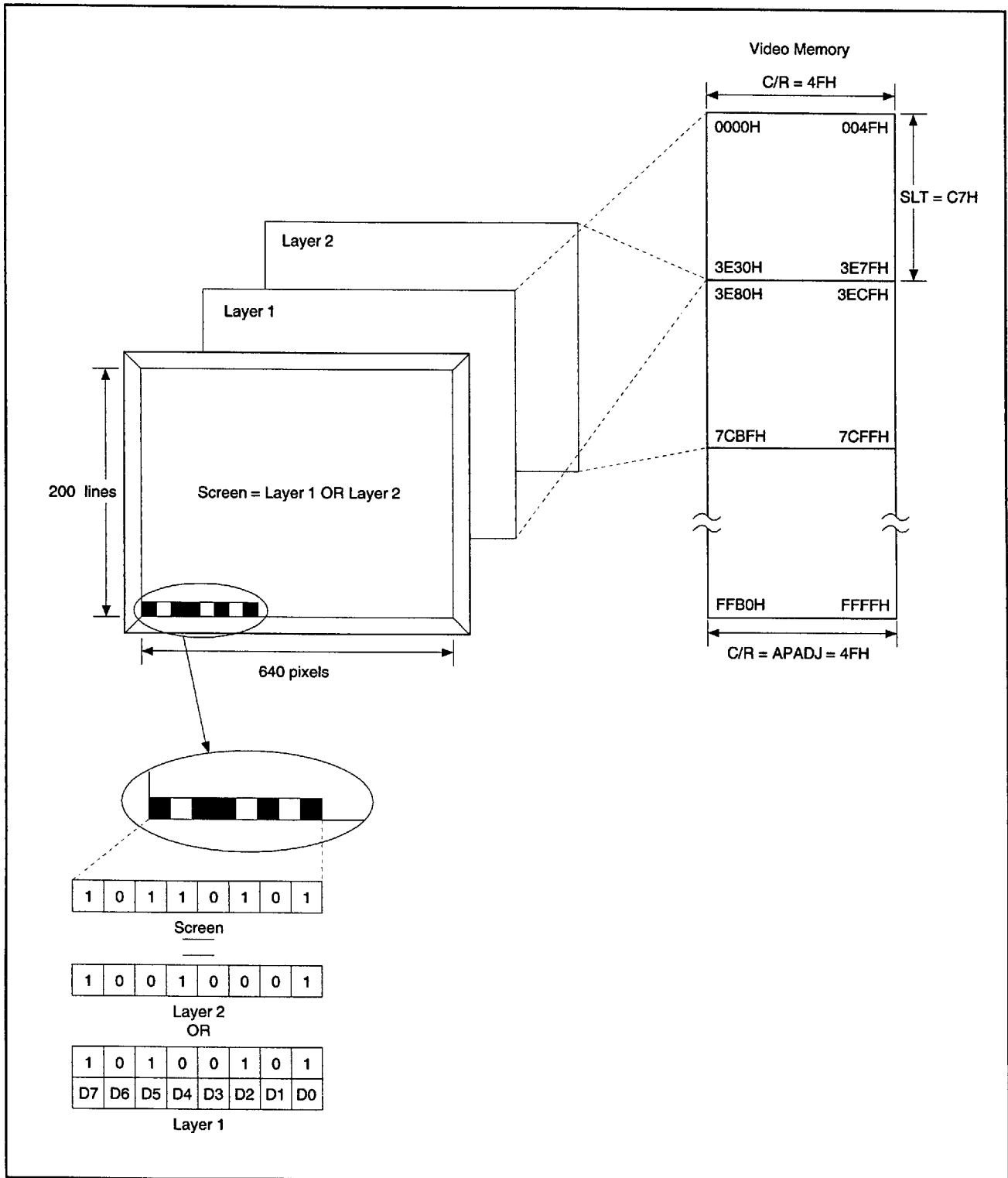


Figure 7. Display vs. VRAM: Mode 3

## Mode 3 basic timing:

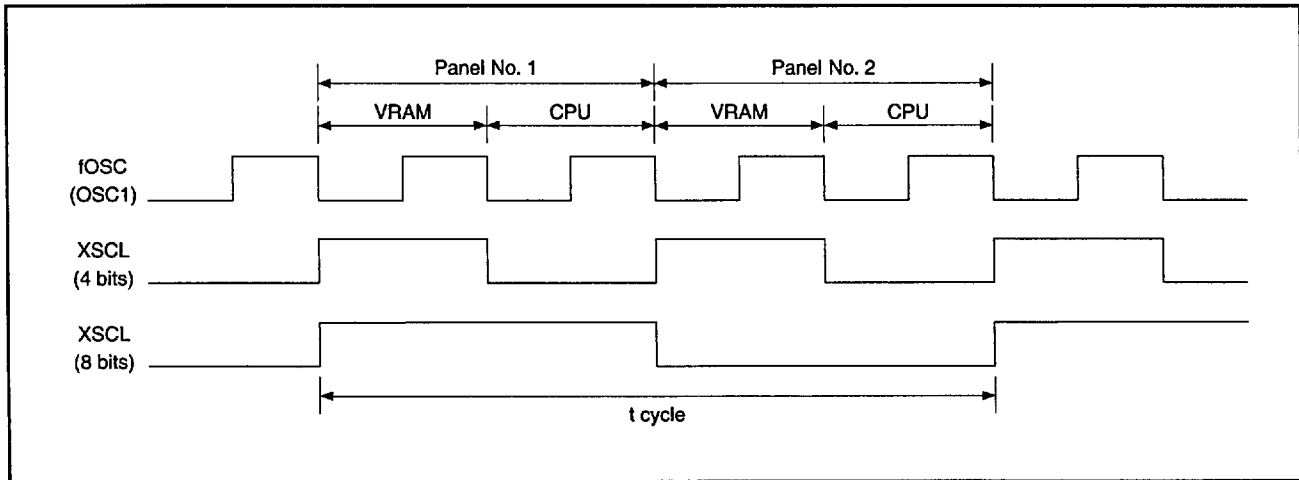


Figure 8. Basic Timing: Mode 3

For an ORed display one basic cycle is required for each layer, that is 4 cycles of  $f_{\text{osc}}$  are required for 1 basic period. The period of 1 horizontal line is given by  $t_H = (4 / f_{\text{osc}} \times (C/R + LPW))$  and the period of 1 frame by  $t_{FH} = (f_H) \times (SLT + 2)$ .

For example:

- $t_{FH} = 116 \text{ msec}$  ( $f_{FR} = 62.5 \text{ Hz}$ )
- $f_{\text{osc}} = 5 \text{ MHz}$

$$16 \times 10^{-3} = t_H \times (200 + 2)$$

$$\therefore t_H = 7.92 \times 10^{-5} \text{ s}$$

$$7.92 \times 10^{-5} = \frac{4}{5 \times 10^6} \times (80 + LPW)$$

$$\therefore LPW \approx 19 \text{ characters (12H)}$$

## 5.4 MODE 4

- Single-panel, single-drive LCD
- ORed layer display
- Gray-scale display

**Table 18. Display Mode 4**

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	PANEL	OR	GRAY	$\overline{4/8}$	LCDE	RAMS
*	*	0	1	1	*	*	*

An example setting for a 640 pixel × 200 line LCD panel is:

- C/R = 9FH
- LPW = 18HSLT = 00C7H
- SAD1 = 0000H
- SAD2 = 7D00H
- APADJ = 00H
- GS1 = 29H
- GS2 = D5H

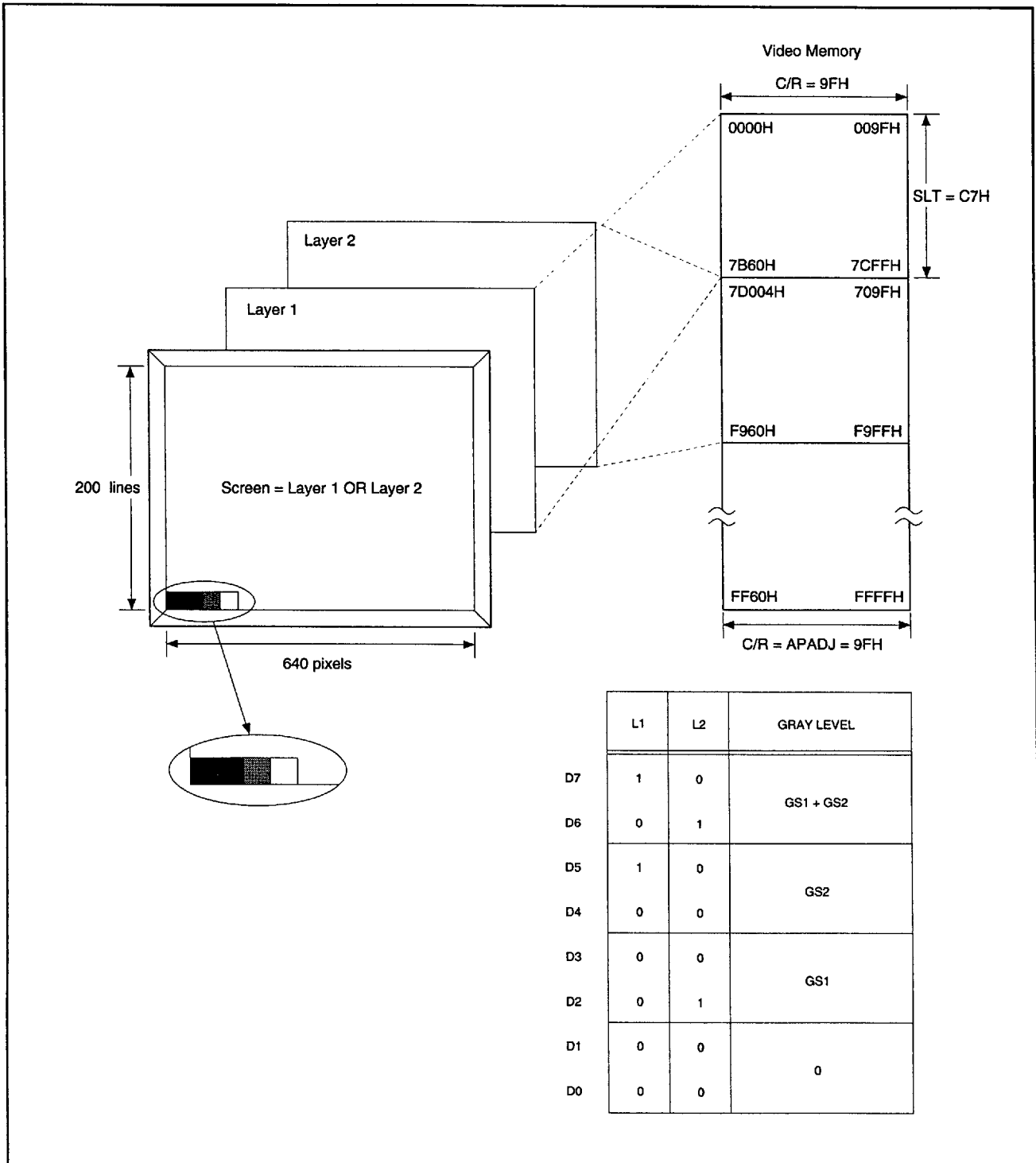


Figure 9. Display vs. VRAM: Mode 4

**Mode 4 basic timing: See Mode 3**

For example:

- $t_{FR} = 14.3 \text{ ms}$  ( $f_{FR} = 70 \text{ Hz}$ )
- $f_{OSC} = 10 \text{ MHz}$

$$14.3 \times 10^{-3} = t_H \times (200 + 2)$$

$$\therefore t_H = 7.08 \times 10^{-5} \text{ s}$$

$$6.19 \times 10^{-5} = \frac{4}{12 \times 10^6} \times (160 + LPW)$$

$$\therefore LPW \approx 17 \text{ characters (10H)}$$

## 5.5 MODE 5

- Dual-panel, dual-drive LCD
- B&W display

**Table 19. Display Mode 5**

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	PANEL	OR	GRAY	4/8	LCDE	RAMS
*	*	1	X	0	X	*	*

An example setting for two 640 pixel × 200 line LCD panels is:

- C/R = 4FH
- LPW = 12H
- SLT = 0047H
- SAD1 = 0000H
- SAD2 = 3E80H
- APADJ = 00H



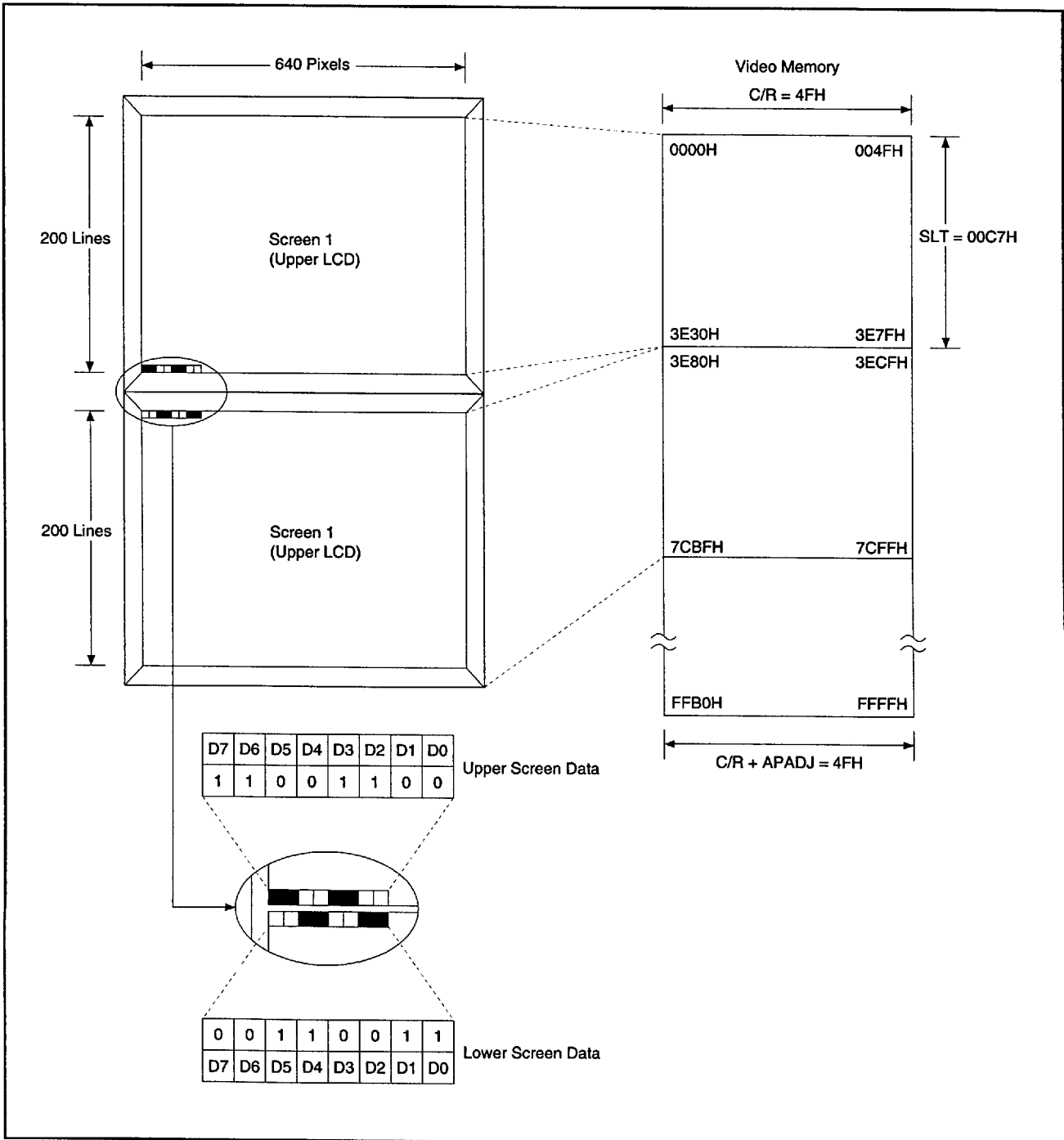
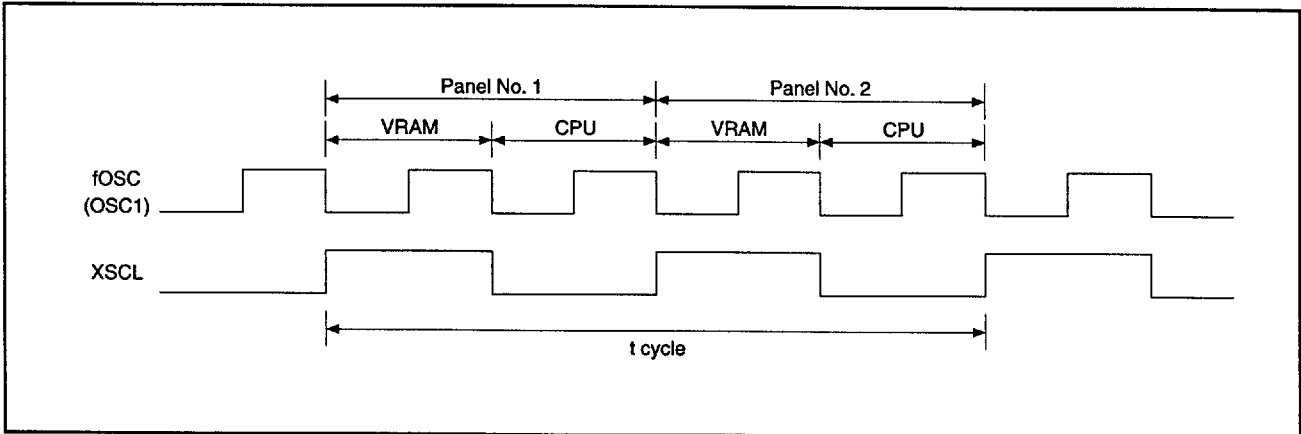


Figure 10. Display vs VRAM: Mode 5

**Mode 5 basic timing:**



**Figure 11. Basic Timing: Mode 5**

With a dual LCD-panel display chosen, one basic cycle is required for each of the panels, that is 4 f<sub>osc</sub> cycles. The line and frame periods are the same as for Mode 3.

For example:

- t<sub>FR</sub> = 16 msec (f<sub>FR</sub> = 62.5 Hz)
- f<sub>osc</sub> = 5 MHz

$$16 \times 10^{-3} = t_H \times (200 + 2)$$

$$\therefore t_H = 7.92 \times 10^{-5} \text{ s}$$

$$7.92 \times 10^{-5} = \frac{4}{5 \times 10^6} \times (80 + \text{LPW})$$

$$\therefore \text{LPW} \approx 19 \text{ characters (12H)}$$

## 5.6 Mode 6

- Dual-panel, dual-drive LCD
- Gray-scale display

Table 20. Display Mode 6

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	PANEL	OR	GRAY	$\overline{4/8}$	LCDE	RAMS
*	*	1	X	1	X	*	*

An example setting for two 640 pixel × 200 line LCD panels is:

- C/R = 9FH
- LPW = 18H
- SLT = 00C7H
- SAD1 = 0000H
- SAD2 = 7D00H
- APADJ = 00H
- GS1 = 29H
- GS2 = D5H

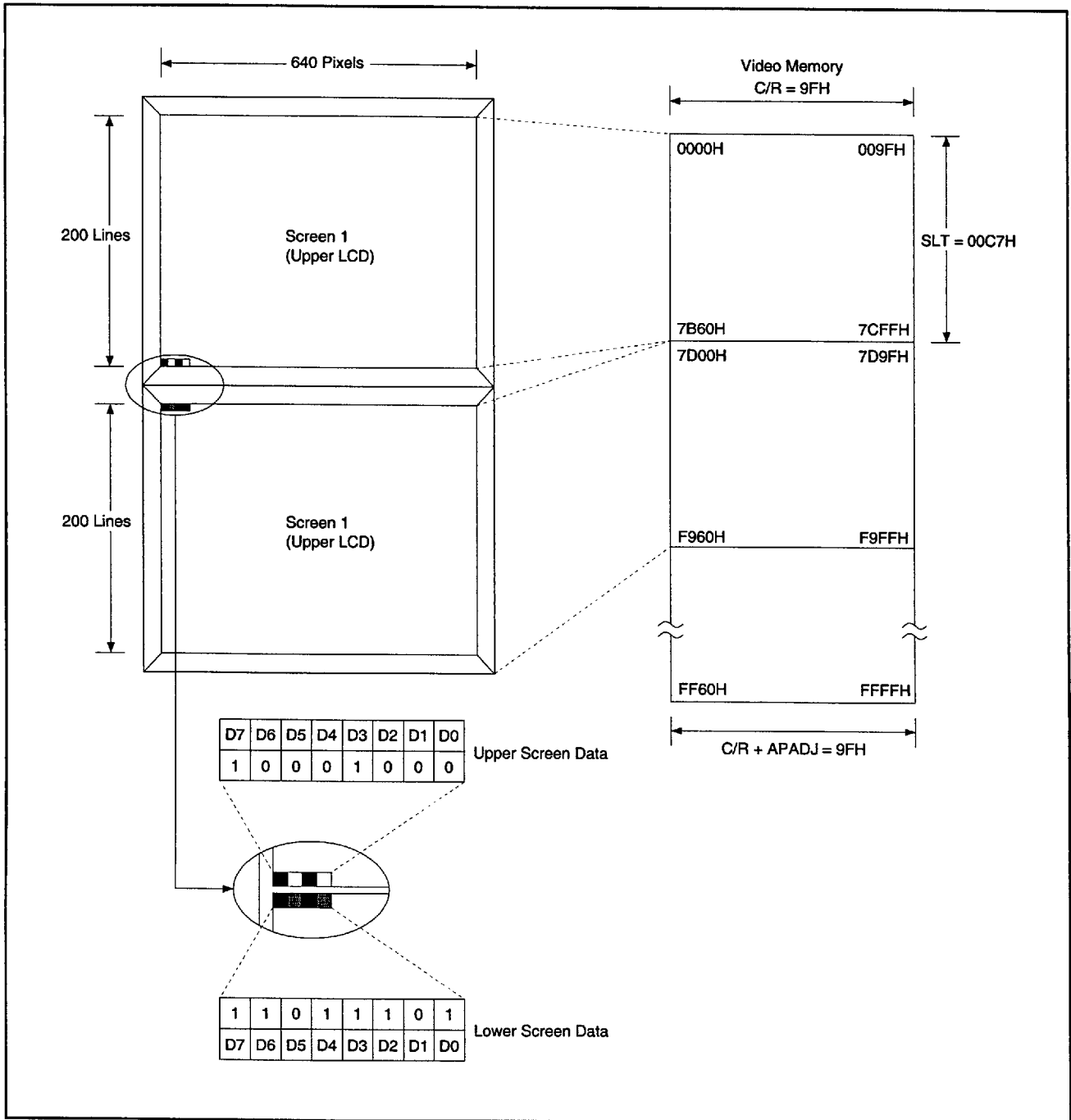


Figure 12. Display vs. VRAM: Mode 6

**Mode 6 basic timing: See Mode 5**

For example:

- $t_{FR} = 14.3 \text{ msec}$  ( $f_{FR} = 70 \text{ Hz}$ )
- $f_{osc} = 10 \text{ MHz}$

$$14.3 \times 10^{-3} = t_H \times (200 + 2)$$

$$\therefore t_H = 7.08 \times 10^{-5} \text{ s}$$

$$6.19 \times 10^{-5} = \frac{4}{12 \times 10^6} \times (160 + LPW)$$

$$\therefore LPW \approx 17 \text{ characters (10H)}$$

# **6.0**

## ***MPU Interface***

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# 6.0 MPU INTERFACE

## 6.1 8-BIT MPU INTERFACE

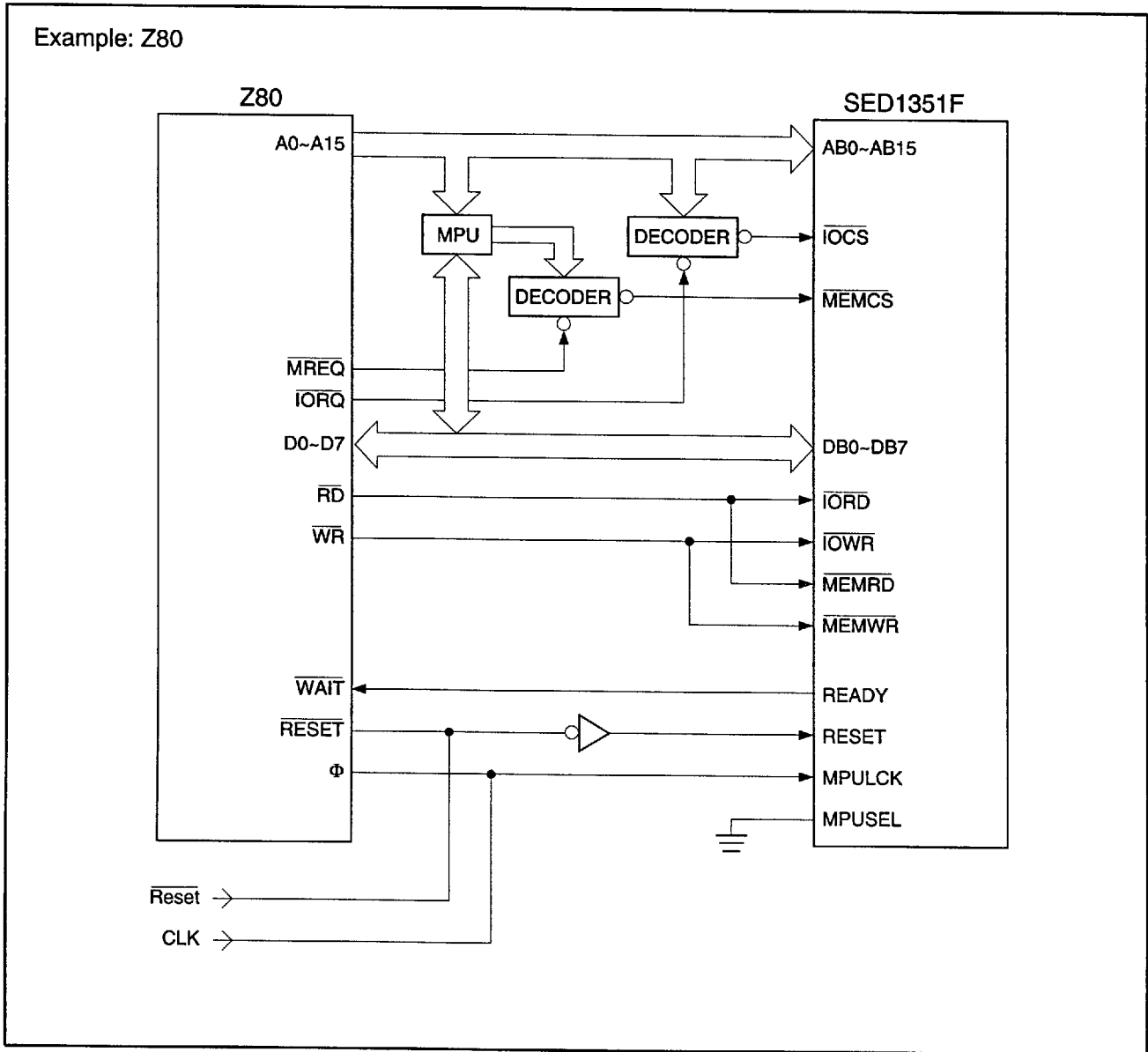


Figure 13. SED1351F/Z80 Interface



6.2 16-BIT MPU INTERFACE

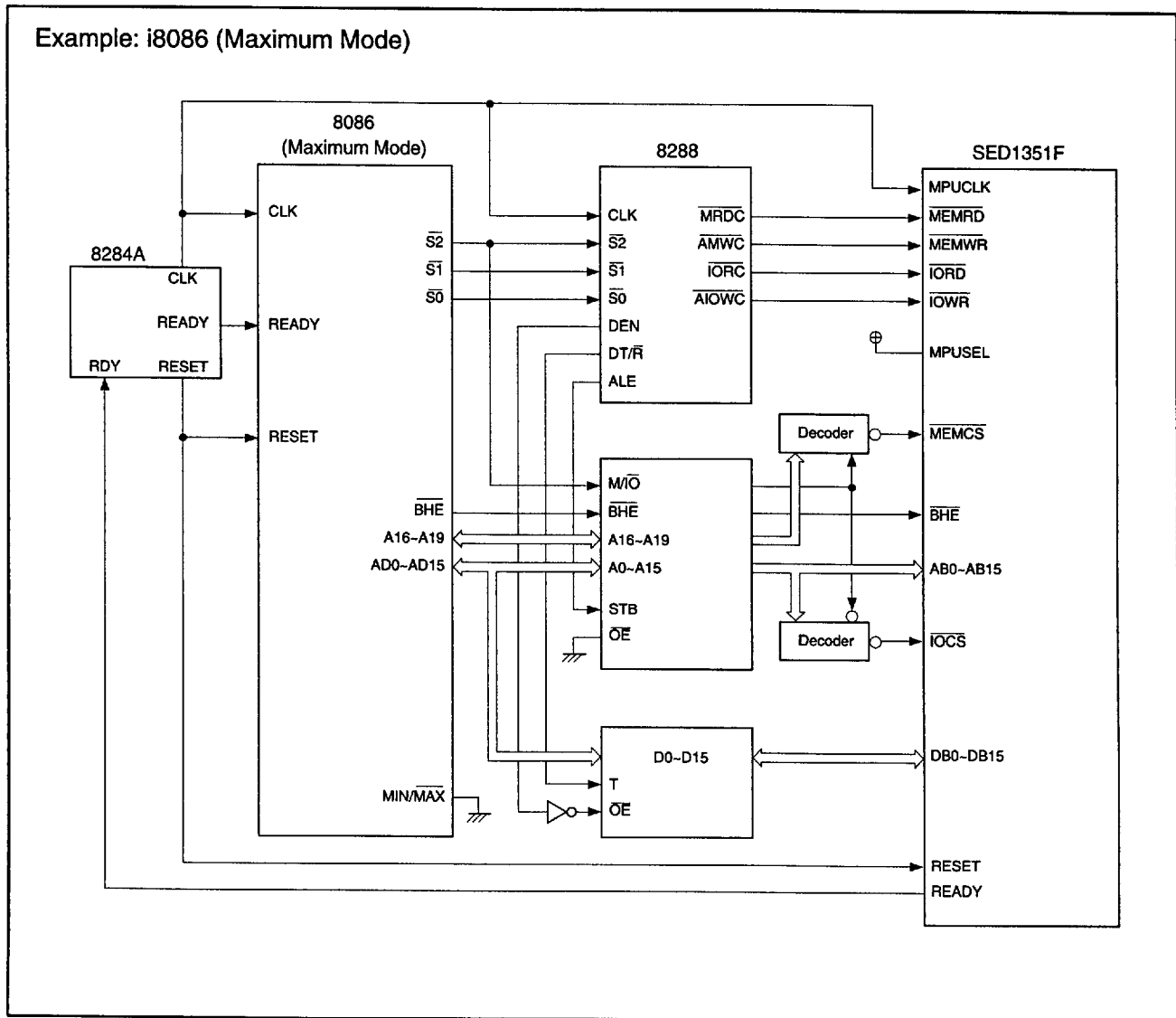


Figure 14. SED1351F/i8086 Interface

# **7.0**

## ***Video Memory Interface***

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# 7.0 VIDEO MEMORY INTERFACE

## 7.1 64 KBIT SRAM/8-BIT MPU

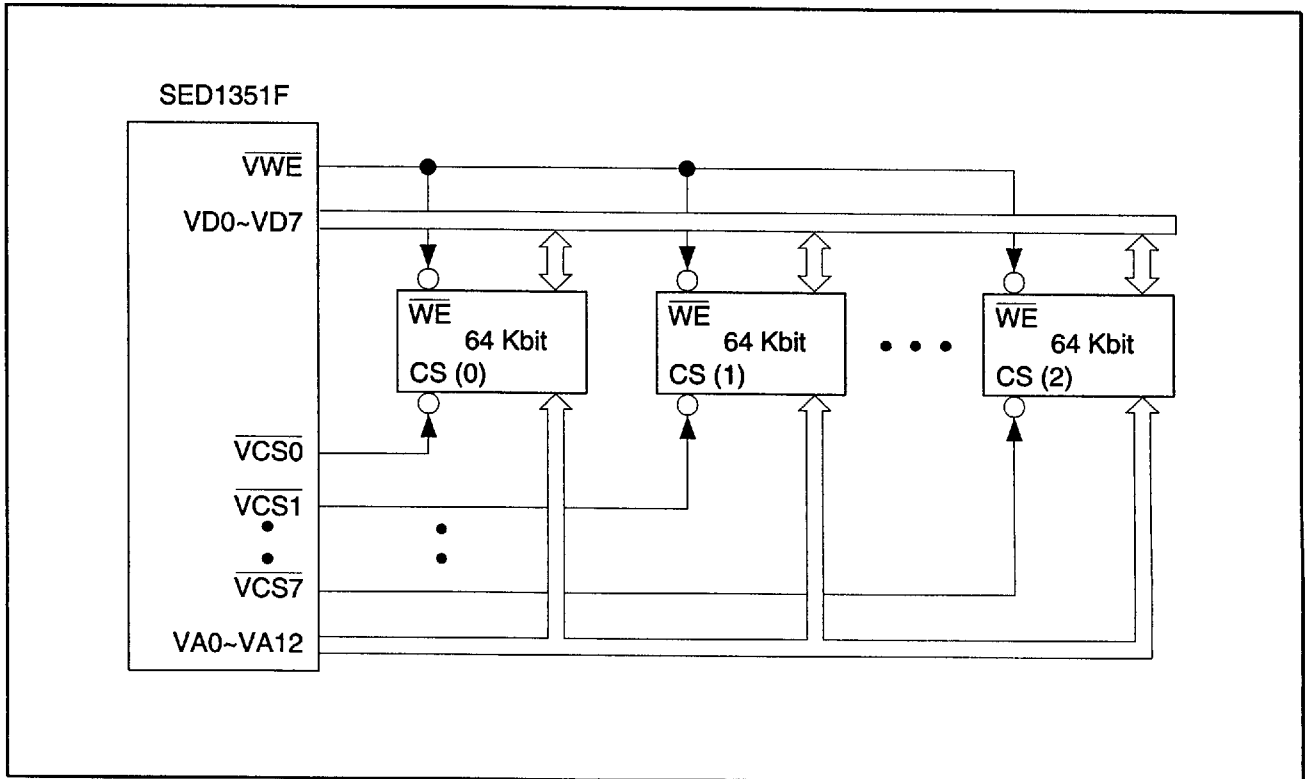


Figure 15. 8-bit MPU/64 Kbit SRAM Interface

Table 21. 8-bit MPU/64 Kbit SRAM Address Assignment

SED1351	VRAM		
	VRAM Terminals		Memory Mapping
	Address Bus	Chip Select	
VA0	A0		
VA1	A1		
VA2	A2		
VA3	A3		
VA4	A4		
VA5	A5		
VA6	A6		
VA7	A7		
VA8	A8		
VA9	A9		
VA10	A10		
VA11	A11		
VA12	A12		
VA13 / $\overline{\text{VCS7}}$		$\overline{\text{VCS7}}$	E000H to FFFFH
VA14 / $\overline{\text{VCS6}}$		$\overline{\text{VCS6}}$	C000H to DFFFH
VA15 / $\overline{\text{VCS5}}$		$\overline{\text{VCS5}}$	A000H to BFFFH
$\overline{\text{VCS4}}$		$\overline{\text{VCS4}}$	8000H to 9FFFH
$\overline{\text{VCS3}}$		$\overline{\text{VCS3}}$	6000H to 7FFFH
$\overline{\text{VCS2}}$		$\overline{\text{VCS2}}$	4000H to 5FFFH
$\overline{\text{VCS1}}$		$\overline{\text{VCS1}}$	2000H to 3FFFH
$\overline{\text{VCS0}}$		$\overline{\text{VCS0}}$	0000H to 1FFFH

7.2 256 KBIT SRAM/8-BIT MPU

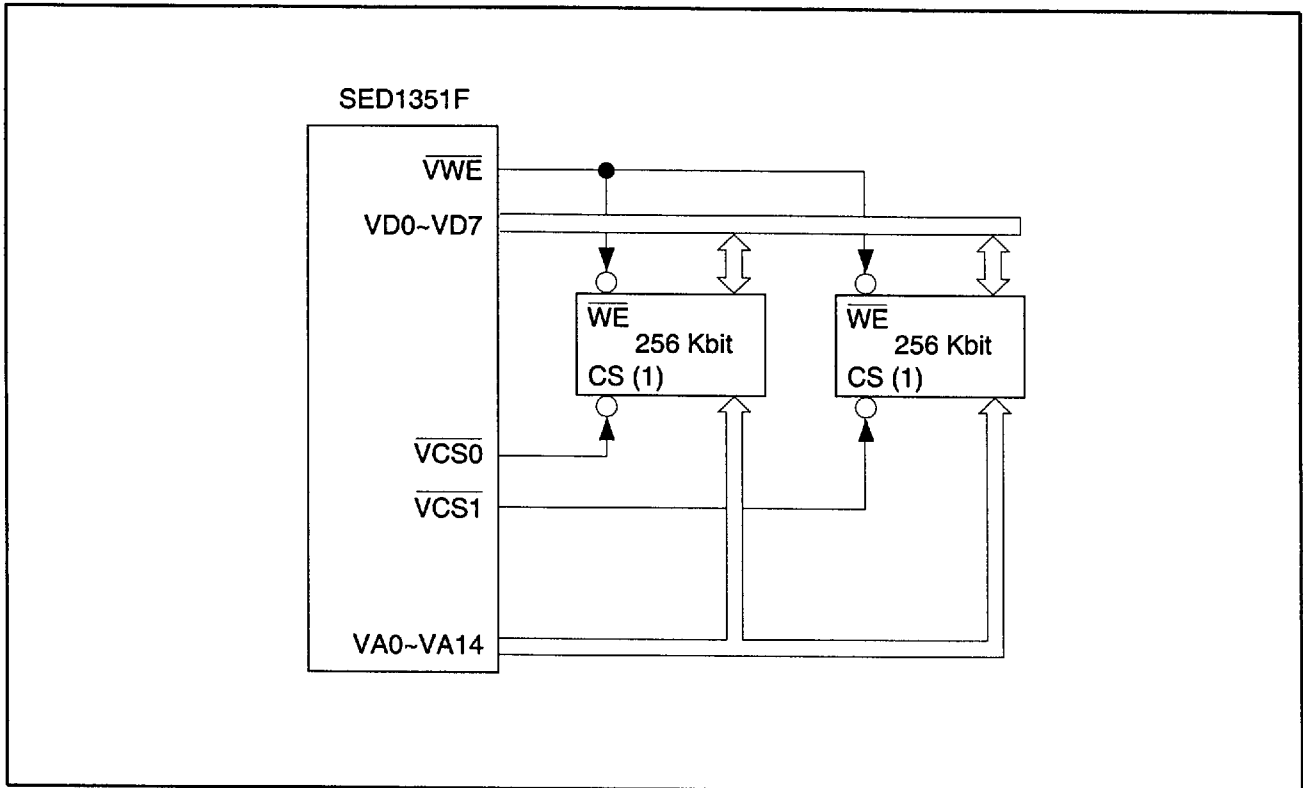


Figure 16. 8-bit MPU/256 Kbit SRAM Interface

Table 22. 8-bit MPU/256 Kbit SRAM Address Assignment

SED1351	VRAM		
	VRAM Terminals		Memory Mapping
	Address Bus	Chip Select	
VA0	A0		
VA1	A1		
VA2	A2		
VA3	A3		
VA4	A4		
VA5	A5		
VA6	A6		
VA7	A7		
VA8	A8		
VA9	A9		
VA10	A10		
VA11	A11		
VA12	A12		
VA13 / $\overline{\text{VCS7}}$	A13		
VA14 / $\overline{\text{VCS6}}$	A14		
VA15 / $\overline{\text{VCS5}}$ $\overline{\text{VCS4}}$ $\overline{\text{VCS3}}$ $\overline{\text{VCS2}}$	Not used		
$\overline{\text{VCS1}}$ $\overline{\text{VCS0}}$		$\overline{\text{VCS1}}$ $\overline{\text{VCS0}}$	8000H to FFFFH 0000H to 7FFFH

7.3 64 KBIT SRAM/16-BIT MPU

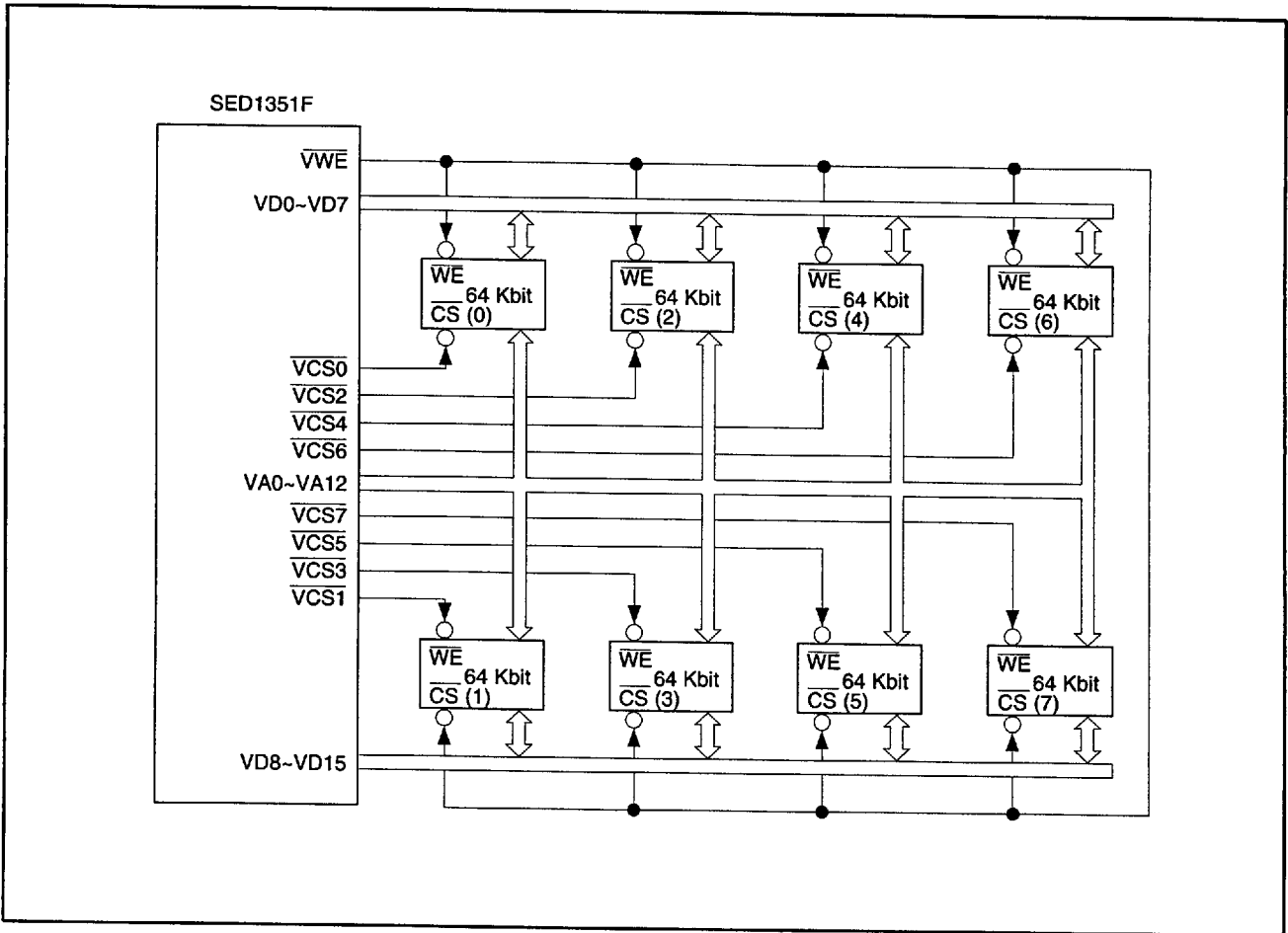


Figure 17. 16-bit MPU/64 Kbit SRAM Interface



Table 23. 16-bit MPU/64 Kbit SRAM Address Assignment

SED1351	VRAM			
	VRAM Terminals		Memory Mapping	
	Address Bus	Chip Select	Address	Odd/Even
VA0	A12			
VA1	A0			
VA2	A1			
VA3	A2			
VA4	A3			
VA5	A4			
VA6	A5			
VA7	A6			
VA8	A7			
VA9	A8			
VA10	A9			
VA11	A10			
VA12	A11			
VA13 / $\overline{\text{VCS7}}$		$\overline{\text{VCS7}}$	C000H to FFFFH	Odd address
VA14 / $\overline{\text{VCS6}}$		$\overline{\text{VCS6}}$		Even address
VA15 / $\overline{\text{VCS5}}$		$\overline{\text{VCS5}}$	8000H to BFFFH	Odd address
VA16 / $\overline{\text{VCS4}}$		$\overline{\text{VCS4}}$		Even address
$\overline{\text{VCS3}}$		$\overline{\text{VCS3}}$	4000H to 7FFFH	Odd address
$\overline{\text{VCS2}}$		$\overline{\text{VCS2}}$		Even address
$\overline{\text{VCS1}}$		$\overline{\text{VCS1}}$	0000H to 3FFFH	Odd address
$\overline{\text{VCS0}}$		$\overline{\text{VCS0}}$		Even address

7.4 256 KBIT SRAM/16-BIT MPU

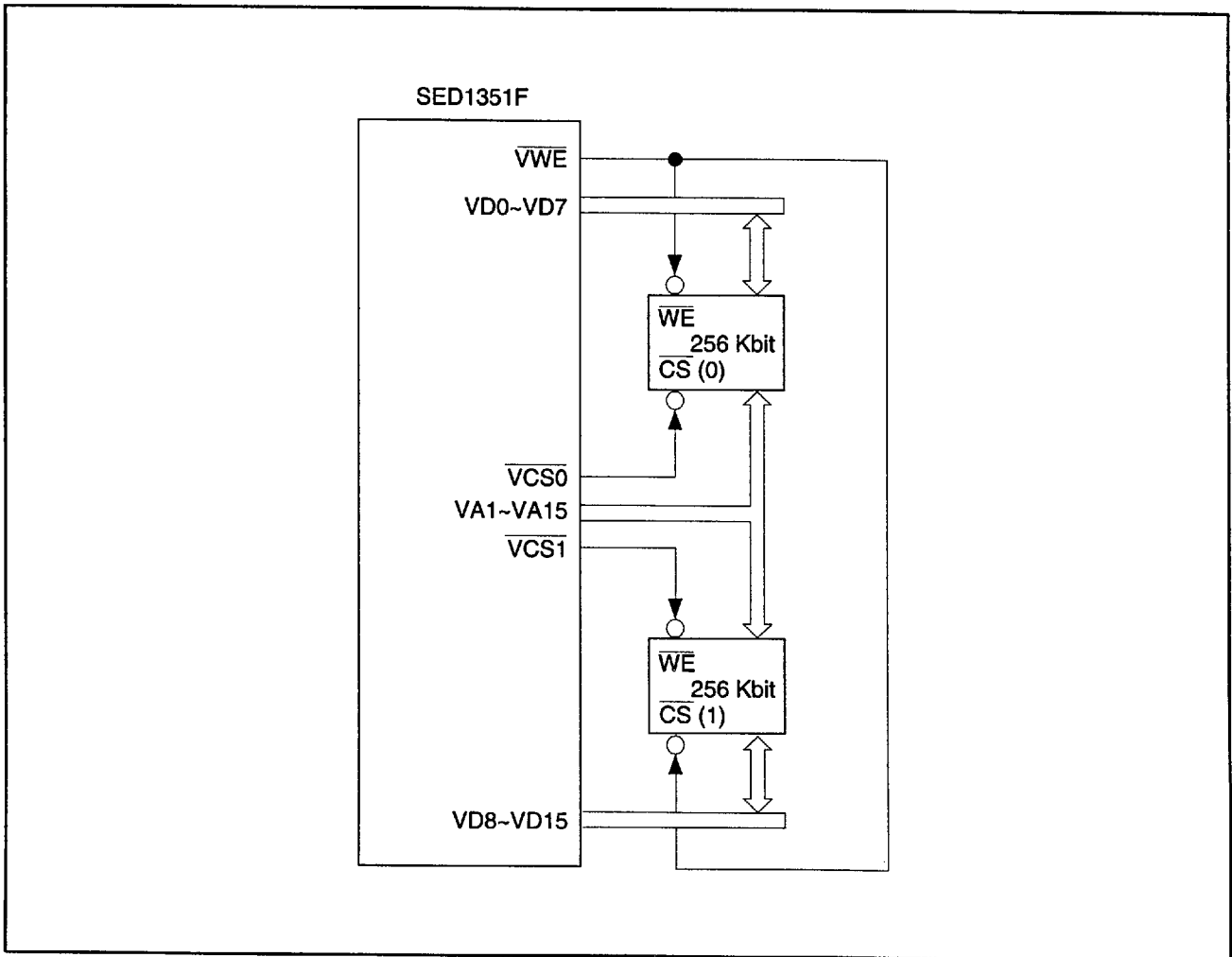


Figure 18. 16-bit MPU/256 Kbit SRAM Interface

Table 24. 16-bit MPU/256 Kbit SRAM Address Assignment

SED1351	VRAM			
	VRAM Terminals		Memory Mapping	
	Address Bus	Chip Select	Address	Odd/Even
VA0	Not used			
VA1	A0			
VA2	A1			
VA3	A2			
VA4	A3			
VA5	A4			
VA6	A5			
VA7	A6			
VA8	A7			
VA9	A8			
VA10	A9			
VA11	A10			
VA12	A11			
VA13 / $\overline{\text{VCS7}}$	A12			
VA14 / $\overline{\text{VCS6}}$	A13			
VA15 / $\overline{\text{VCS5}}$	A14			
$\overline{\text{VCS4}}$	Not used			
$\overline{\text{VCS3}}$	Not used			
$\overline{\text{VCS2}}$	Not used			
$\overline{\text{VCS1}}$		$\overline{\text{VCS1}}$	0000H to FFFFH	Odd address
$\overline{\text{VCS0}}$		$\overline{\text{VCS0}}$		Even address

# **8.0**

## ***LCD Interface***

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## 8.0 LCD INTERFACE

### 8.1 DC PROTECTION

The LCD panels will be damaged if  $V_{LCD}$  is applied to the LCD panel before  $V_{DD}$  is applied. To prevent this the LCDENB line should be connected to the enable input of the  $V_{LCD}$  control circuitry in the LCD module and the following startup procedure used.

- Set up the control register as required, with LCDE (R1:D1) set to "0".
- Set LCDE to "1" to apply  $V_{LCD}$ .

When shutting down the system, set LCDENB to "0" to switch off  $V_{LCD}$  before removing  $V_{DD}$  from the LCD panel.

### 8.2 Y-DRIVERS IN DUAL-LCD PANEL MODE

The SED1351F has a two line vertical retrace period, so when cascaded Y drivers are used to drive two LCD panels, two lines should be left disconnected between the upper and lower panel.

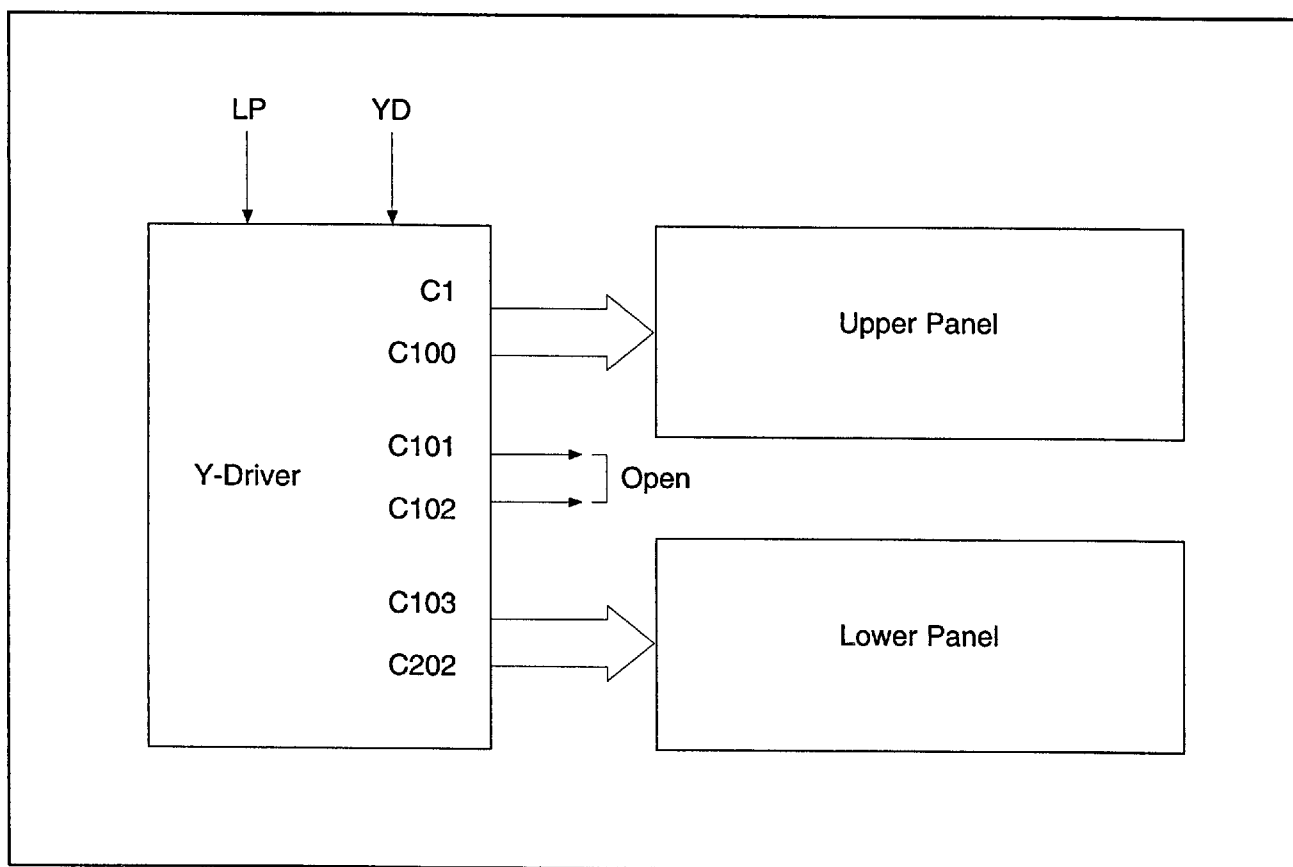
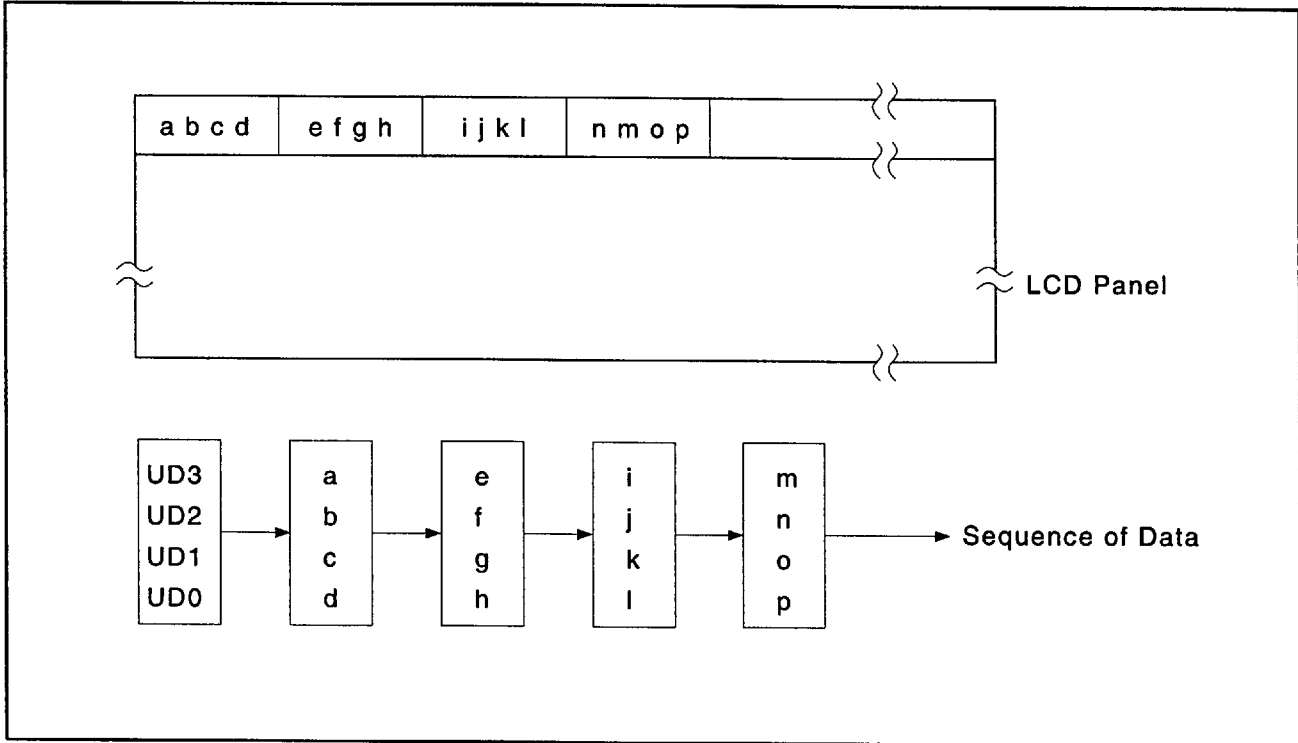


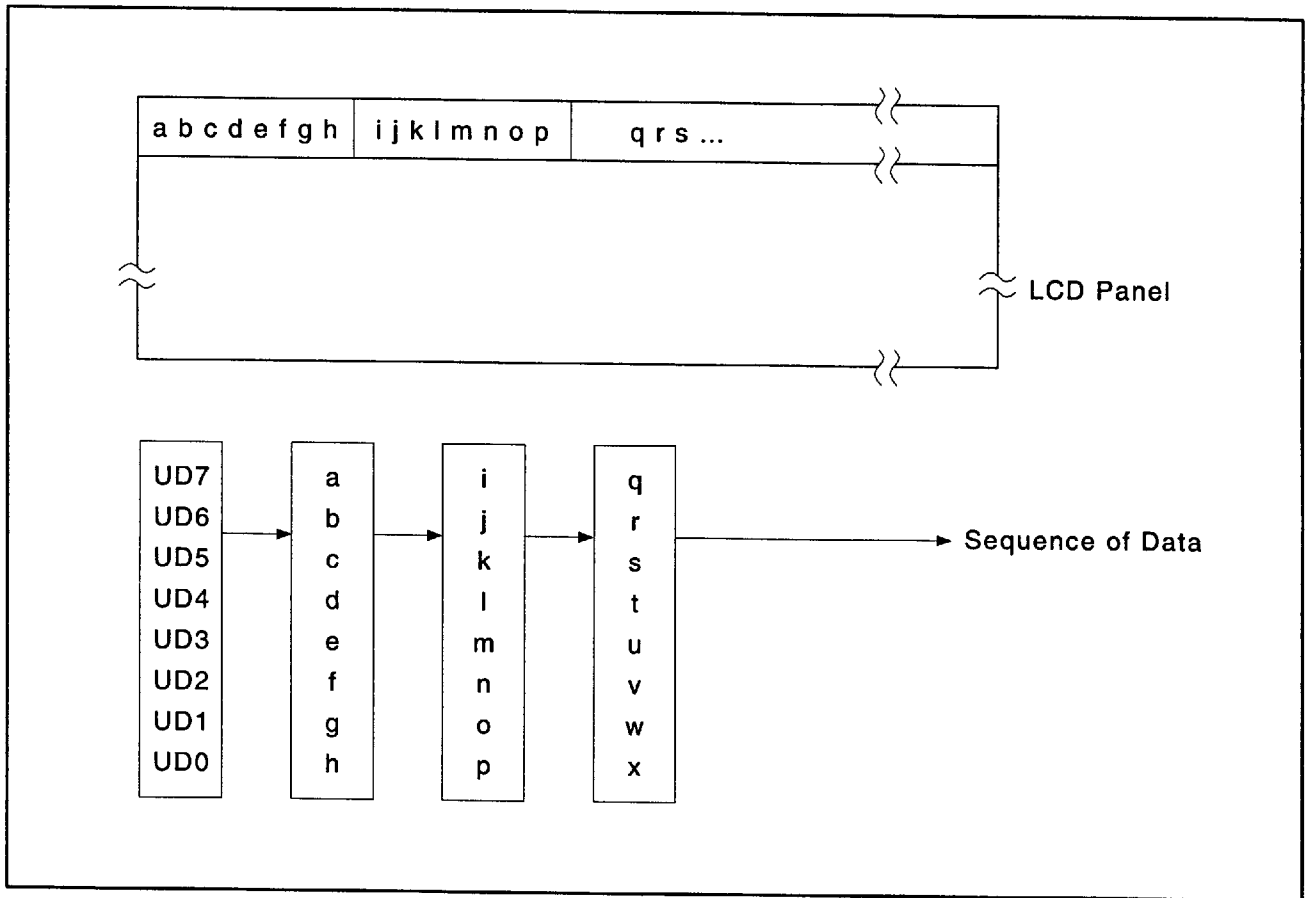
Figure 19. Cascaded Connection of Y-drivers

8.3 OUTPUT DATA FORMAT

8.3.1 Single LCD/4-bit data

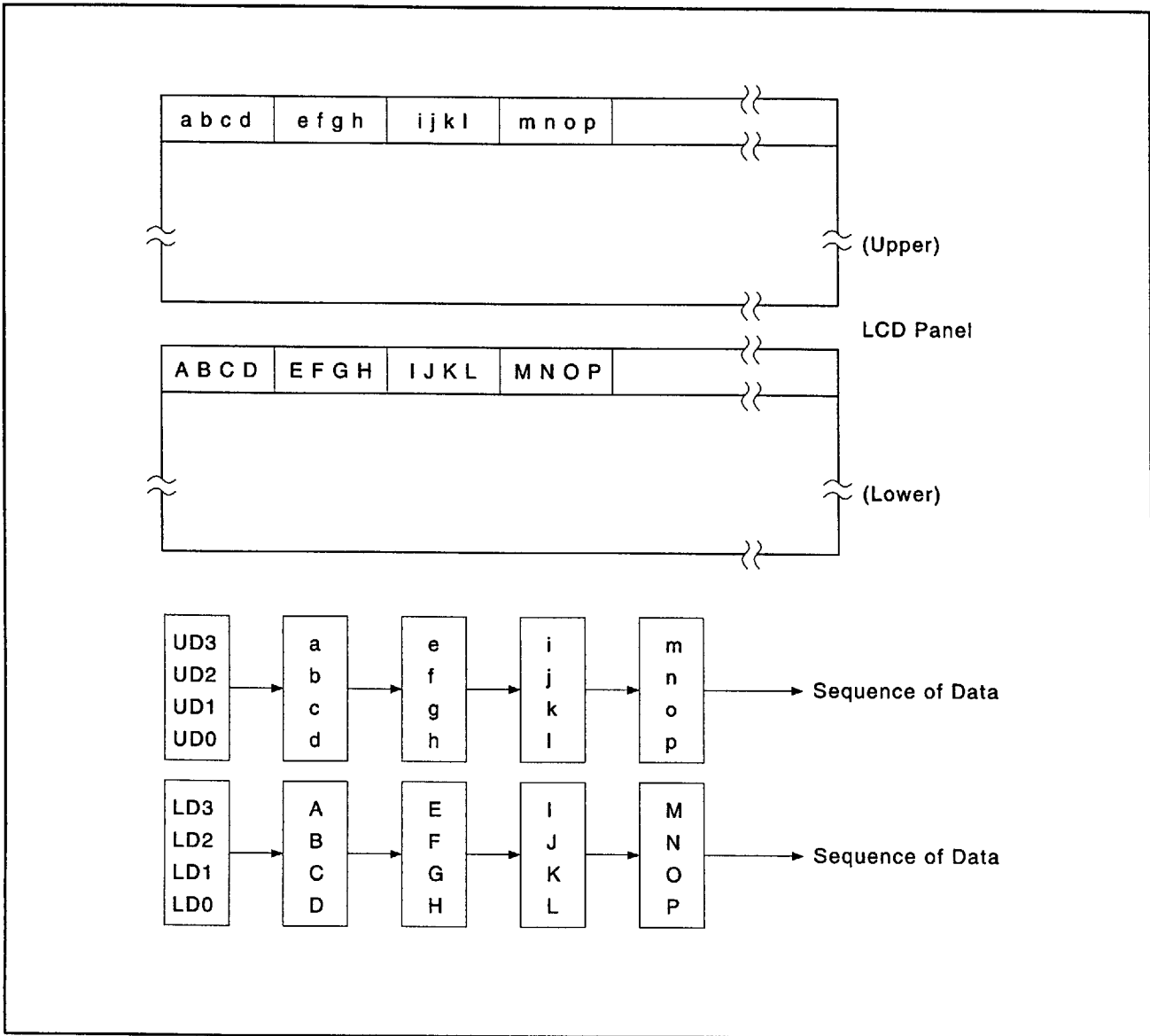


8.3.2 Single LCD/8-bit data





8.3.3 Dual LCD



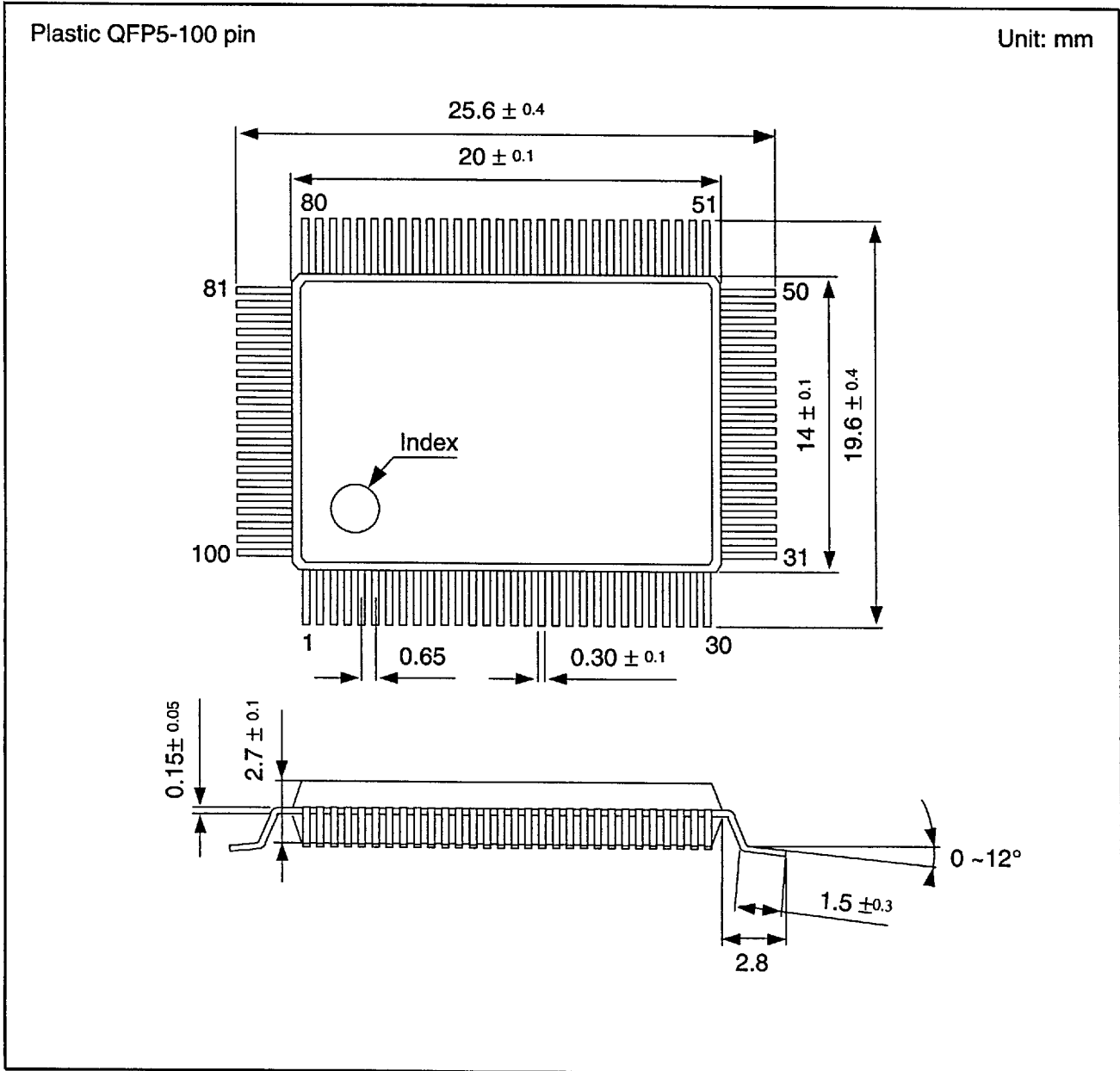
# 9.0

## *Package Dimensions*

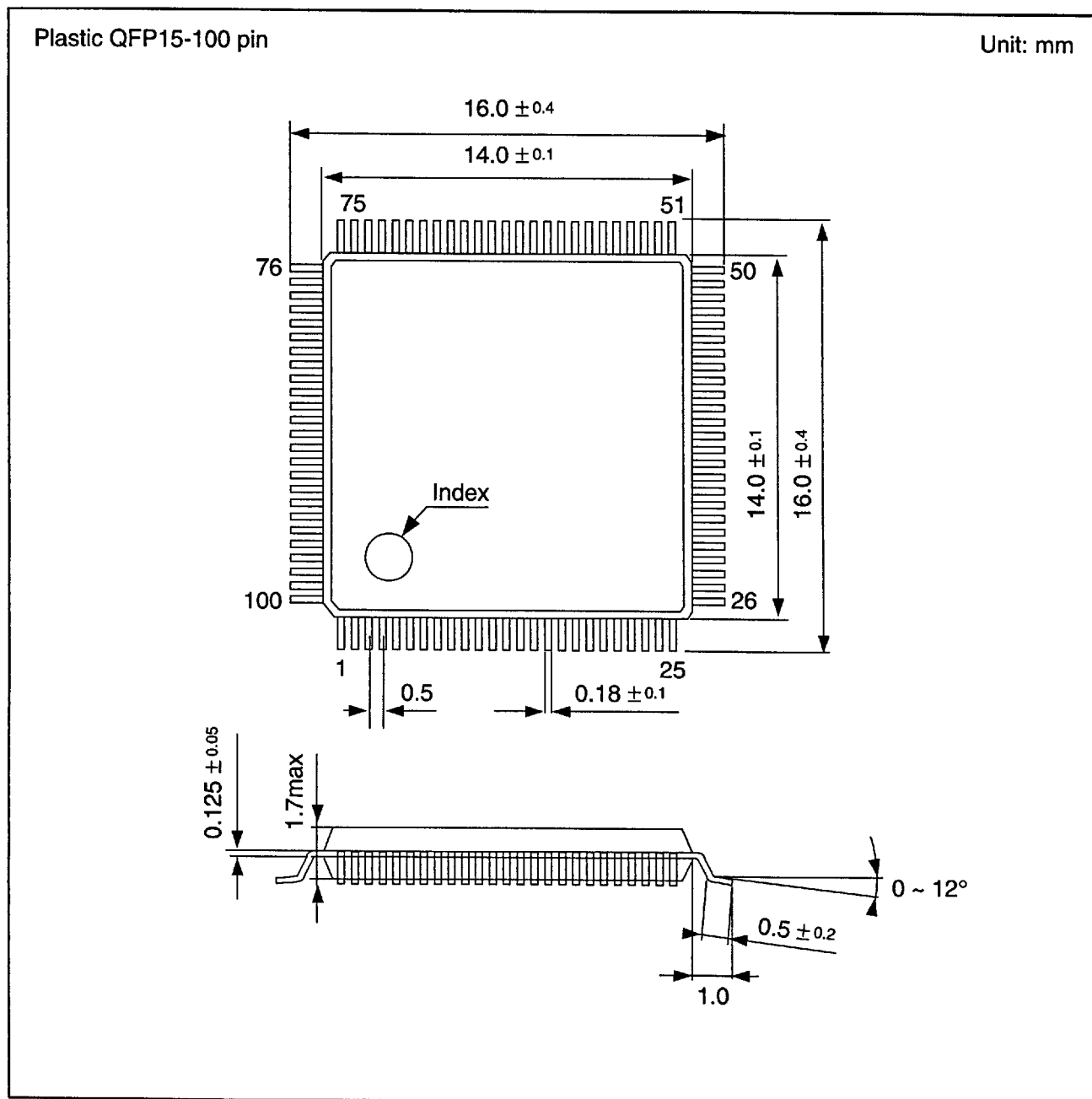
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# 9.0 PACKAGE DIMENSIONS

## 9.1 SED1351F<sub>0A</sub>



9.2 SED1351FLB



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