PWM Power Control for DC Loads

Description

The U2352B bipolar circuit is a PWM device for controlling logic level Power MOSFETs and IGBTs. It allows simple power control for DC loads. Integrated load current monitoring with adjustable switch-off threshold also gives the option of measuring the load current via the MOS transistor's on-state resistance, $R_{DS(on)}$, or via a shunt resistor.

Special Features

- Pulse width control up to 50 kHz clock frequency
- Load current monitoring via the on-state resistance, $R_{DS(on)}$, of the FET or via shunt resistor (optional)
- 100 mA push-pull output stage
- Voltage monitoring
- Temperature-compensated supply voltage limitation
- Chip temperature monitoring

Applications

- Battery-operated screwdrivers
- Battery-operated machine tools
- Halogen lamp controllers
- Dimmers
- Electronic fuses
- High-performance clock generators

Block Diagram

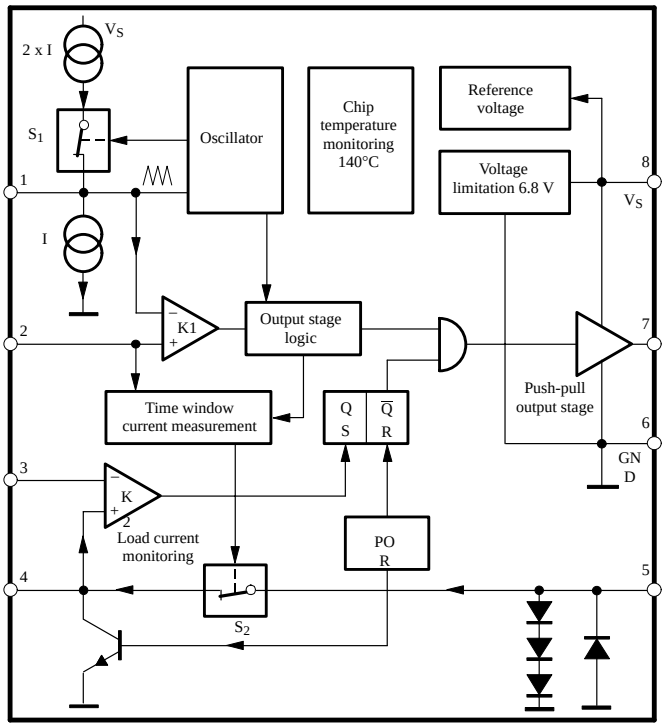


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2352B-x	DIP8	Tube
U2352B-xFP	SO8	Tube
U2352B-xFPG3	SO8	Taped and reeled

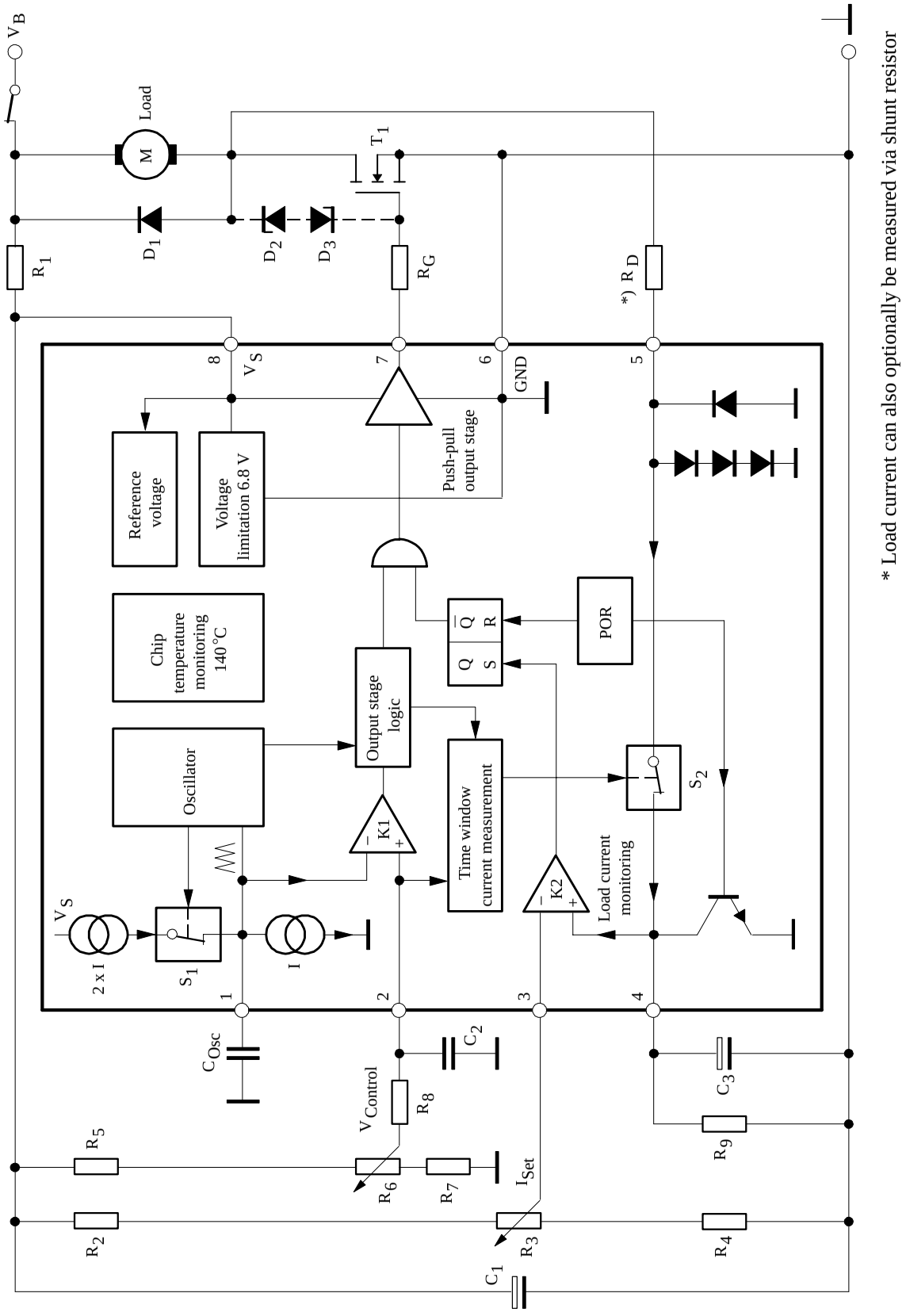


Figure 2. Block diagram with typical circuit

Pin Description

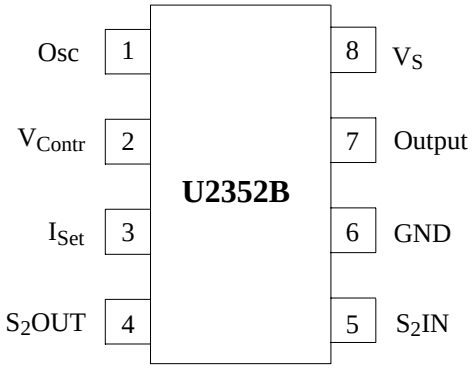


Figure 3. Pinning

Pin	Symbol	Function
1	Osc	Oscillator
2	V_{Contr}	Control voltage input
3	I_{Set}	Setpoint value current monitoring
4	S_2OUT	Output, current switch S_2
5	S_2IN	Input, current switch S_2
6	GND	Ground
7	Output	Output
8	V_S	Supply voltage

Supply, Pin 8

Internal voltage limitation in the U2352B allows a simple supply via a series resistor R_1. This enables operation of the circuit under different operating voltages. Supply voltage between Pin 8 (V_S) and Pin 6 (GND) builds up via R_1 and is smoothed by C_1.

The series resistor R_1 is calculated as follows:

$$R_{1max} = \frac{V_{Bmin} - V_{Smax}}{I_{tot}}$$

where

V_{Bmin} = Minimum operating voltage
V_{Smax} = Maximum supply voltage

I_{tot} = $I_{Smax} + I_X$
I_{Smax} = Maximum current consumption of the IS
I_X = Current consumption of the external elements

Various thresholds are derived from an internal reference voltage source.

Voltage Monitoring

During build-up and reduction of the operating voltage, uncontrolled output pulses with excessively low amplitude are suppressed by the internal monitoring circuit. All latches are reset and the output of the load current detection Pin 4 is switched to ground.

Chip Temperature Monitoring

U2352B has integrated chip temperature monitoring which switches off the output stage when a temperature of approximately 140°C is reached. The device is not enabled again until cooling has taken place and the supply voltage has been switched off and then back on again.

Pulse Width Control, Pins 1 and 2

At the frequency-determining capacitor, C_{osc}, at Pin 1, switching over of two internal current sources gives rise to a triangular voltage which comparator, K_1, compares with the control voltage at Pin 2. If the voltage, V_1, is more negative than the control voltage V_2, the output stage is switched on via the output stage logic. When C_{osc} is charged, the whole process then runs in reverse order (see figure 3).

Load Current Monitoring, Pins 3, 4, 5

Load current can be measured with the aid of an external shunt resistor, but this is only appropriate for decreased loads due to additional power loss and component size and costs. This involves the shunt voltage being fed directly to Pin 4 via a protective resistor (see figure 5).

In order to save component costs and additional power loss, the integrated load current monitoring allows the load current to be directly measured via the voltage drop at the on-state resistance, $R_{DS(on)}$, of the FET, without an additional shunt resistor. The drain voltage of the FET is supplied via an external protective resistor to Pin 5. During the off-state of the FET, a diode clamp circuit protects the detection input, Pin 5. In the on state, the load current flowing through the FET generates a corresponding voltage drop at its $R_{DS(on)}$, which is in turn converted into a current at Pin 5 by the protective resistor. This current reaches the integration element at Pin 4 via the switch S_2, which is only closed in the on-state of the FET. If the voltage at Pin 4 exceeds the setpoint value set at Pin 3, as a result of a high load current, the shutdown latch is set and the output stage is blocked. To enable the circuit again, it is necessary to switch the operating voltage off and then back on again.

Switch-off behavior is adjusted with the resistors at Pin 4 and Pin 5 and also with the capacitor at Pin 4.

A time space, Δt, must be observed between switching the output stage off and on and switching S_2 (current measurement enable switch) in order to avoid incorrect measurement and incorrect switching-off. To create this time window, the control voltage V_2 is reduced internally about ΔV_2 = approximately 300 mV and the resulting voltage, V_2*, is compared with the triangular voltage, V_1 (see figure 3).

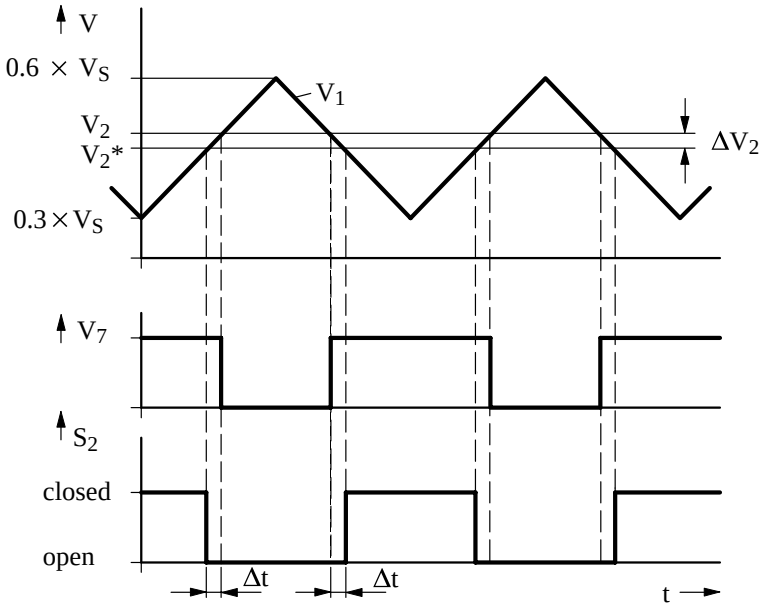


Figure 4. Signal characteristics of pulse width control with time window generation

Absolute Maximum Ratings

Reference point Pin 6, unless otherwise specified

Parameters		Symbol	Value	Unit
Power supply				
current	Pin 8	I_S	40	mA
t < 10 µs	Pin 8	i_S	400	mA
Push-pull output stage				
Output current	Pin 7	$\pm I_O$	20	mA
t < 2 ms	Pin 7	$\pm i_O$	100	mA
Input currents	Pins 4 and 5	$\pm I_I$	10	mA
	Pins 1 and 3	I_I	2	mA
Input voltages	Pins 1, 2 and 3	V_I	0 to V_8	V
Storage temperature range		T_{stg}	–40 to +125	°C
Junction temperature		T_j	+125	°C
Ambient temperature		T_{amb}	–10 to +100	°C

Thermal Resistance

Parameters		Symbol	Maximum	Unit
Junction ambient	DIP8	R_{thJA}	110	K/W
	SO8 on PC board	R_{thJA}	220	K/W
	SO8 on ceramic	R_{thJA}	140	K/W

Electrical Characteristics

V_S = 6 V, T_{amb} = 25°C, reference point Pin 6, unless otherwise specified

Parameters	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
Supply voltage limitation	I_S = 5 mA I_S = 20 mA	Pin 8	V_S V_S	6.4 6.5	6.8 6.9	7.2 7.3	V V
Current consumption	V_S = 6 V	Pin 8	I_S		2.7	3.5	mA
Voltage monitoring							
Switch-on threshold Switch-off threshold		Pin 8 Pin 8	V_{SON} V_{SOFF}	5.2 4.7	5.6 5.1	6.0 5.5	V V
Oscillator $f_{OSC}\ [kHz] \approx \frac{55}{C_{OSC}\ [nF] \times V_S\ [V]}$		Pin 1					
Upper threshold ($0.6 \times V_S$) Lower threshold ($0.3 \times V_S$) Charge current Discharge current			V_{Tu} V_{Tl} $-I_{ch}$ I_{dis}	3.4 1.7 26 26	3.6 1.8 33 33	3.8 1.9 40 40	V V µA µA
Control voltage input							
Input voltage range Input current, Offset voltage K_1 Window, current measurement	 0 V ≤ V_2 ≤ V_8 	Pin 2 Pin 2 Pin 2–1 Pin 2–1	V_I $\pm I_i$ $\pm V_{Offs}$ $-\Delta V_2$	0 260	 300	V_8 500 15 340	V nA mV mV
Load current monitoring							
Setpoint value input: Input voltage range Input current	 0 V ≤ V_3 ≤ 6 V	 Pin 3 Pin 3	 V_I $\pm I_i$	 0 	 	 6 500	 V nA
Offset voltage K_2		Pin 4–3	$\pm V_{Offs}$			15	mV
Load current detection: Voltage limitation Voltage limitation	 I_5 = 1 mA I_5 = –1 mA	 Pin 5 Pin 5	 V_L $-V_L$	 	 2.3 0.7	 	 V V
Discharge current at POR		Pin 4	I_{dis}	1			mA
Switch S_2		Pin 5–4					
Residual voltage at closed switch V_4 = 0 V, I_5 = 50 µA V_4 = 0.1 V, I_5 = 50 µA V_4 = 0.3 V, I_5 = 50 µA V_4 = 0.3 V, I_5 = 100 µA			 V_{Sat} V_{Sat} V_{Sat} V_{Sat}		 175 150 125 200		 mV mV mV mV
Push-pull output stage		Pin 7					
Upper saturation voltage	I_7 = –2 mA	Pin 7–8	$-V_{Satu}$			1	V
Lower saturation voltage	I_7 = 10 mA	Pin 7	V_{Satl}			0.3	V
Output current ON state OFF state	 t ≤ 2 µs t ≤ 2 µs		 $-i_o$ i_o	 100 100	 	 	 mA mA

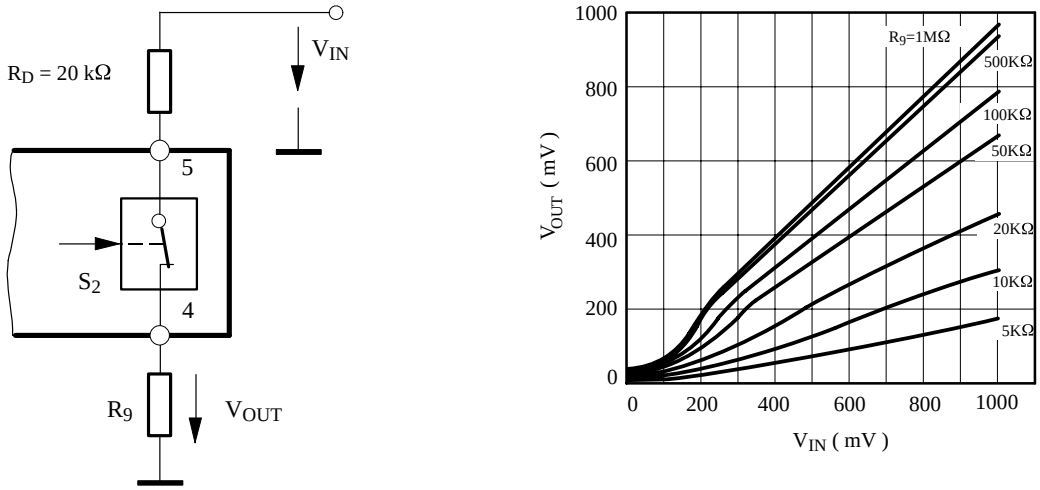


Figure 5. Typical circuitry of the current switch S_2 with associated transfer characteristics (S_2 closed)

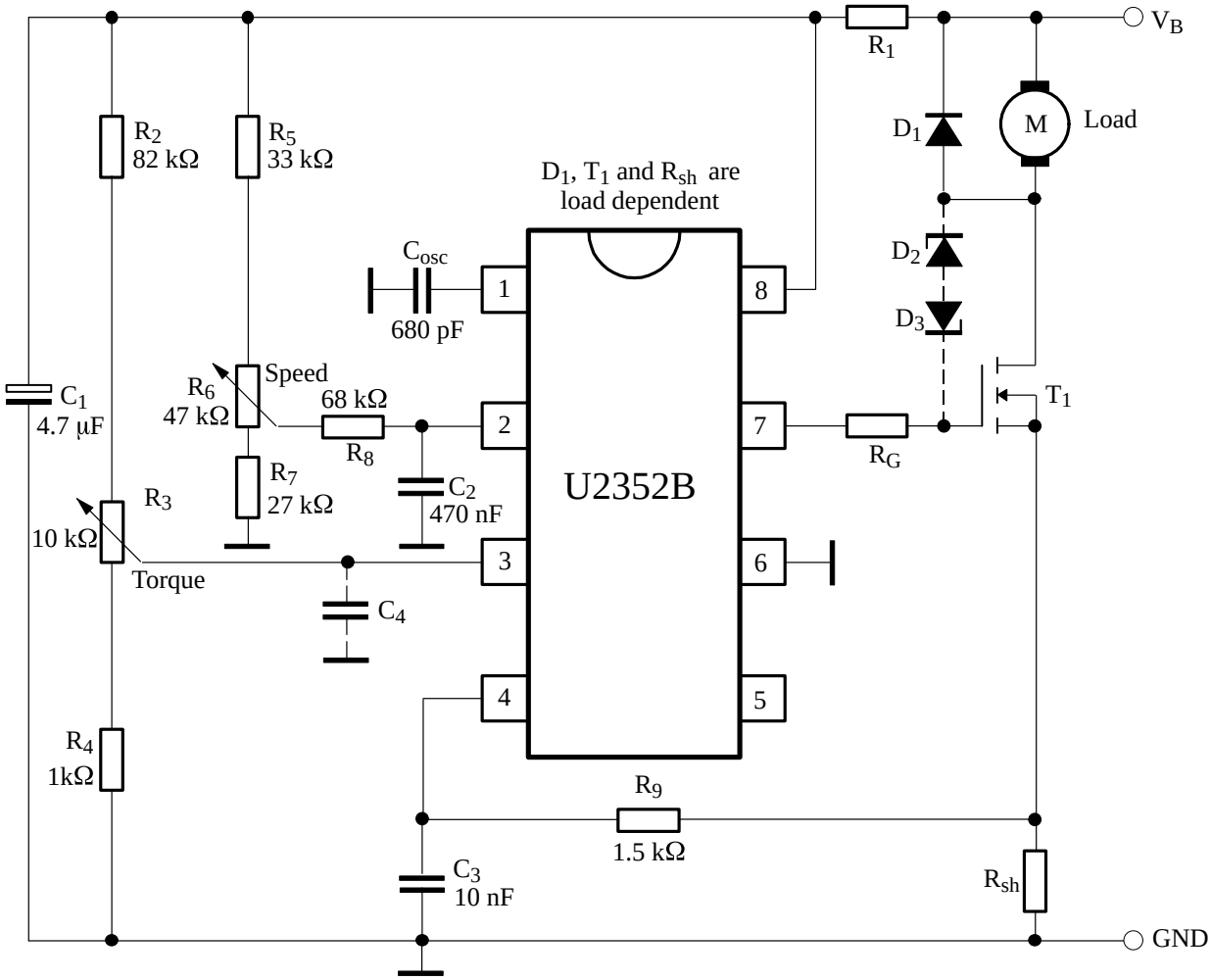
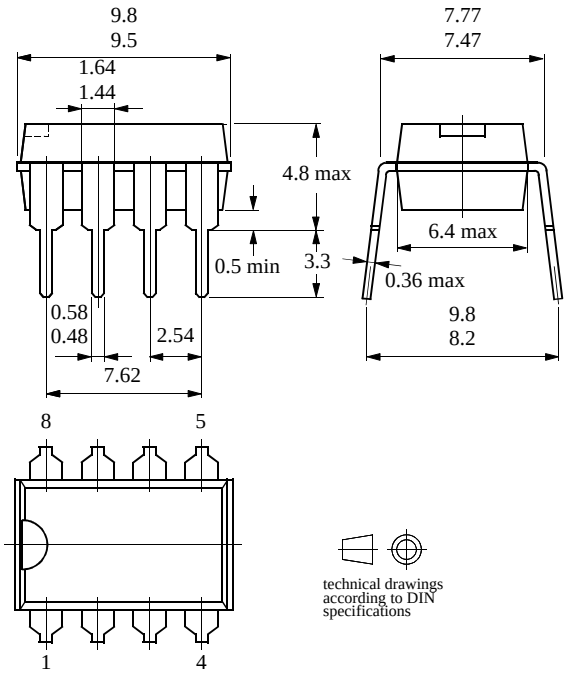


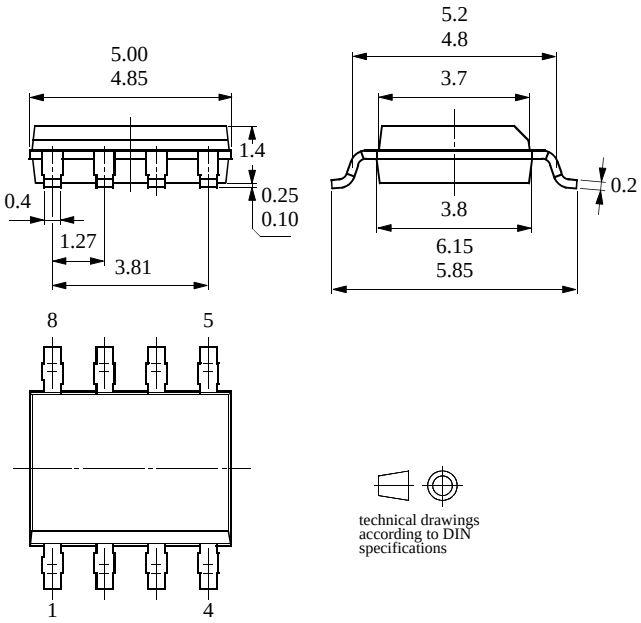
Figure 6. Speed control with load current monitoring (load current detection via shunt resistor)

Package Information

Package DIP8
Dimensions in mm



Package SO8
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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