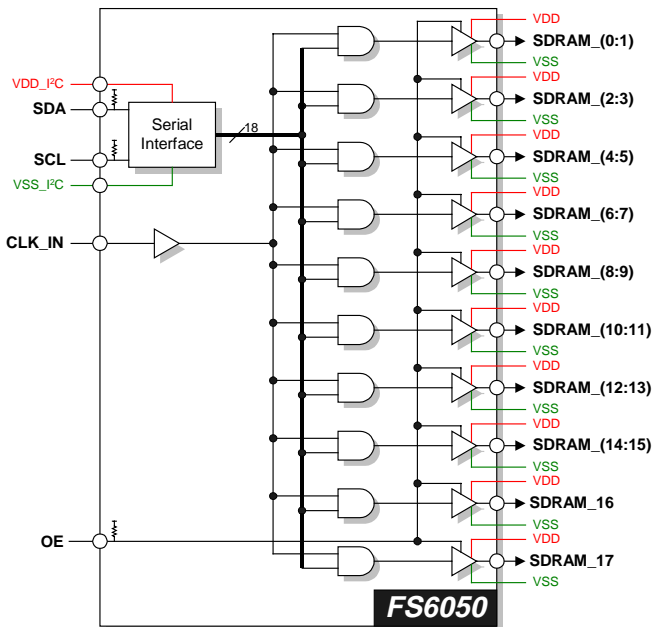


April 1999

1.0 Features

- Generates up to eighteen low-skew, non-inverting clocks from one clock input
- Supports up to four SDRAM DIMMs
- Uses either I²C™-bus or SMBus serial interface with Read and Write capability for individual clock output control
- Output enable pin tristates all clock outputs to facilitate board testing
- Clock outputs skew-matched to less than 250ps
- Less than 5ns propagation delay
- Output impedance: 17Ω at 0.5V_{DD}
- Serial interface I/O meet I²C specifications; all other I/O are LVTTTL/LVCMOS-compatible
- Five different pin configurations available:
 - FS6050: 18 clock outputs in a 48-pin SSOP
 - FS6051: 10 clock outputs in a 28-pin SOIC, SSOP
 - FS6053: 13 clock outputs in a 28-pin SOIC
 - FS6054: 14 clock outputs in a 28-pin SOIC

Figure 1: Block Diagram (FS6050)



2.0 Description

The FS6050 family of CMOS clock fanout buffer ICs are designed for high-speed motherboard applications, such as Intel Pentium® II PC100-based systems with 100MHz SDRAM.

Up to eighteen buffered, non-inverting clock outputs are fanned-out from one clock input. Individual clocks are skew matched to less than 250ps at 100MHz. Multiple power and ground supplies reduce the effects of supply noise on device performance.

Under I²C-bus control, individual clock outputs may be turned on or off. An active-low output enable is available to force all the clock outputs to a tristate level for system testing.

Figure 2: Pin Configuration (FS6050)

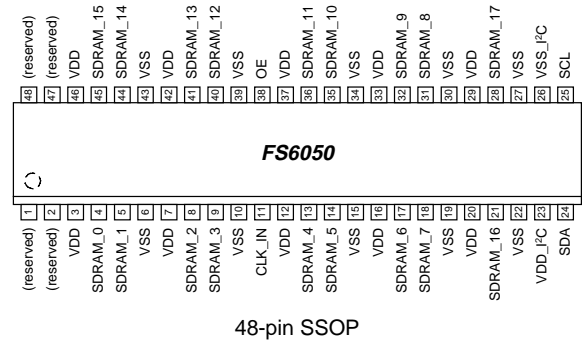
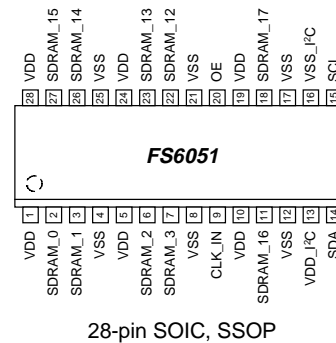


Figure 3: Pin Configuration (FS6051)



Additional pin configurations are noted on Page 2.

FS6050/FS6051/FS6053/FS6054

Low-Skew Clock Fanout Buffer ICs



April 1999

Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI^D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

| PIN (FS6050) | PIN (FS6051) | PIN (FS6053) | PIN (FS6054) | TYPE | NAME | DESCRIPTION |
|---------------------------------------|----------------------|------------------|--------------|-------------------|----------------------|--|
| 11 | 9 | 9 | 9 | DI | CLK_IN | Clock input for SDRAM clock outputs |
| 25 | 15 | 15 | 15 | DI ^U | SCL | Serial clock input |
| 24 | 14 | 14 | 14 | DI ^U O | SDA | Serial data input/output |
| 4 | 2 | 2 | 2 | DO | SDRAM_0 | SDRAM clock outputs (Byte 0) |
| 5 | 3 | 3 | 3 | DO | SDRAM_1 | |
| 8 | 6 | 6 | 6 | DO | SDRAM_2 | |
| 9 | 7 | 7 | 7 | DO | SDRAM_3 | |
| 13 | - | - | - | DO | SDRAM_4 | |
| 14 | - | - | - | DO | SDRAM_5 | |
| 17 | - | 10 | 10 | DO | SDRAM_6 | |
| 18 | - | 11 | 11 | DO | SDRAM_7 | |
| 31 | - | 18 | 18 | DO | SDRAM_8 | SDRAM clock outputs (Byte 1) |
| 32 | - | 19 | 19 | DO | SDRAM_9 | |
| 35 | - | - | - | DO | SDRAM_10 | |
| 36 | - | - | - | DO | SDRAM_11 | |
| 40 | 22 | 22 | 22 | DO | SDRAM_12 | |
| 41 | 23 | 23 | 23 | DO | SDRAM_13 | |
| 44 | 26 | 26 | 26 | DO | SDRAM_14 | SDRAM feedback clock outputs (Byte 2) |
| 45 | 27 | 27 | 27 | DO | SDRAM_15 | |
| 21 | 11 | 12 | 12 | DO | SDRAM_16 | |
| 28 | 18 | - | 17 | DO | SDRAM_17 | |
| 38 | 20 | - | 20 | DI ^U | OE | Output enable tristates all clock outputs when low |
| 3, 7, 12, 16, 20, 29, 33, 37, 42, 46 | 1, 5, 10, 19, 24, 28 | 1, 5, 20, 24, 28 | 1, 5, 24, 28 | P | VDD | 3.3V ± 5% power supply for SDRAM clock buffers |
| 23 | 13 | 13 | 13 | P | VDD_I ² C | 3.3V ± 5% power supply for serial communications |
| 6, 10, 15, 19, 22, 27, 30, 34, 39, 43 | 4, 8, 12, 17, 21, 25 | 4, 8, 17, 21, 25 | 4, 8, 21, 25 | P | VSS | Ground for SDRAM clock buffers |
| 26 | 16 | 16 | 16 | P | VSS_I ² C | Ground for serial communications |
| 1, 2, 47, 48 | - | - | - | - | (reserved) | Reserved |

Figure 4: Pin Configuration (FS6053)

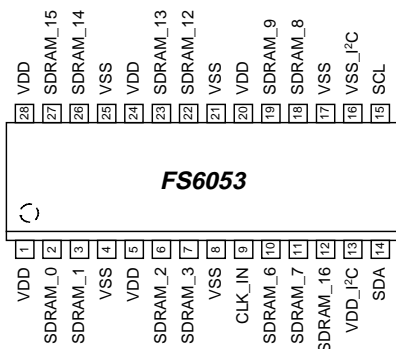
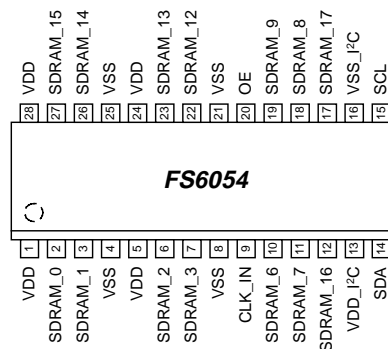


Figure 5: Pin Configuration (FS6054)



April 1999

3.0 Programming Information

Table 2: Clock Enable

| CONTROL INPUTS | CLOCK OUTPUTS (MHz) |
|----------------|---------------------|
| OE | SDRAM_0:17 |
| 0 | tristate |
| 1 | CLK_IN |

3.1 Power-Up Initialization

All outputs are enabled and active upon power-up, and all output control register bits are initialized to one.

The outputs must be configured at power-up and are not expected to be configured during normal operation. Inactive outputs are held low and are disabled from switching.

3.1.1 Unused Outputs

Outputs that are not used in versions of this device with a reduced pinout are still operational internally. To reduce power dissipation and crosstalk effects from the unloaded outputs, it is recommended that these outputs be shut off via the Control Registers.

3.2 Register Programming

A logic-one written to a valid bit location turns on the assigned output clock. Likewise, a logic-zero written to a valid bit location turns off the assigned output clock.

Any unused or reserved register bits should be cleared to zero.

Serial bits are written to this device in the order shown in Table 3.

Table 3: Register Summary

| SERIAL BIT | DATA BYTE | CLOCK OUTPUT |
|------------|---|--------------|
| 0 | (MSB) | SDRAM_7 |
| 1 | Byte 0 SDRAM Control Register 0 | SDRAM_6 |
| 2 | | SDRAM_5 |
| 3 | | SDRAM_4 |
| 4 | | SDRAM_3 |
| 5 | | SDRAM_2 |
| 6 | | SDRAM_1 |
| 7 | (LSB) | SDRAM_0 |
| 8 | (MSB) | SDRAM_15 |
| 9 | Byte 1 SDRAM Control Register 1 | SDRAM_14 |
| 10 | | SDRAM_13 |
| 11 | | SDRAM_12 |
| 12 | | SDRAM_11 |
| 13 | | SDRAM_10 |
| 14 | | SDRAM_9 |
| 15 | (LSB) | SDRAM_8 |
| 16 | (MSB) | SDRAM_17 |
| 17 | Byte 2 SDRAM Control Register 2 | SDRAM_16 |
| 18 | | Reserved |
| 19 | | Reserved |
| 20 | | Reserved |
| 21 | | Reserved |
| 22 | | Reserved |
| 23 | (LSB) | Reserved |

FS6050/FS6051/FS6053/FS6054

Low-Skew Clock Fanout Buffer ICs



April 1999

Table 4: Byte 0 - SDRAM Control Register 0

| REGISTER BIT | CLOCK OUTPUT | DESCRIPTION | OUTPUT PIN (FS6050) | OUTPUT PIN (FS6051) | OUTPUT PIN (FS6053) | OUTPUT PIN (FS6054) |
|--------------|--------------|------------------|---------------------|---------------------|---------------------|---------------------|
| 7 | SDRAM_7 | On (1) / Off (0) | Pin 18 | - | Pin 11 | Pin 11 |
| 6 | SDRAM_6 | On (1) / Off (0) | Pin 17 | - | Pin 10 | Pin 10 |
| 5 | SDRAM_5 | On (1) / Off (0) | Pin 14 | - | - | - |
| 4 | SDRAM_4 | On (1) / Off (0) | Pin 13 | - | - | - |
| 3 | SDRAM_3 | On (1) / Off (0) | Pin 9 | Pin 7 | Pin 7 | Pin 7 |
| 2 | SDRAM_2 | On (1) / Off (0) | Pin 8 | Pin 6 | Pin 6 | Pin 6 |
| 1 | SDRAM_1 | On (1) / Off (0) | Pin 5 | Pin 3 | Pin 3 | Pin 3 |
| 0 | SDRAM_0 | On (1) / Off (0) | Pin 4 | Pin 2 | Pin 2 | Pin 2 |

Table 5: Byte 1 - SDRAM Control Register 1

| REGISTER BIT | CLOCK OUTPUT | DESCRIPTION | OUTPUT PIN (FS6050) | OUTPUT PIN (FS6051) | OUTPUT PIN (FS6053) | OUTPUT PIN (FS6054) |
|--------------|--------------|------------------|---------------------|---------------------|---------------------|---------------------|
| 15 | SDRAM_15 | On (1) / Off (0) | Pin 45 | Pin 27 | Pin 27 | Pin 27 |
| 14 | SDRAM_14 | On (1) / Off (0) | Pin 44 | Pin 26 | Pin 26 | Pin 26 |
| 13 | SDRAM_13 | On (1) / Off (0) | Pin 41 | Pin 23 | Pin 23 | Pin 23 |
| 12 | SDRAM_12 | On (1) / Off (0) | Pin 40 | Pin 22 | Pin 22 | Pin 22 |
| 11 | SDRAM_11 | On (1) / Off (0) | Pin 36 | - | - | - |
| 10 | SDRAM_10 | On (1) / Off (0) | Pin 35 | - | - | - |
| 9 | SDRAM_9 | On (1) / Off (0) | Pin 32 | - | Pin 19 | Pin 19 |
| 8 | SDRAM_8 | On (1) / Off (0) | Pin 31 | - | Pin 18 | Pin 18 |

Table 6: Byte 2 - SDRAM Control Register 2

| REGISTER BIT | CLOCK OUTPUT | DESCRIPTION | OUTPUT PIN (FS6050) | OUTPUT PIN (FS6051) | OUTPUT PIN (FS6053) | OUTPUT PIN (FS6054) |
|--------------|--------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 23 | SDRAM_17 | On (1) / Off (0) | Pin 28 | Pin 18 | - | Pin 17 |
| 22 | SDRAM_16 | On (1) / Off (0) | Pin 21 | Pin 11 | Pin 12 | Pin 12 |
| 21 | | Reserved (set to 0) | - | - | - | - |
| 20 | | Reserved (set to 0) | - | - | - | - |
| 19 | | Reserved (set to 0) | - | - | - | - |
| 18 | | Reserved (set to 0) | - | - | - | - |
| 17 | | Reserved (set to 0) | - | - | - | - |
| 16 | | Reserved (set to 0) | - | - | - | - |

April 1999

4.0 Dual Serial Interface Control

This integrated circuit is a read/write slave device that supports both the Inter IC Bus (I²C-bus) and the System Management Bus (SMBus) two-wire serial interface protocols. The unique device address that is written to the device determines whether the part expects to receive SMBus commands or I²C commands. Since SMBus is derived from the I²C-bus, the protocol for both bus types is very similar.

In general, the bus has to be controlled by a master device that generates the serial clock SCL, controls bus access, and generates the START and STOP conditions while the device works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated. A device that sends data onto the bus is defined as the transmitter, and a device receiving data as the receiver.

Bus logic levels and timing parameters noted herein follow I²C-bus convention. Logic levels are based on a percentage of VDD. A logic-one corresponds to a nominal voltage of VDD, while a logic-zero corresponds to ground (VSS).

4.1 Bus Conditions

Data transfer on the bus can only be initiated when the bus is not busy. During the data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is high. Changes in the data line when the clock line is high is interpreted by the device as a START or STOP condition. Both I²C-bus and SMBus protocols define the following conditions on the bus. Refer to Figure 12: Bus Timing Data for more information.

4.1.1 Not Busy

Both the data (SDA) and clock (SCL) lines remain high to indicate the bus is not busy.

4.1.2 START Data Transfer

A high to low transition of the SDA line while the SCL input is high indicates a START condition. All commands to the device must be preceded by a START condition.

4.1.3 STOP Data Transfer

A low to high transition of the SDA line while SCL is held high indicates a STOP condition. All commands to the device must be followed by a STOP condition.

4.1.4 Data Valid

The state of the SDA line represents valid data if the SDA line is stable for the duration of the high period of the SCL line after a START condition occurs. The data on the SDA line must be changed only during the low period of the SCL signal. There is one clock pulse per data bit.

Each data transfer is initiated by a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is determined by the master device, and can continue indefinitely. However, data that is overwritten to the device after the data registers are filled will overflow from the last register into the first register, then the second, and so on, in a first-in, first-overwritten fashion.

4.1.5 Acknowledge

When addressed, the receiving device is required to generate an Acknowledge after each byte is received. The master device must generate an extra clock pulse to coincide with the Acknowledge bit. The acknowledging device must pull the SDA line low during the high period of the master acknowledge clock pulse. Setup and hold times must be taken into account.

The master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been read (clocked) out of the slave. In this case, the slave must leave the SDA line high to allow the master to generate a STOP condition.

4.2 Bus Operation and Commands

All programmable registers can be accessed via the bi-directional two wire digital interface. The device accepts the Random Register Read/Write and the Sequential Register Read/Write I²C commands. The device also supports the Block Read/Write SMBus commands.

4.2.1 I²C-bus and SMBus Device Addressing

After generating a START condition, the bus master broadcasts a seven-bit device address followed by a R/W bit. Note that every device on an I²C-bus or SMBus must have a unique address to avoid bus conflicts.

For an SMBus interface, the address of the device is:

| A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |

For an I²C-bus interface, the device can support two device addresses to permit multiple devices on one I²C-bus. The A2 address bit is ignored and can be set to either a one or a zero.

Therefore, for an I²C-bus interface the device address is:

| A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|----|----|----|----|----|----|----|
| 1 | 0 | 1 | 1 | X | 0 | 0 |

4.2.2 I²C-bus: Random Register Write Procedure



Random write operations, as shown in Figure 6, allow the master to directly write to any register. To initiate a write procedure, the R/W bit that is transmitted after the seven-bit I²C device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write eight bits of data into the addressed register. A final acknowledge is returned by the device, and the master generates a STOP condition.

If either a STOP or a repeated START condition occurs during a Register Write, the data that has been transferred is ignored.

4.2.3 I²C-bus: Random Register Read Procedure

Random read operations allow the master to directly read from any register. To perform a read procedure, as shown in Figure 7, the R/W bit that is transmitted after the seven-bit I²C address is a logic-low, as in the Register Write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits the eight-bit word. The master does not acknowledge the transfer but does generate a STOP condition.

4.2.4 I²C-bus: Sequential Register Write Procedure

Sequential write operations, as shown in Figure 8, allow the master to write to each register in order. The register pointer is automatically incremented after each write. This procedure is more efficient than the Random Register Write if several registers must be written.

To initiate a write procedure, the R/W bit that is transmitted after the seven-bit I²C device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write data up to the last addressed register before the register address pointer overflows back to the beginning address. An acknowledge by the device between each byte of data must occur before the next data byte is sent.

Registers are updated every time the device sends an acknowledge to the host. The register update does not wait for the STOP condition to occur. Registers are therefore updated at different times during a Sequential Register Write.

4.2.5 I²C-bus: Sequential Register Read Procedure

Sequential read operations allow the master to read from each register in order. The register pointer is automatically incremented by one after each read. This procedure, as shown in Figure 9, is more efficient than the Random Register Read if several registers must be read from.

To perform a read procedure, the R/W bit that is transmitted after the seven-bit I²C address is a logic-low, as in the Register Write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits all data starting with the initial addressed register. The register address pointer will overflow if the initial register address is larger than zero. After the last byte of data, the master does not acknowledge the transfer but does generate a STOP condition.

April 1999

Figure 6: Random Register Write Procedure (I²C-bus)

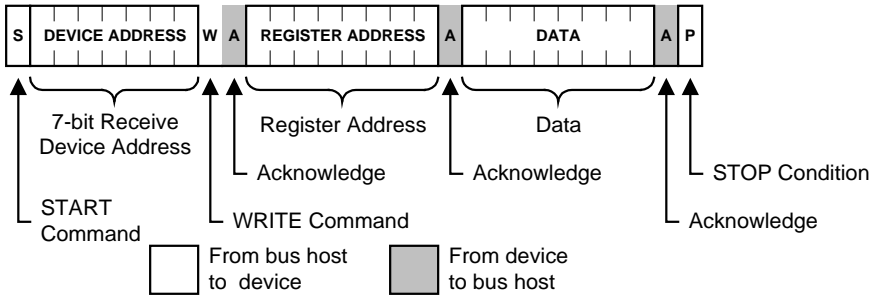


Figure 7: Random Register Read Procedure (I²C-bus)

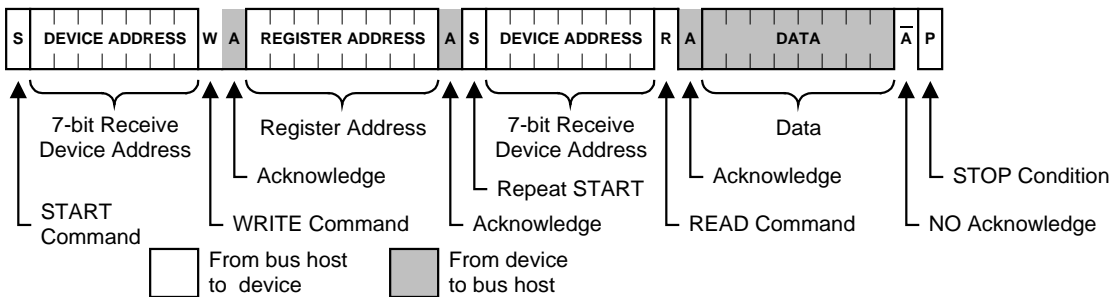


Figure 8: Sequential Register Write Procedure (I²C-bus)

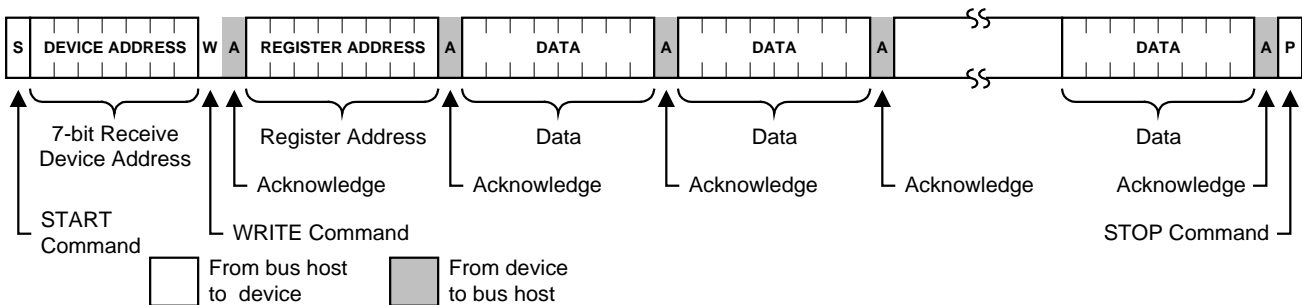
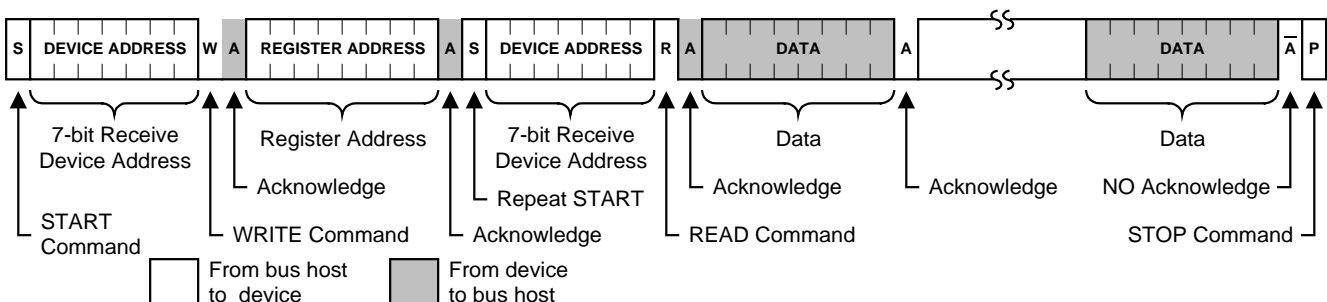


Figure 9: Sequential Register Read Procedure (I²C-bus)



4.2.6 SMBus: Block Write

SMBus

The Block Write command permits the master to write several bytes of data to sequential registers, starting by default at Register 0. The Block Write command, as noted in Figure 10, begins with the seven-bit SMBus device address followed by a logic-low R/W bit to begin a Write command. Following an acknowledge of the SMBus address and R/W bit by the slave device, a command code is written. *It is defined that all eight bits of the command code must be zero (0).*

After the command code of zero and an acknowledge, the host then issues a byte count that describes the number of data bytes to be written. According to SMBus convention, the byte count should be a value between 0 and 32; however this slave device ignores the byte count value.

Following an acknowledge of the byte count, data bytes may be written starting with Register 0 and incrementing sequentially. An acknowledge by the device between each byte of data must occur before the next data byte is sent.

registers, starting by default at Register 0. To perform a Block Read procedure the R/W bit that is transmitted after the seven-bit SMBus address is a logic-low, as in the Block Write procedure. The write bit resets the register address pointer to zero. Following an acknowledge of the SMBus address and R/W bit by the slave device, a command code is written. *It is defined that all eight bits of the command code must be zero (0).*

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave SMBus address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read.

The slave will acknowledge the device address, and then will expect a byte count value (which will be ignored). Following the byte count value, the device will take command of the bus and will transmit all the data beginning with Register 0. After the last byte of data, the master does not acknowledge the transfer but does generate a STOP condition.

If the master does not want to receive all the data, the master can not acknowledge the last data byte and then can issue a STOP condition of the next clock.

4.2.7 SMBus: Block Read

The Block Read command, shown in Figure 11, permits the master to read several bytes of data from sequential

Figure 10: Block Write (SMBus)

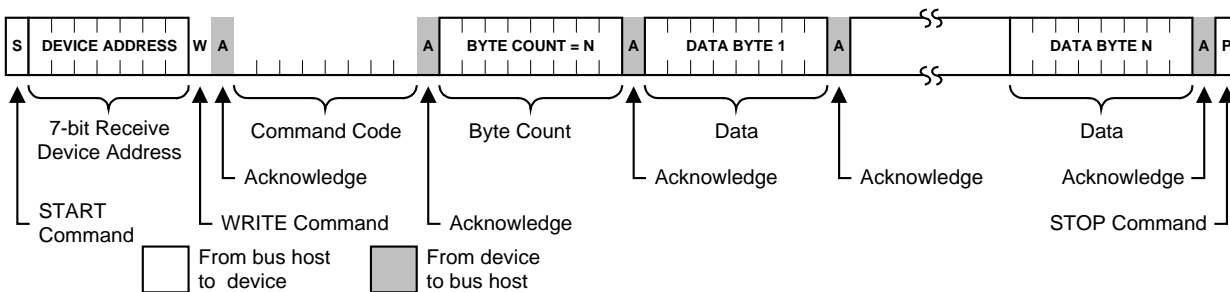
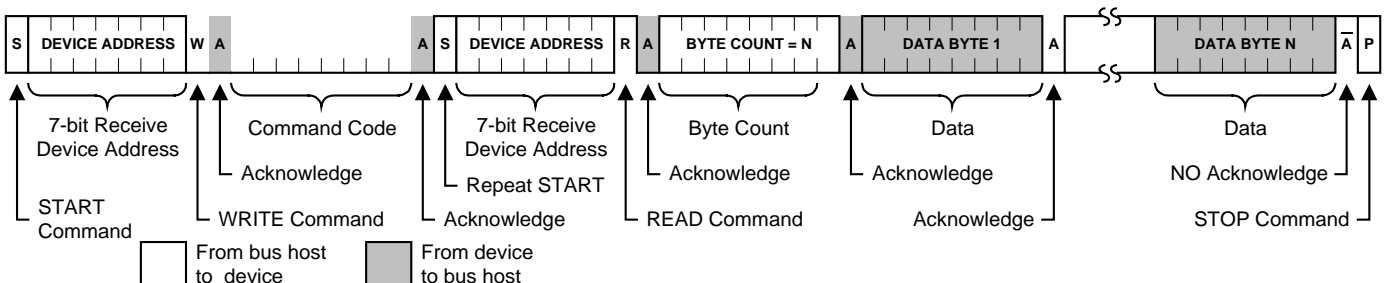


Figure 11: Block Read (SMBus)



April 1999

5.0 Electrical Specifications

Table 7: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

| PARAMETER | SYMBOL | MIN. | MAX. | UNITS |
|---|---------------|--------------|--------------|-------|
| Supply Voltage, dc, Clock Buffers ($V_{SS} = \text{ground}$) | V_{DD} | $V_{SS}-0.5$ | 7 | V |
| Supply Voltage, dc, Serial Communications | V_{DD_I2C} | $V_{SS}-0.5$ | 7 | V |
| Input Voltage, dc | V_I | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V |
| Output Voltage, dc | V_O | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V |
| Input Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$) | I_{IK} | -50 | 50 | mA |
| Output Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$) | I_{OK} | -50 | 50 | mA |
| Storage Temperature Range (non-condensing) | T_S | -65 | 150 | °C |
| Ambient Temperature Range, Under Bias | T_A | -55 | 125 | °C |
| Junction Temperature | T_J | | 125 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7) | | | 2 | kV |



CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 8: Operating Conditions

| PARAMETER | SYMBOL | CONDITIONS/DESCRIPTION | MIN. | TYP. | MAX. | UNITS |
|---------------------------------------|---------------|------------------------|-------|------|-------|-------|
| Supply Voltage, Clock Buffers | V_{DD} | $3.3V \pm 5\%$ | 3.135 | 3.3 | 3.465 | V |
| Supply Voltage, Serial Communications | V_{DD_I2C} | $3.3V \pm 5\%$ | 3.135 | 3.3 | 3.465 | V |
| Ambient Operating Temperature Range | T_A | | 0 | | 70 | °C |
| Input Frequency | f_{CLK} | | 0 | | 133 | MHz |
| Output Load Capacitance | C_L | | | | 30 | pF |
| Serial Data Transfer Rate | | Standard mode | 10 | 100 | 400 | kb/s |

FS6050/FS6051/FS6053/FS6054

Low-Skew Clock Fanout Buffer ICs



April 1999

Table 9: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical. Negative currents indicate current flows out of the device.

| PARAMETER | SYMBOL | CONDITIONS/DESCRIPTION | MIN. | TYP. | MAX. | UNITS |
|--|---------------|---|--------------|------|--------------|---------------|
| Overall (FS6050) | | | | | | |
| Supply Current, Dynamic, with Loaded Outputs | I_{DD} | $f_{CLK} = 100\text{MHz}; V_{DD} = 3.47\text{V}$ | | 180 | 360 | mA |
| Supply Current, Static | I_{DDL} | Outputs low; $V_{DD} = 3.47\text{V}$ | | 0.75 | 3 | mA |
| Serial Communication Inputs/Output (SDA, SCL) | | | | | | |
| High-Level Input Voltage | V_{IH} | Outputs low | 2.31 | | $V_{DD}+0.3$ | V |
| Low-Level Input Voltage | V_{IL} | Outputs low | $V_{SS}-0.3$ | | 0.9 | V |
| Hysteresis Voltage * | V_{hys} | Outputs low | 1.0 | | | V |
| High-Level Input Current | I_{IH} | | -1 | | 1 | μA |
| Low-Level Input Current (pull-up) | I_{IL} | Outputs low; $V_{IH} = 0.4\text{V}, V_{DD} = 3.47\text{V}$. Note: SDA requires an external pull-up to drive the data bus. | 5 | 11 | 15 | μA |
| Low-Level Output Sink Current (SDA) | I_{OL} | $V_{OL} = 0.4\text{V}$ | 10 | 25 | | mA |
| Output Enable Input (OE) | | | | | | |
| High-Level Input Voltage | V_{IH} | | 2.0 | | $V_{DD}+0.3$ | V |
| Low-Level Input Voltage | V_{IL} | | $V_{SS}-0.3$ | | 0.8 | V |
| High-Level Input Current | I_{IH} | | -1 | | 1 | μA |
| Low-Level Input Current (pull-up) | I_{IL} | $V_{IH} = 0.4\text{V}; V_{DD} = 3.47\text{V}$ | 10 | 22 | 30 | μA |
| Clock Input (CLK_IN) | | | | | | |
| High-Level Input Voltage | V_{IH} | | 2.0 | | $V_{DD}+0.3$ | V |
| Low-Level Input Voltage | V_{IL} | | $V_{SS}-0.3$ | | 0.8 | V |
| Input Leakage Current | I_I | | -1 | | 1 | μA |
| Clock Outputs (SDRAM_0:17 3.3V Type 4 Clock Buffer) | | | | | | |
| High-Level Output Source Current | $I_{OH\ min}$ | $V_{DD} = 3.135\text{V}, V_O = 2.0\text{V}$ | -54 | -65 | | mA |
| | $I_{OH\ max}$ | $V_{DD} = 3.465\text{V}, V_O = 3.135\text{V}$ | | -28 | -46 | |
| Low-Level Output Sink Current | $I_{OL\ min}$ | $V_{DD} = 3.135\text{V}, V_O = 1.0\text{V}$ | 54 | 69 | | mA |
| | $I_{OL\ max}$ | $V_{DD} = 3.465\text{V}, V_O = 0.4\text{V}$ | | 33 | 53 | |
| Output Impedance | Z_{OH} | $V_O = 0.5V_{DD}$; output driving high | 10 | 17.9 | 24 | Ω |
| | Z_{OL} | $V_O = 0.5V_{DD}$; output driving low | 10 | 16.3 | 24 | |
| Tristate Output Current | I_{OZ} | | -5 | | 5 | μA |
| Short Circuit Source Current * | I_{OSH} | $V_O = 0\text{V}$; shorted for 30s, max. | | -106 | | mA |
| Short Circuit Sink Current * | I_{OSL} | $V_O = 3.3\text{V}$; shorted for 30s, max. | | 107 | | mA |

April 1999

Table 10: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical.

| PARAMETER | SYMBOL | CONDITIONS/DESCRIPTION | CLOCK (MHz) | MIN. | TYP. | MAX. | UNITS |
|--|---|---|-------------|------|------|------|-------|
| Overall | | | | | | | |
| Clock Skew, Maximum; SDRAM_0 to any SDRAM pin * | t_{skw} | Measured on the rising edge at 1.5V; $C_L = 20\text{pF}$ | 66.67 | | 182 | | ps |
| | | | 100 | | 228 | | |
| Propagation Delay, Average; CLK_IN to any SDRAM pin * | $t_{PLH(min)}$ | Measured on the rising edge at 1.5V; $C_L = 20\text{pF}$ | 66.67 | | 3.7 | | ns |
| | | | 100 | | 3.8 | | |
| | $t_{PLH(max)}$ | Measured on the rising edge at 1.5V; $C_L = 30\text{pF}$ | 66.67 | | 3.7 | | |
| | | | 100 | | 4.0 | | |
| | $t_{PHL(min)}$ | Measured on the rising edge at 1.5V; $C_L = 20\text{pF}$ | 66.67 | | 3.9 | | |
| | | | 100 | | 3.8 | | |
| $t_{PHL(max)}$ | Measured on the rising edge at 1.5V; $C_L = 30\text{pF}$ | 66.67 | | 4.2 | | | |
| | | 100 | | 4.0 | | | |
| Clock Outputs (SDRAM_0:17 3.3V Type 4 Clock Buffer) | | | | | | | |
| Rise Time * | $t_{r(min)}$ | $V_O = 0.4\text{V}$ to 2.4V ; $C_L = 20\text{pF}$ | 66.67 | | 1.0 | | ns |
| | | | 100 | | 0.9 | | |
| | $t_{r(max)}$ | $V_O = 0.4\text{V}$ to 2.4V ; $C_L = 30\text{pF}$ | 66.67 | | 1.2 | | |
| | | | 100 | | 1.0 | | |
| Fall Time * | $t_{f(min)}$ | $V_O = 2.4\text{V}$ to 0.4V ; $C_L = 20\text{pF}$ | 66.67 | | 1.0 | | ns |
| | | | 100 | | 0.7 | | |
| | $t_{f(max)}$ | $V_O = 2.4\text{V}$ to 0.4V ; $C_L = 30\text{pF}$ | 66.67 | | 1.1 | | |
| | | | 100 | | 0.8 | | |
| Clock High Time * | $t_{KH(min)}$ | $V_O = 2.4\text{V}$; $C_L = 20\text{pF}$ | 66.67 | | 6.5 | | ns |
| | | | 100 | | 3.8 | | |
| | $t_{KH(max)}$ | $V_O = 2.4\text{V}$; $C_L = 30\text{pF}$ | 66.67 | | 6.5 | | |
| | | | 100 | | 3.8 | | |
| Clock Low Time * | $t_{KL(min)}$ | $V_O = 0.4\text{V}$; $C_L = 20\text{pF}$ | 66.67 | | 6.5 | | ns |
| | | | 100 | | 4.6 | | |
| | $t_{KL(max)}$ | $V_O = 0.4\text{V}$; $C_L = 30\text{pF}$ | 66.67 | | 6.3 | | |
| | | | 100 | | 4.5 | | |
| Duty Cycle * | | From rising edge to rising edge at 1.5V; $C_L = 20\text{pF}$ | 66.67 | | 49 | | % |
| | | | 100 | | 45 | | |
| | | From rising edge to rising edge at 1.5V; $C_L = 30\text{pF}$ | 66.67 | | 50 | | |
| | | | 100 | | 46 | | |
| Tristate Enable Delay * | t_{PZL} | Output tristated to output active; $C_L = 20\text{pF}$ | | | 4.7 | | ns |
| | t_{PZH} | | | | 4.6 | | |
| Tristate Disable Delay * | t_{PLZ} | Output active to output tristated; $C_L = 20\text{pF}$ | | | 6.3 | | ns |
| | t_{PHZ} | | | | 7.9 | | |

FS6050/FS6051/FS6053/FS6054

Low-Skew Clock Fanout Buffer ICs



April 1999

Table 11: Serial Interface Timing Specifications

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range $T_A = 0^\circ\text{C}$ to 70°C . Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are $\pm 3\sigma$ from typical.

| PARAMETER | SYMBOL | CONDITIONS/DESCRIPTION | MIN. | MAX. | UNITS |
|--------------------------------------|---------------------|---|------|------|---------------|
| Clock frequency | f_{SCL} | SCL | 10 | 400 | kHz |
| Bus free time between STOP and START | t_{BUF} | | 4.7 | | μs |
| Set up time, START (repeated) | $t_{\text{su:STA}}$ | | 4.7 | | μs |
| Hold time, START | $t_{\text{hd:STA}}$ | | 4.0 | | μs |
| Set up time, data input | $t_{\text{su:DAT}}$ | SDA | 250 | | ns |
| Hold time, data input | $t_{\text{hd:DAT}}$ | SDA | 300 | | ns |
| Output data valid from clock | t_{AA} | Minimum delay to bridge undefined region of the falling edge of SCL to avoid unintended START or STOP | | 3.5 | μs |
| Rise time, data and clock | t_r | SDA, SCL | | 1000 | ns |
| Fall time, data and clock | t_f | SDA, SCL | | 300 | ns |
| High time, clock | t_H | SCL | 4.0 | | μs |
| Low time, clock | t_L | SCL | 4.7 | | μs |
| Set up time, STOP | $t_{\text{su:STO}}$ | | 4.0 | | μs |

Figure 12: Bus Timing Data

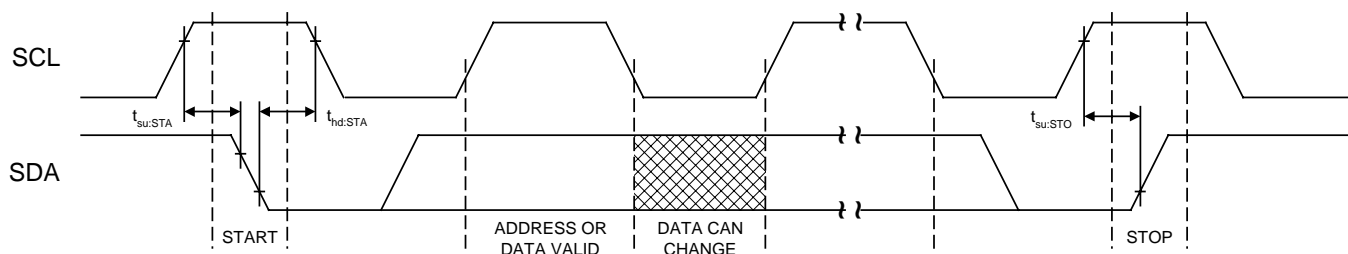
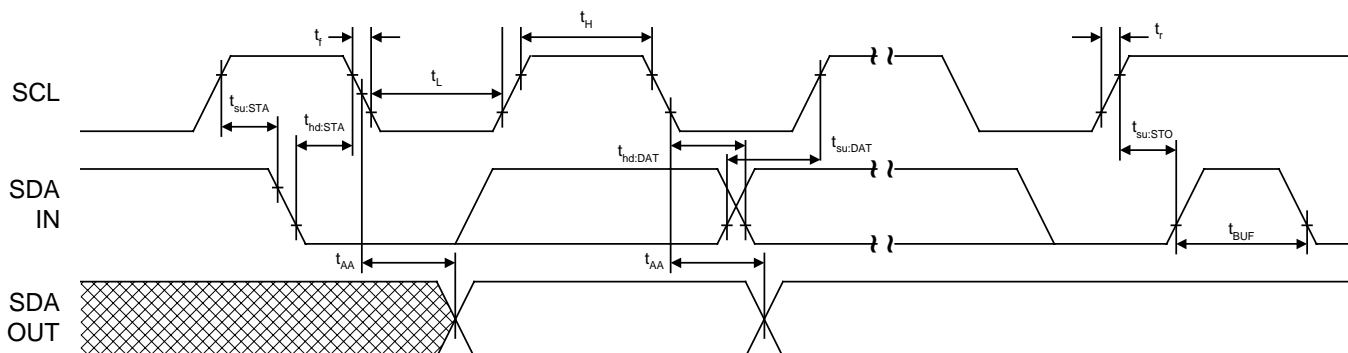


Figure 13: Data Transfer Sequence



April 1999

Figure 14: SDRAM_0:17 Clock Output (3.3V Type 4 Clock Buffer)

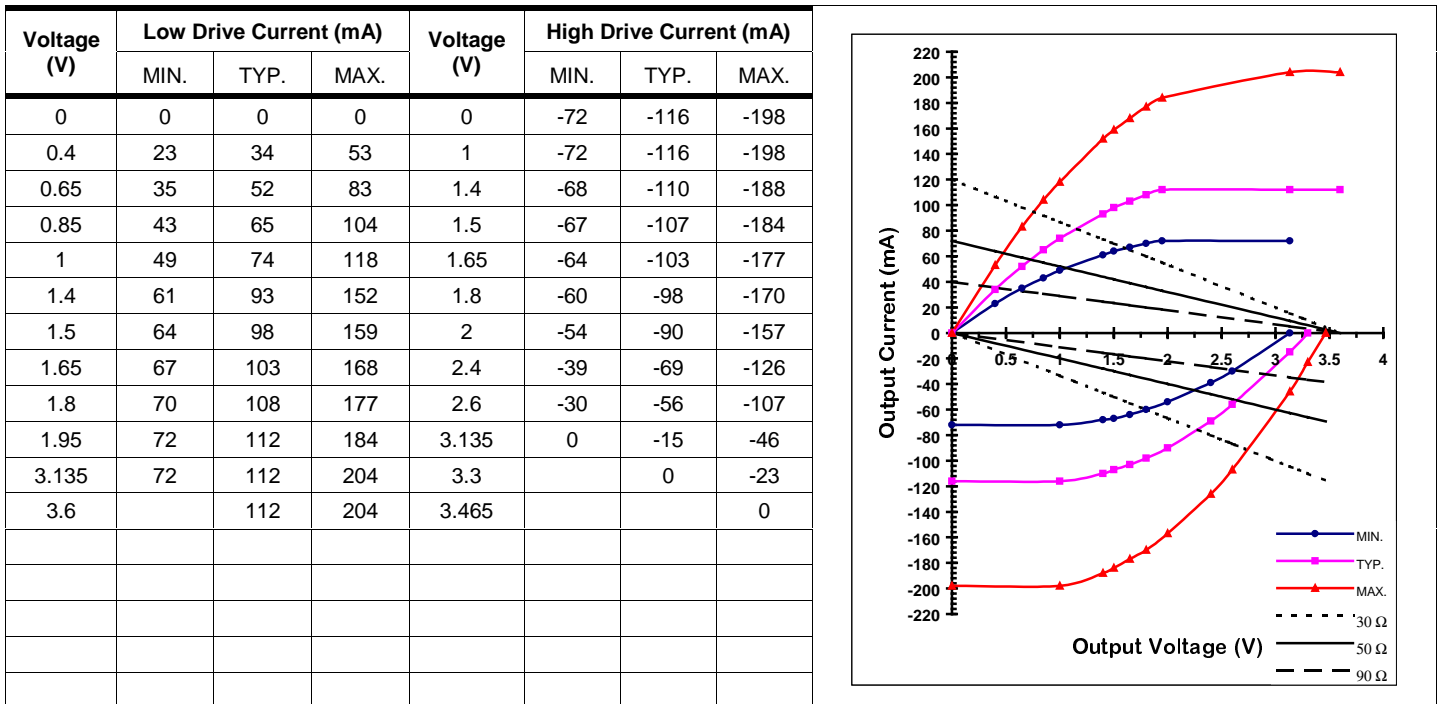


Figure 15: DC Measurement Points

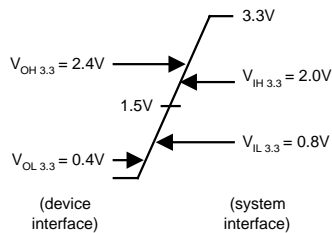


Figure 17: Timing Measurement Points

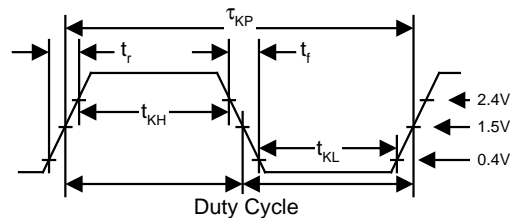
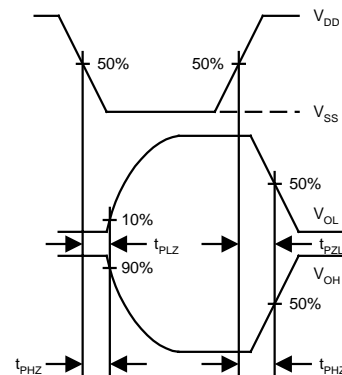
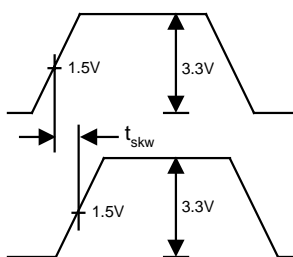


Figure 16: Clock Skew Measurement Point



FS6050/FS6051/FS6053/FS6054

Low-Skew Clock Fanout Buffer ICs



April 1999

6.0 Package Information

Table 12: 48-pin SSOP (7.5mm/0.300") Package Dimensions

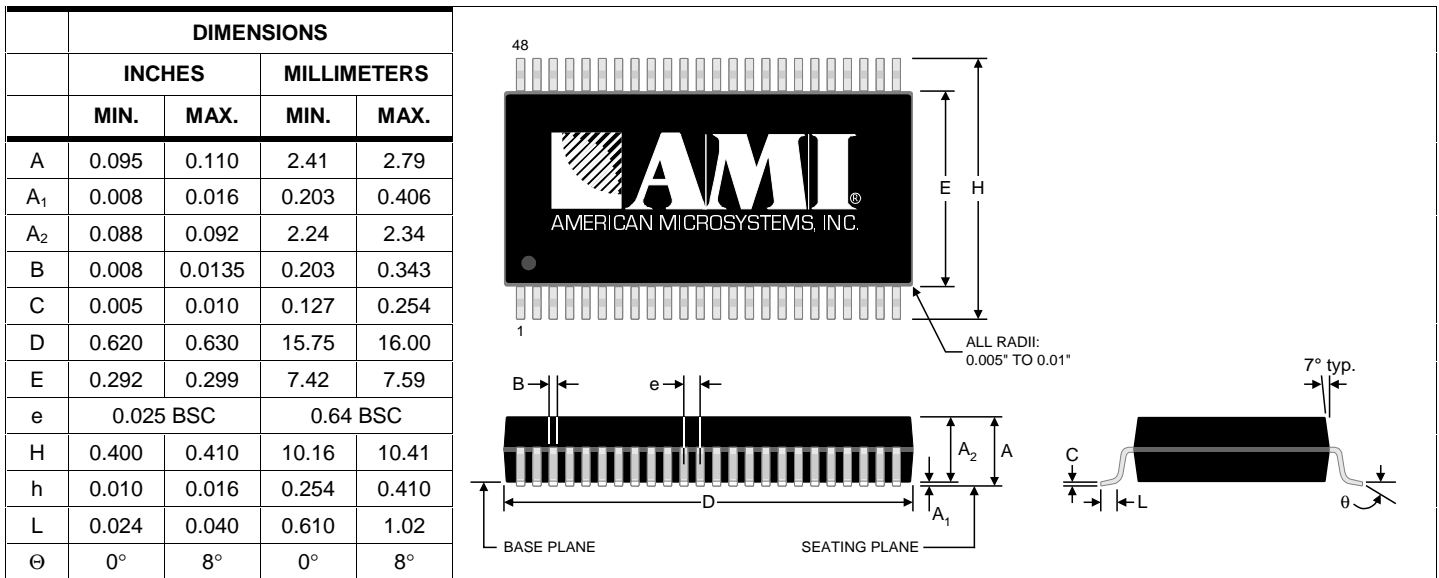


Table 13: 48-pin SSOP (7.5mm/0.300") Package Characteristics

| PARAMETER | SYMBOL | CONDITIONS/DESCRIPTION | TYP. | UNITS |
|---|---------------|----------------------------------|------|-------|
| Thermal Impedance, Junction to Free-Air | Θ_{JA} | Air flow = 0 m/s | 93 | °C/W |
| Lead Inductance, Self | L_{11} | Center lead | 3.3 | nH |
| Lead Inductance, Mutual | L_{12} | Center lead to any adjacent lead | 1.6 | nH |
| Lead Capacitance, Bulk | C_{11} | Center lead to V_{SS} | 0.6 | pF |
| Lead Capacitance, Mutual | C_{12} | Center lead to any adjacent lead | 0.2 | pF |

April 1999

Table 14: 28-pin SOIC (7.5mm/0.300") Package Dimensions

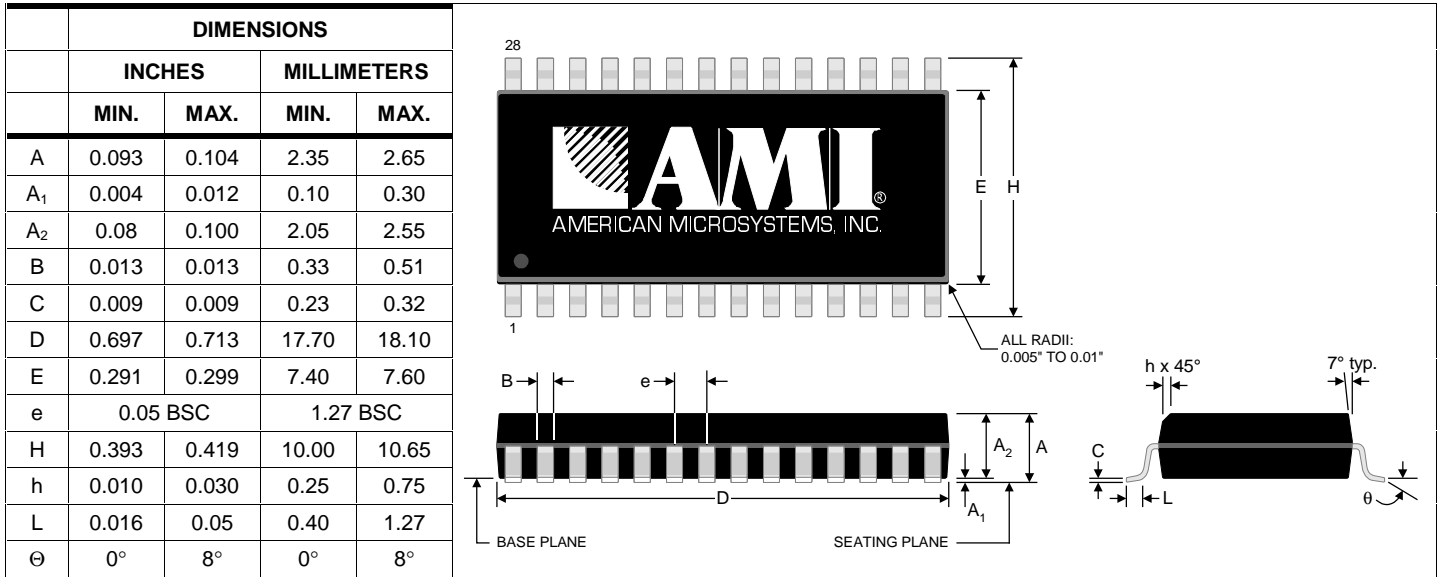


Table 15: 28-pin SOIC (7.5mm/0.300") Package Characteristics

| PARAMETER | SYMBOL | CONDITIONS/DESCRIPTION | TYP. | UNITS |
|---|-----------------|----------------------------------|------|-------|
| Thermal Impedance, Junction to Free-Air | Θ_{JA} | Air flow = 0 m/s | 80 | °C/W |
| Lead Inductance, Self | L ₁₁ | Center lead | 2.5 | nH |
| Lead Inductance, Mutual | L ₁₂ | Center lead to any adjacent lead | 0.85 | nH |
| Lead Capacitance, Bulk | C ₁₁ | Center lead to V _{SS} | 0.42 | pF |
| Lead Capacitance, Mutual | C ₁₂ | Center lead to any adjacent lead | 0.08 | pF |

FS6050/FS6051/FS6053/FS6054

Low-Skew Clock Fanout Buffer ICs



April 1999

Table 16: 28-pin SSOP (5.3mm/0.209") Package Dimensions

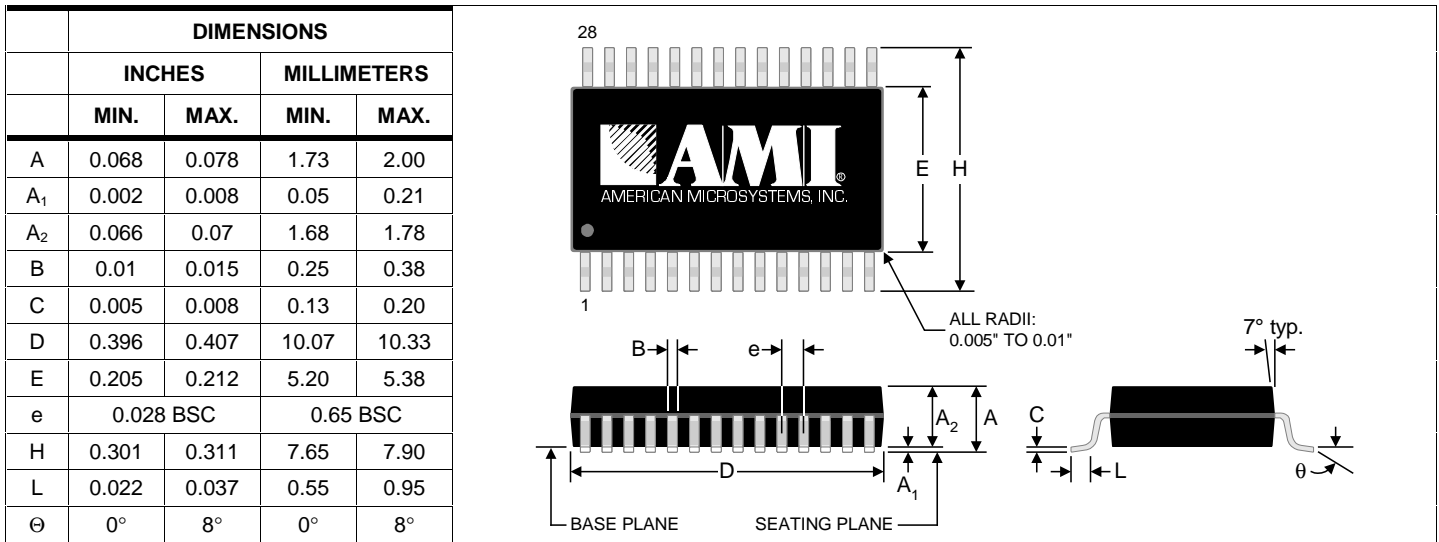


Table 17: 28-pin SSOP (5.3mm/0.209") Package Characteristics

| PARAMETER | SYMBOL | CONDITIONS/DESCRIPTION | TYP. | UNITS |
|---|-----------------|----------------------------------|------|-------|
| Thermal Impedance, Junction to Free-Air | Θ_{JA} | Air flow = 0 m/s | 97 | °C/W |
| Lead Inductance, Self | L ₁₁ | Center lead | 2.24 | nH |
| Lead Inductance, Mutual | L ₁₂ | Center lead to any adjacent lead | 0.95 | nH |
| Lead Capacitance, Bulk | C ₁₁ | Center lead to V _{SS} | 0.25 | pF |
| Lead Capacitance, Mutual | C ₁₂ | Center lead to any adjacent lead | 0.07 | pF |

April 1999

7.0 Ordering Information

| DEVICE NUMBER | ORDERING CODE | PACKAGE TYPE | OPERATING TEMPERATURE RANGE | SHIPPING CONFIGURATION |
|---------------|------------------|----------------------------|-----------------------------|------------------------|
| FS6050 | 11257-801 | 48-pin (7.5mm/0.300") SSOP | 0°C to 70°C (Commercial) | Tape and Reel |
| | 11257-811 | 48-pin (7.5mm/0.300") SSOP | 0°C to 70°C (Commercial) | Tube |
| FS6051 | 11257-802 | 28-pin (7.5mm/0.300") SOIC | 0°C to 70°C (Commercial) | Tape and Reel |
| | 11257-812 | 28-pin (7.5mm/0.209") SOIC | 0°C to 70°C (Commercial) | Tube |
| | 11257-806 | 28-pin (5.3mm/0.209") SSOP | 0°C to 70°C (Commercial) | Tape and Reel |
| | 11257-816 | 28-pin (5.3mm/0.209") SSOP | 0°C to 70°C (Commercial) | Tube |
| FS6053 | 11257-803 | 28-pin (7.5mm/0.300") SOIC | 0°C to 70°C (Commercial) | Tape and Reel |
| | 11257-813 | 28-pin (7.5mm/0.300") SOIC | 0°C to 70°C (Commercial) | Tube |
| FS6054 | 11257-804 | 28-pin (7.5mm/0.300") SOIC | 0°C to 70°C (Commercial) | Tape and Reel |
| | 11257-814 | 28-pin (7.5mm/0.300") SOIC | 0°C to 70°C (Commercial) | Tube |



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8.0 Application Information

8.1 Reduction of EMI

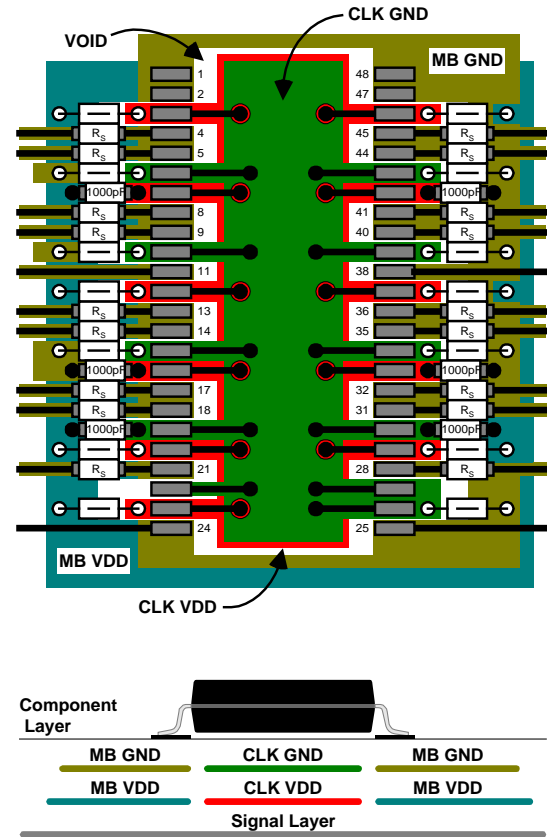
The primary concern when designing the board layout for this device is the reduction of electromagnetic interference (EMI) generated by the 18 copies of the 100MHz SDRAM clock. It is assumed the reader is familiar with basic transmission line theory.

8.1.1 Layout Guidelines

To obtain the best performance, noise should be minimized on the power and ground supplies to the IC. Observe good high-speed board design practices, such as:

- Use multi-layer circuit boards with dedicated low impedance power and ground planes for the device (denoted as CLK VDD and CLK GND in Figure 18). The device power and ground planes should be completely isolated from the motherboard power and ground planes by a void in the power planes.
- Several low-pass filters using low impedance ferrite beads (5Ω at 100MHz) are recommended to decouple the device power and ground planes from the motherboard power and ground planes (MB VDD and MB GND). The beads should span the gap between the power and ground planes. Seven beads for power and seven beads for ground are suggested (14 total) so that the clock rise times ($1V/ns$) can be maintained.
- Place 1000pF bypass capacitors as close as possible to the power pins of the IC. Use RF-quality low-inductance multi-layer ceramic chip capacitors. Six capacitors is optimal, one on each power/ground grouping as shown in Figure 18.
- Load similar clock outputs equally, and keep output loading as light as possible to help reduce clock skew and power dissipation.
- Use equal-length clock traces that are as short as possible. Rounded trace corners help reduce reflections and ringing in the clock signal.
- The clock traces must never cross the void area between power/ground planes. Each trace must have a complete plane (either VDD or GND) under the complete length of the trace.

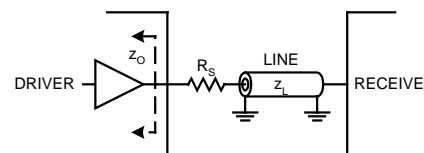
Figure 18: Board Layout



8.1.2 Output Driver Termination

A signal reflection will occur at any point on a PC-board trace where impedance mismatches exist. Reflections cause several undesirable effects in high-speed applications, such as an increase in clock jitter and a rise in electromagnetic emissions from the board. Using a properly designed series termination on each high-speed line can alleviate these problems by eliminating signal reflections.

Figure 19: Series Termination



April 1999

Series termination adds no dc loading to the driver, and requires less power than other resistive termination methods. Further, no extra impedance exists from the signal line to a reference voltage, such as ground.

As shown in Figure 19, the sum of the driver's output impedance (z_o) and the series termination resistance (R_s) must equal the line impedance (z_L). That is,

$$R_s = z_L - z_o.$$

Note that when the source impedance ($z_o + R_s$) is matched to the line impedance, then by voltage division the incident wave amplitude is one-half of the full signal amplitude.

$$V_i = V \frac{(z_o + R_s)}{(z_o + R_s) + z_L} = \frac{V}{2}$$

The full signal amplitude may take up to twice as long as the propagation delay of the line to develop, reducing noise immunity during the half-amplitude period. Note also that the voltage at the receive end must add up to a signal amplitude that meets the receiver switching thresholds. The slew rate of the signal is also reduced due to the additional RC delay of the load capacitance and the line impedance. Also note that the output driver impedance will vary slightly with the output logic state (high or low).

8.2 Dynamic Power Dissipation

High-speed clock drivers require careful attention to power dissipation. Transient power (P_T) consumption can be derived from

$$P_T = V_{DD}^2 \times C_{load} \times f_{CLK} \times N_{sw}$$

where C_{load} is the load capacitance, V_{DD} is the supply voltage, f_{CLK} is the clock frequency, and N_{sw} is the number of switching outputs.

The internal heat (junction temperature, T_J) generated by the power dissipation can be calculated from

$$T_J = \Theta_{JA} \times P_T + T_A$$

where Θ_{JA} is the package thermal resistance, T_A is the ambient temperature, and P_T is derived above.

8.3 Serial Communications

Connection of devices to a standard-mode implementation of either the I²C-bus or the SMBus is similar to that shown in Figure 20. Selection of the pull-up resistors (R_p) and the optional series resistors (R_s) on the SDA and SCL lines depends on the supply voltage, the bus ca-

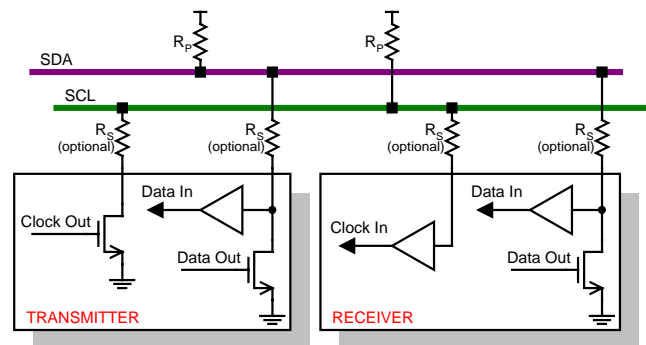
pacitance, and the number of connected devices with their associated input currents.

Control of the clock and data lines is done through open drain/collector current-sink outputs, and thus requires external pull-up resistors on both lines. A guideline is

$$R_p < \frac{t_r}{2 \times C_{bus}},$$

where t_r is the maximum rise time (minus some margin) and C_{bus} is the total bus capacitance. Assuming an I²C device on each DIMM, an I²C controller, the clock buffer, and two other bus devices results in values in the 5k Ω to 7k Ω range. Use of a series resistor to provide protection against high voltage spikes on the bus will alter the values for R_p .

Figure 20: Connections to the Serial Bus



8.3.1 For More Information

More detailed information on serial bus design can be obtained from SMBus and I²C Bus Design, available from the Intel Corporation at <http://www.intel.com>.

Information on the I²C-bus can be found in the document The I²C-bus And How To Use It (Including Specifications), available from Philips Semiconductors at <http://www-us2.semiconductors.philips.com>.

Additional information on the System Management Bus can be found in the System Management Bus Specification, available from the Smart Battery System Implementers' Forum at <http://www.sbs-forum.org>.