16 V Rail-to-Rail Operational Amplifiers

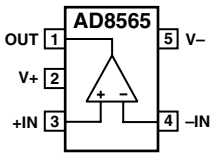
AD8565/AD8566/AD8567

FEATURES
Single-Supply Operation: 4.5 V to 16 V
Input Capability beyond the Rails
Rail-to-Rail Output Swing
Continuous Output Current: 35 mA
Peak Output Current: 250 mA
Offset Voltage: 10 mV
Slew Rate: 6 V/μs
Unity Gain Stable with Large Capacitive Loads
Supply Current: 700 μA per Amplifier

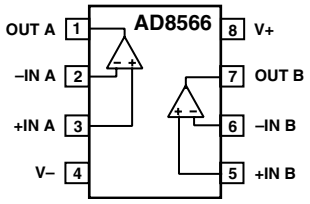
APPLICATIONS
LCD Reference Drivers
Portable Electronics
Communications Equipment

PIN CONFIGURATIONS

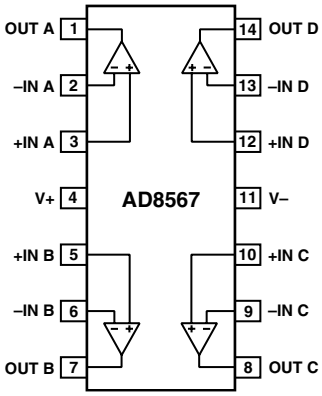
5-Lead SC70 (KS Suffix)



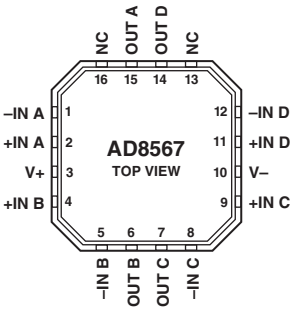
8-Lead MSOP (RM Suffix)



14-Lead TSSOP (RU Suffix)



16-Lead LFCSP (CP Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The AD8565, AD8566, and AD8567 are low cost, single-supply rail-to-rail input and output operational amplifiers optimized for LCD monitor applications. They are built on an advanced high voltage CBCMOS process. The AD8565 contains a single amplifier, the AD8566 has two amplifiers, and the AD8567 has four amplifiers.

These LCD op amps have high slew rates, 35 mA continuous output drive, 250 mA peak output drive, and high capacitive load drive capability. They have a wide supply range and offset voltages below 10 mV. The AD8565, AD8566, and AD8567 are ideal for LCD grayscale reference buffer and V_{COM} applications.

The AD8565, AD8566, and AD8567 are specified over the –40°C to +85°C temperature range. The AD8565 single is available in a 5-lead SC70 package. The AD8566 dual is available in an 8-lead MSOP package. The AD8567 quad is available in 14-lead TSSOP and 16-lead LFCSP packages.

REV. C

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AD8565/AD8566/AD8567–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($4.5\ V \le V_S \le 16\ V$, $V_{CM} = V_S/2$, $T_A = 25°C$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	10	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40°C \le T_A \le +85°C$		5		µV/°C
Input Bias Current	I_B			80	600	nA
		$-40°C \le T_A \le +85°C$			800	nA
Input Offset Current	I_{OS}			1	80	nA
		$-40°C \le T_A \le +85°C$			130	nA
Input Voltage Range		Common-Mode Input	–0.5		$V_S + 0.5$	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0$ to V_S,				
		$-40°C \le T_A \le +85°C$	54	95		dB
Large Signal Voltage Gain	AVO	$R_L = 10\ k\Omega$,				
		$V_O = 0.5\ V$ to $(V_S - 0.5\ V)$	3	10		V/mV
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 100\ \mu A$		$V_S - 0.005$		V
		$V_S = 16\ V$, $I_L = 5\ mA$	15.85	15.95		V
		$-40°C \le T_A \le +85°C$	15.75			V
		$V_S = 4.5\ V$, $I_L = 5\ mA$	4.2	4.38		V
		$-40°C \le T_A \le +85°C$	4.1			V
Output Voltage Low	V_{OL}	$I_L = 100\ \mu A$		5		mV
		$V_S = 16\ V$, $I_L = 5\ mA$		42	150	mV
		$-40°C \le T_A \le +85°C$			250	mV
		$V_S = 4.5\ V$, $I_L = 5\ mA$		95	300	mV
		$-40°C \le T_A \le +85°C$			400	mV
Continuous Output Current	I_{OUT}			35		mA
Peak Output Current	I_{PK}	$V_S = 16\ V$		250		mA
POWER SUPPLY						
Supply Voltage	V_S		4.5		16	V
Power Supply Rejection Ratio	PSRR	$V_S = 4\ V$ to $17\ V$,				
		$-40°C \le T_A \le +85°C$	70	90		dB
Supply Current/Amplifier	I_{SY}	$V_O = V_S/2$, No Load		700	850	µA
		$-40°C \le T_A \le +85°C$			1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\ k\Omega$, $C_L = 200\ pF$	4	6		V/µs
Gain Bandwidth Product	GBP	$R_L = 10\ k\Omega$, $C_L = 10\ pF$		5		MHz
Phase Margin	Øo	$R_L = 10\ k\Omega$, $C_L = 10\ pF$		65		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		26		$nV/\sqrt{Hz}$
	e_n	f = 10 kHz		25		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 10 kHz		0.8		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S) . . . . . 18 V
Input Voltage . . . . . –0.5 V to V_S + 0.5 V
Differential Input Voltage . . . . . V_S
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
5-Lead SC70 (KS)	376	126	°C/W
8-Lead MSOP (RM)	210	45	°C/W
14-Lead TSSOP (RU)	180	35	°C/W
16-Lead LFCSP (CP)	38[2]	30[2]	°C/W

NOTES
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for a device soldered onto a circuit board for surface-mount packages.
[2]DAP is soldered down to PCB.

ORDERING GUIDE

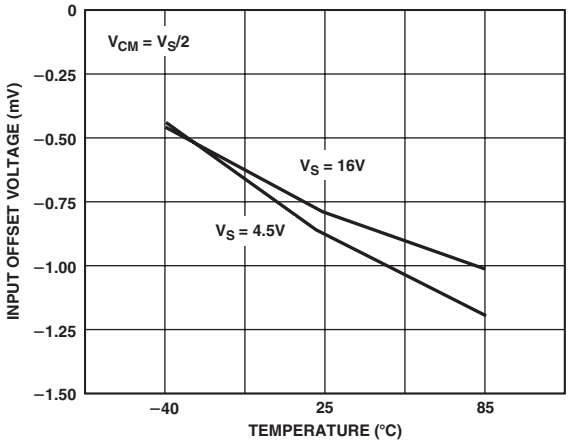
Model	Temperature Range	Package Description	Package Option	Branding
AD8565AKS-R2	–40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package	KS-5	ASA
AD8565AKS-REEL7	–40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package	KS-5	ASA
AD8565AKSZ-REEL7*	–40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package	KS-5	ASA
AD8566ARM-R2	–40°C to +85°C	8-Lead Micro Small Outline Package	RM-8	ATA
AD8566ARM-REEL	–40°C to +85°C	8-Lead Micro Small Outline Package	RM-8	ATA
AD8566ARMZ-REEL*	–40°C to +85°C	8-Lead Micro Small Outline Package	RM-8	ATA
AD8567ARU	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package	RU-14	
AD8567ARU-REEL	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package	RU-14	
AD8567ARUZ*	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package	RU-14	
AD8567ARUZ-REEL*	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package	RU-14	
AD8567ACP-R2	–40°C to +85°C	16-Lead Lead Frame Chip Scale Package	CP-16	
AD8567ACP-REEL	–40°C to +85°C	16-Lead Lead Frame Chip Scale Package	CP-16	
AD8567ACP-REEL7	–40°C to +85°C	16-Lead Lead Frame Chip Scale Package	CP-16	
AD8567ACPZ-REEL*	–40°C to +85°C	16-Lead Lead Frame Chip Scale Package	CP-16	
AD8567ACPZ-REEL7*	–40°C to +85°C	16-Lead Lead Frame Chip Scale Package	CP-16	

*Z = Pb-free part.

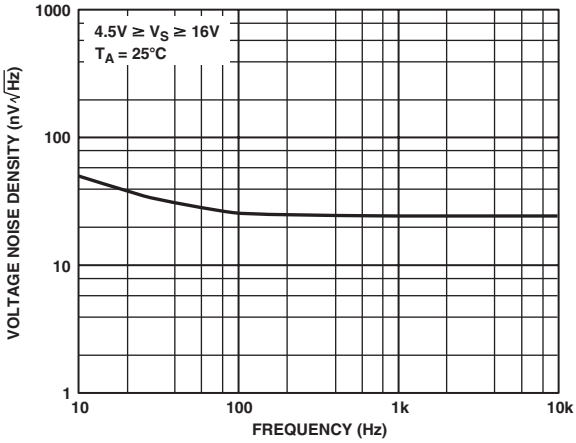
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8565/AD8566/AD8567 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

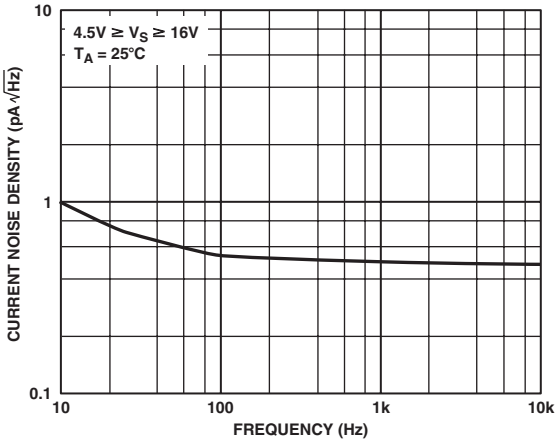
AD8565/AD8566/AD8567–Typical Performance Characteristics



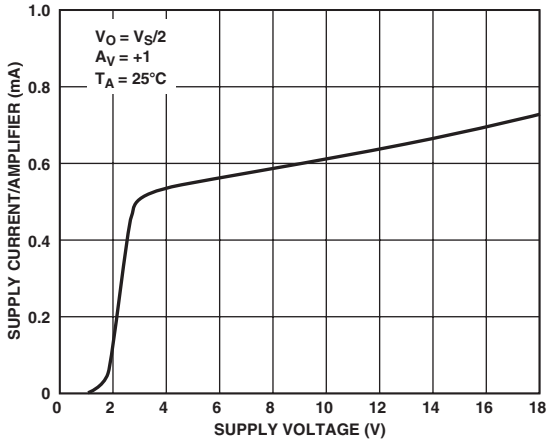
TPC 1. Input Offset Voltage vs. Temperature



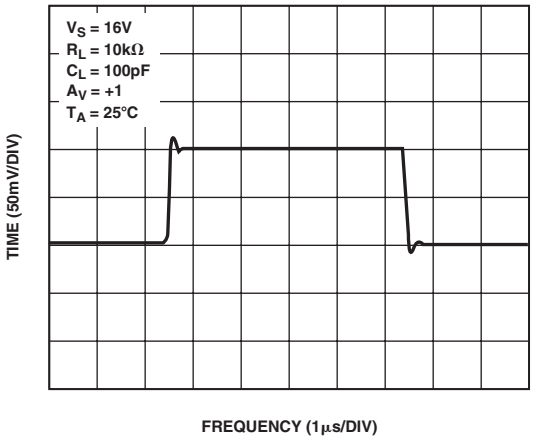
TPC 4. Voltage Noise Density vs. Frequency



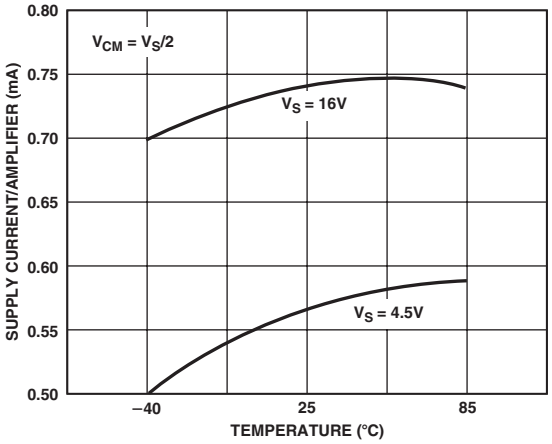
TPC 2. Current Noise Density vs. Frequency



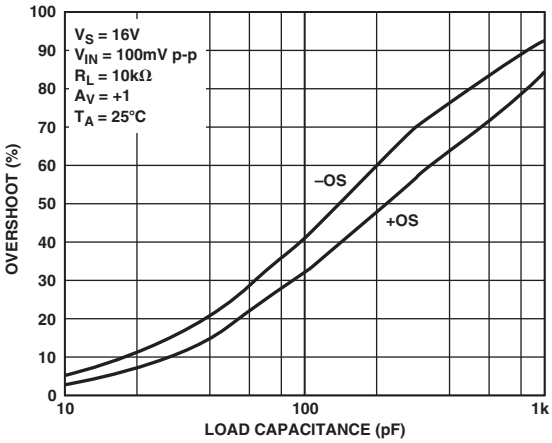
TPC 5. Supply Current/Amplifier vs. Supply Voltage



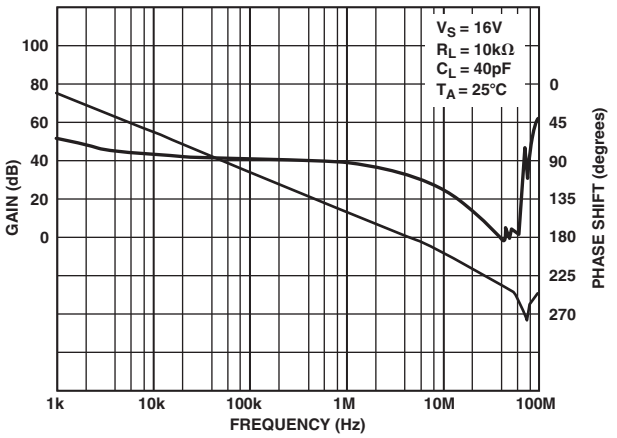
TPC 3. Small Signal Transient Response



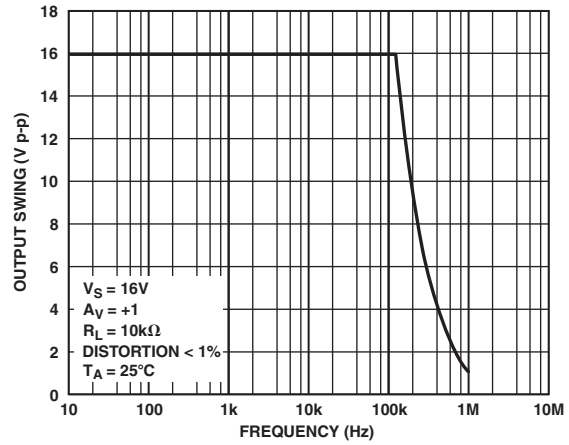
TPC 6. Supply Current/Amplifier vs. Temperature



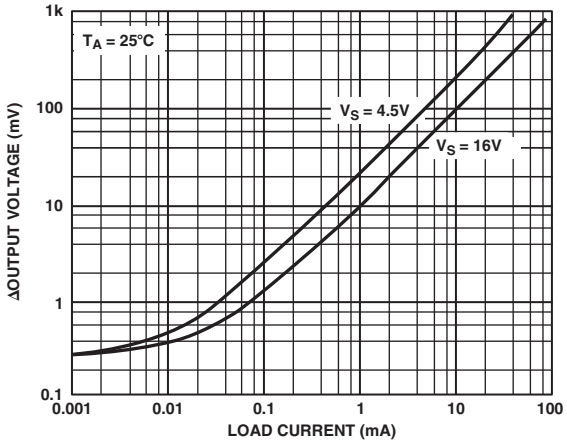
TPC 7. Small Signal Overshoot vs. Load Capacitance



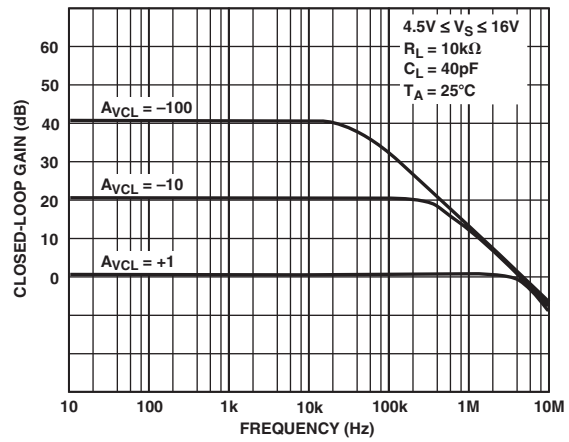
TPC 10. Open-Loop Gain and Phase Shift vs. Frequency



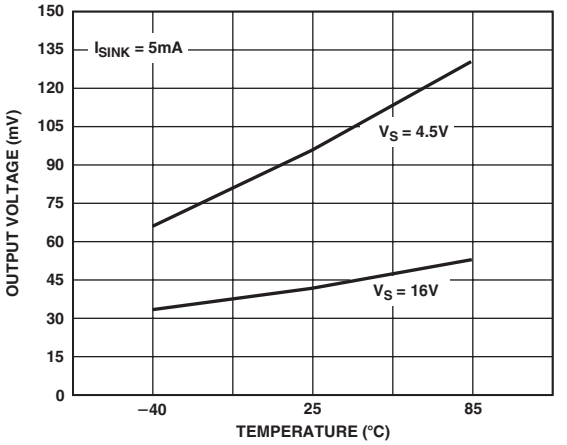
TPC 8. Closed-Loop Output Swing vs. Frequency



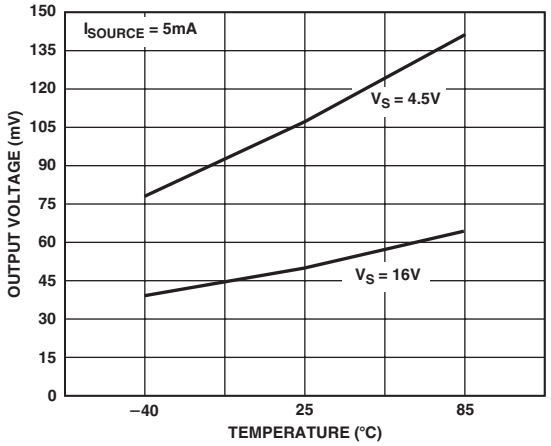
TPC 11. Output Voltage to Supply Rail vs. Load Current



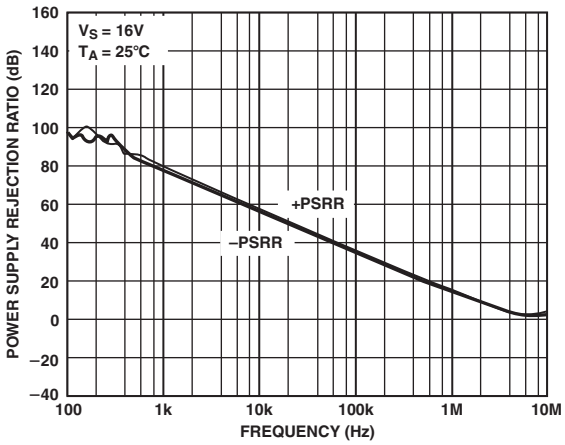
TPC 9. Closed-Loop Gain vs. Frequency



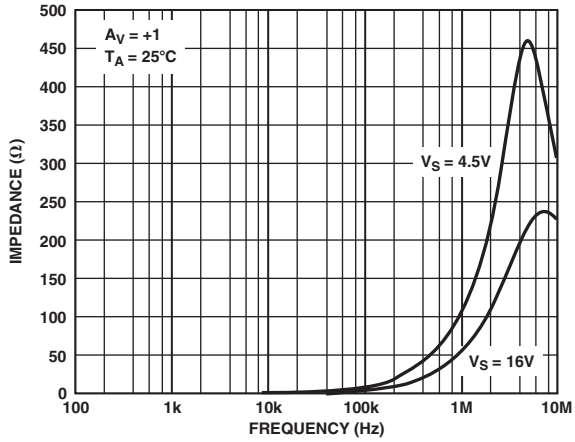
TPC 12. Output Voltage Swing to Rail vs. Temperature



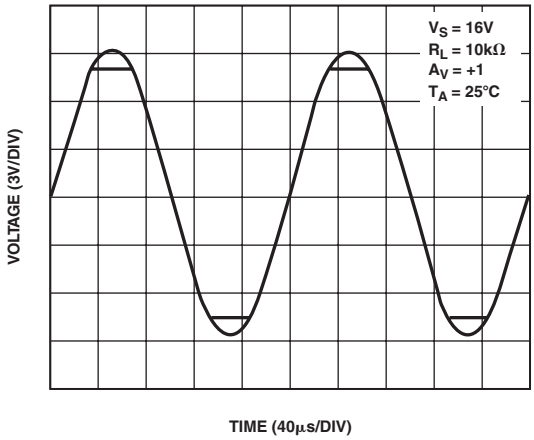
TPC 13. Output Voltage Swing to Rail vs. Temperature



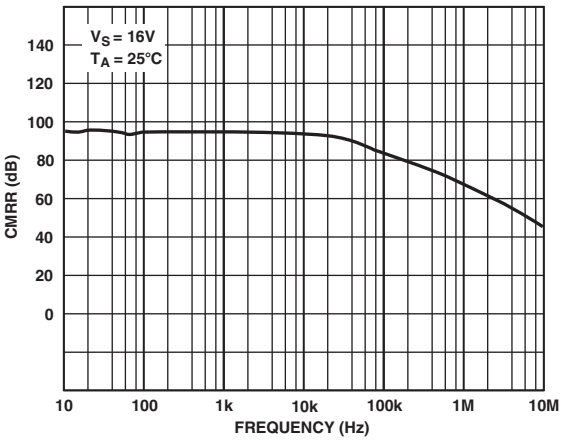
TPC 16. Power Supply Rejection Ratio vs. Frequency



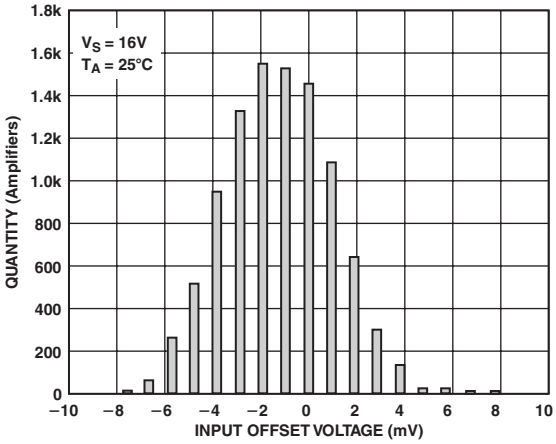
TPC 14. Closed-Loop Output Impedance vs. Frequency



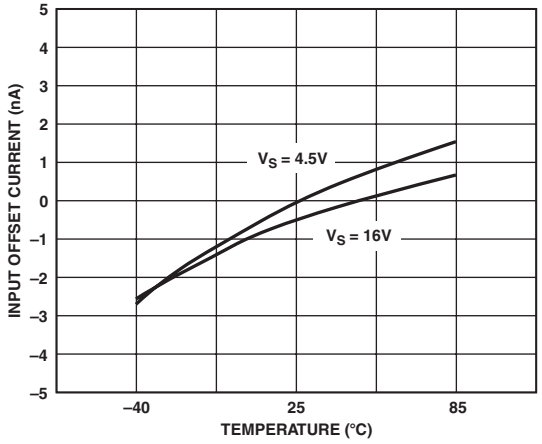
TPC 17. No Phase Reversal



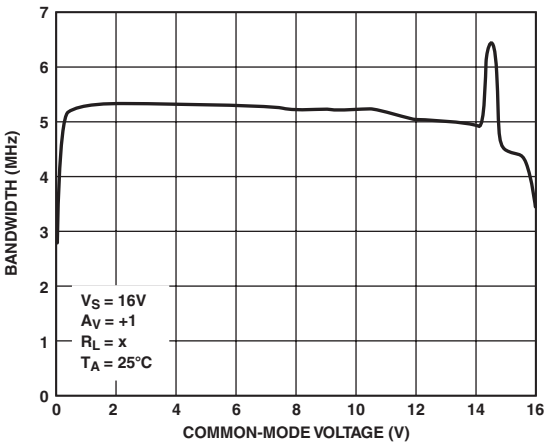
TPC 15. Common-Mode Rejection Ratio vs. Frequency



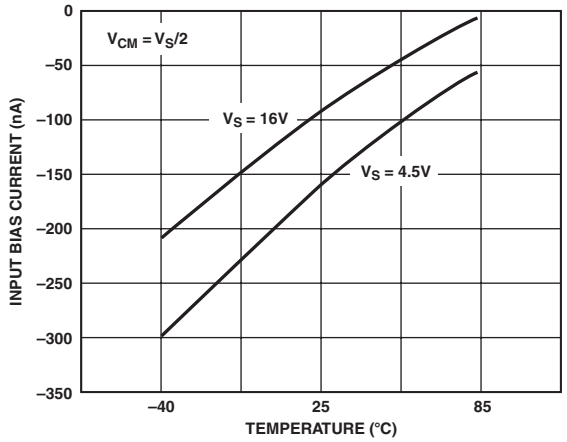
TPC 18. Input Offset Voltage Distribution



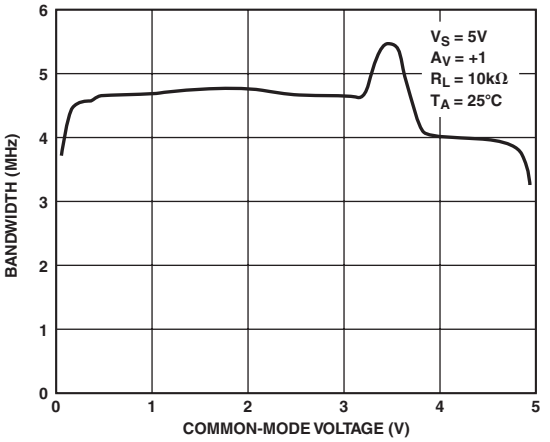
TPC 19. Input Offset Current vs. Temperature



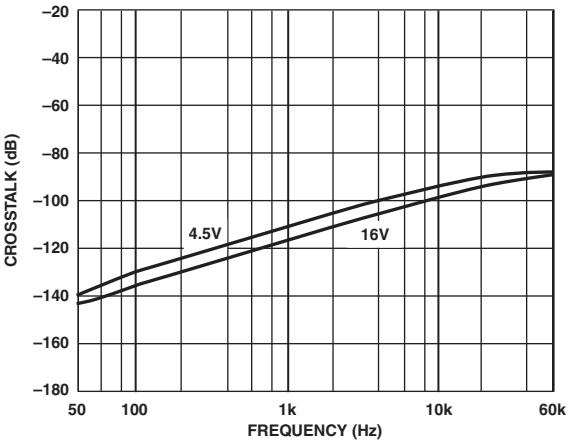
TPC 22. Frequency vs. Common-Mode Voltage (V_S = 16 V)



TPC 20. Input Bias Current vs. Temperature



TPC 23. Frequency vs. Common-Mode Voltage (V_S = 5.0 V)



TPC 21. Channel A vs. Channel B Crosstalk

APPLICATIONS

Theory of Operation

The AD856x family is designed to drive large capacitive loads in LCD applications. It has high output current drive, rail-to-rail input/output operation, and is powered from a single 16 V supply. It is also intended for other applications where low distortion and high output current drive are needed.

Figure 1 illustrates a simplified equivalent circuit for the AD856x. The rail-to-rail bipolar input stage is composed of two PNP differential pairs, Q4 to Q5 and Q10 to Q11, operating in series with diode protection networks, D1 to D2. Diode network D1 to D2 serves as protection against large transients for Q4 to Q5 to accommodate rail-to-rail input swing. D5 to D6 protect Q10 to Q11 against Zenering. In normal operation, Q10 to Q11 are off and their input stage is buffered from the operational amplifier inputs by Q6 to D3 and Q8 to D4. Operation of the input stage is best understood as a function of applied common-mode voltage: when the inputs of the AD856x are biased midway between the supplies, the differential signal path gain is controlled by resistive loads (via R9, R10) Q4 to Q5. As the input common-mode level is reduced toward the negative supply (V_{NEG} or GND), the input transistor current sources, I1 and I2, are forced into saturation, thereby forcing the Q6 to D3 and Q8 to D4 networks into cutoff. However, Q4 to Q5 remain active, providing input stage gain. Inversely, when common-mode input voltage is increased toward the positive supply, Q4 to Q5 are driven into cutoff, Q3 is driven into saturation, and Q4 becomes active, providing bias to the Q10 to Q11 differential pair. The point at which Q10 to Q11 differential pair becomes active is approximately equal to (V_{POS} – 1 V).

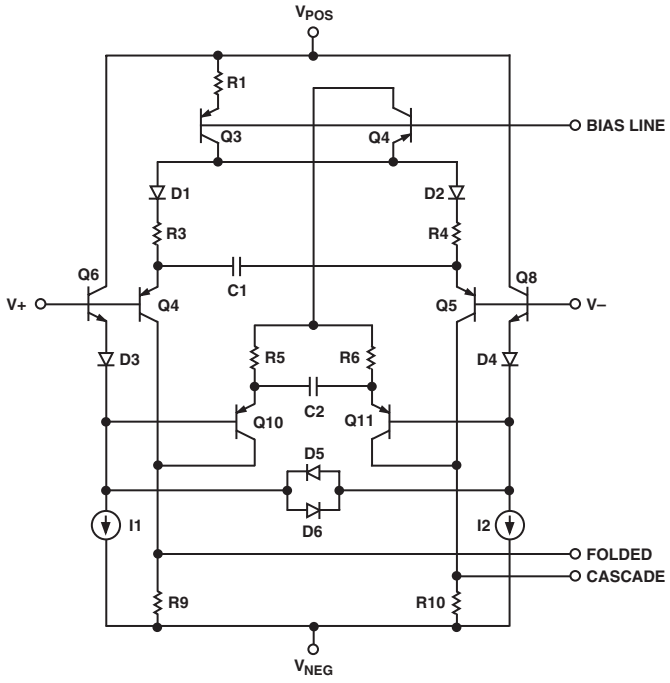


Figure 1. AD856x Equivalent Input Circuit

The benefit of this type of input stage is low bias current. The input bias current is the sum of base currents of Q4 to Q5 and Q6 to Q8 over the range from (V_{NEG} + 1 V) to (V_{POS} – 1 V). Outside of this range, input bias current is dominated by the sum of base currents of Q10 to Q11 for input signals close to V_{NEG} and of Q6 to Q8 (Q10 to Q11) for signals close to V_{POS}. From this type of design, the input bias current of AD856x not only exhibits different amplitude but also exhibits different polarities. Figure 2 provides the characteristics of the input bias current versus the common-mode voltage. It is important to keep in mind that the source impedances driving the AD856x inputs are balanced for optimum dc and ac performance.

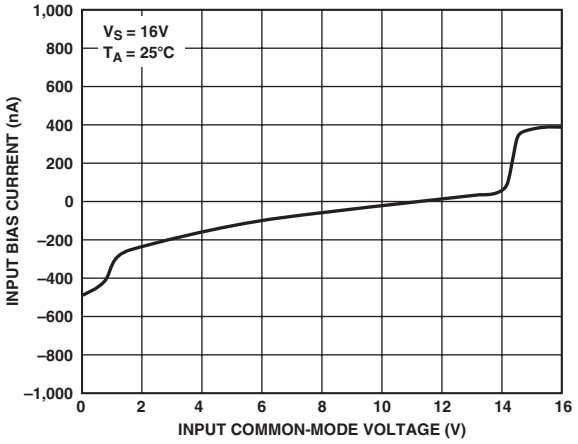


Figure 2. AD856x Input Bias Current vs. Common-Mode Voltage

In order to achieve rail-to-rail output performance, the AD856x design uses a complementary common-source (or gmRL) output. This configuration allows output voltages to approach the power supply rails, particularly if the output transistors are allowed to enter the triode region on extremes of signal swing, which are limited by V_{GS}, the transistor sizes, and output load current. Also, this type of output stage exhibits voltage gain in an open-loop gain configuration. The amount of gain depends on the total load resistance at the output of the AD856x.

Input Overvoltage Protection

As with any semiconductor device, whenever the input exceeds either supply voltages, attention needs to be paid to the input overvoltage characteristics. As an overvoltage occurs, the amplifier could be damaged, depending on the voltage level and the magnitude of the fault current. When the input voltage exceeds either supply by more than 0.6 V, internal pn junctions allow current to flow from the input to the supplies.

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. If a condition exists using the AD856x where the input exceeds the supply more than 0.6 V, an external series resistor should be added. The size of the resistor can be calculated by using the maximum overvoltage divided by 5 mA. This resistance should be placed in series with either input exposed to an overvoltage.

Output Phase Reversal

The AD856x family is immune to phase reversal. Although the device's output will not change phase, large currents due to input overvoltage could damage the device. In applications where the possibility of an input voltage exceeding the supply voltage exists, overvoltage protection should be used as described in the previous section.

Power Dissipation

The maximum allowable internal junction temperature of 150°C limits the AD856x family's maximum power dissipation of AD856x devices. As the ambient temperature increases, the maximum power dissipated by AD856x devices must decrease linearly to maintain the maximum junction temperature. If this maximum junction temperature is exceeded momentarily, the device will still operate properly once the junction temperature is reduced below 150°C. If the maximum junction temperature is exceeded for an extended period of time, overheating could lead to permanent damage of the device.

The maximum safe junction temperature, T_{JMAX}, is 150°C. Using the following formula, we can obtain the maximum power that an AD856x device can safely dissipate as a function of temperature:

$$P_{DISS} = T_{JMAX} - T_A/\theta_{JA}$$

where:

P_{DISS} = the AD856x power dissipation.
T_{JMAX} = the AD856x maximum allowable junction temperature (150°C).
T_A = the ambient temperature of the circuit.
θ_{JA} = the AD856x package thermal resistance, junction-to-ambient.

The power dissipated by the device can be calculated as

$$P_{DISS} = (V_S - V_{OUT}) \times I_{LOAD}$$

where:

V_S = the supply voltage.
V_{OUT} = the output voltage.
I_{LOAD} = the output load current.

Figure 3 shows the maximum power dissipation versus temperature. To achieve proper operation, use the previous equation to calculate P_{DISS} for a specific package at any given temperature or use the figure below.

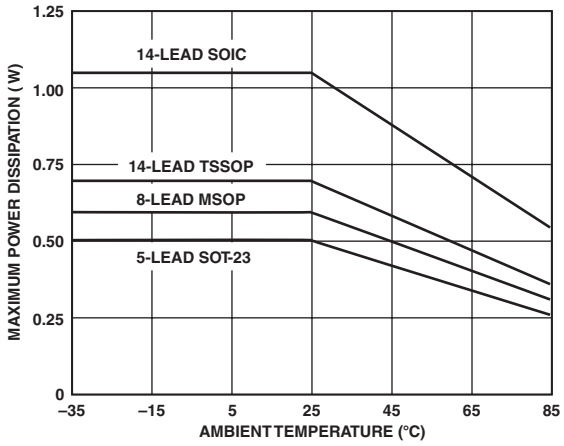


Figure 3. Maximum Power Dissipation vs. Temperature for 5-, 8-, and 14-Lead Packages

Total Harmonic Distortion + Noise (THD+N)

The AD856x family features low total harmonic distortion. Figure 4 shows a graph of THD+N versus frequency. The THD+N for the AD856x over the entire supply range is below 0.008%. When the device is powered from a 16 V supply, the THD+N stays below 0.003%. Figure 4 shows the AD8566 in a unity noninverting configuration.

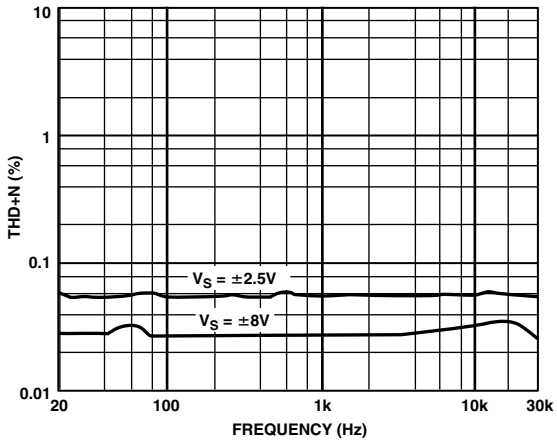


Figure 4. THD+N vs. Frequency Graph

Short-Circuit Output Conditions

The AD856x family does not have internal short-circuit protection circuitry. As a precautionary measure, it is recommended not to short the output directly to the positive power supply or to ground.

It is not recommended to operate the AD856x with more than 35 mA of continuous output current. The output current can be limited by placing a series resistor at the output of the amplifier whose value can be derived using the following equation:

$$R_X \geq \frac{V_S}{35\ \text{mA}}$$

For a 5 V single-supply operation, R_X should have a minimum value of 143 Ω.

LCD Panel Applications

The AD856x amplifier is designed for LCD panel applications or applications where large capacitive load drive is required. It can instantaneously source/sink greater than 250 mA of current. At unity gain, it can drive 1 μF without compensation. This makes the AD856x ideal for LCD V_{COM} driver applications.

To evaluate the performance of the AD856x family, a test circuit was developed to simulate the V_{COM} driver application for an LCD panel.

Figure 5 shows the test circuit. Series capacitors and resistors connected to the output of the op amp represent the load of the LCD panel. The 300 Ω and 3 kΩ feedback resistors are used to improve settling time. This test circuit simulates the worst-case scenario for a V_{COM}. It drives a represented load that is connected to a signal switched symmetrically around V_{COM}. Figure 6 displays a scope photo of the instantaneous output peak current capability of the AD856x family.

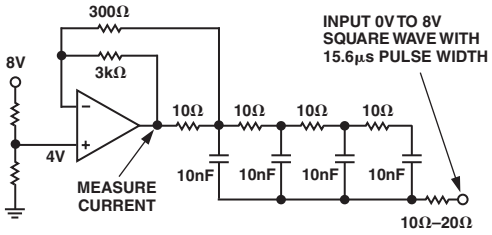


Figure 5. V_{COM} Test Circuit with Supply Voltage at 16 V

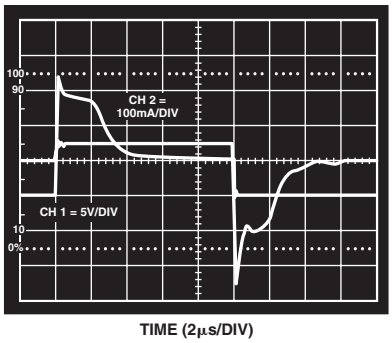
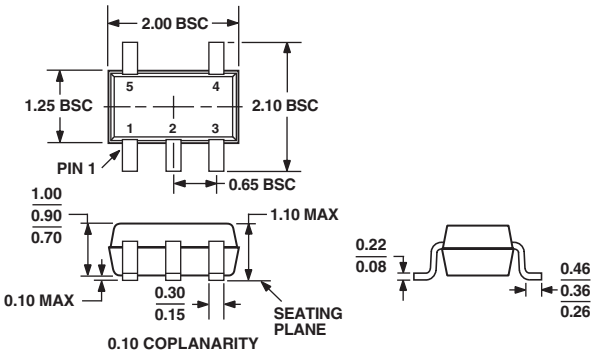


Figure 6. Scope Photo of the V_{COM} Instantaneous Peak Current

OUTLINE DIMENSIONS

5-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-5)

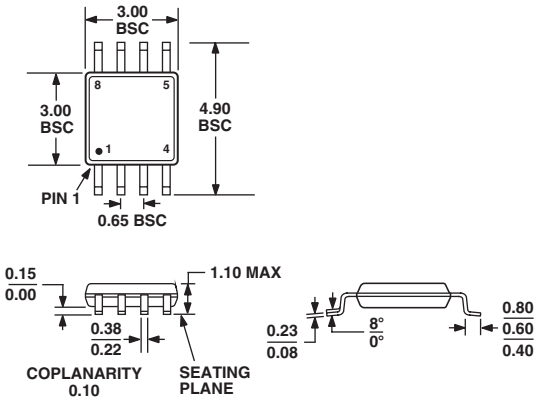
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203AA

8-Lead Micro Small Outline Package [MSOP] (RM-8)

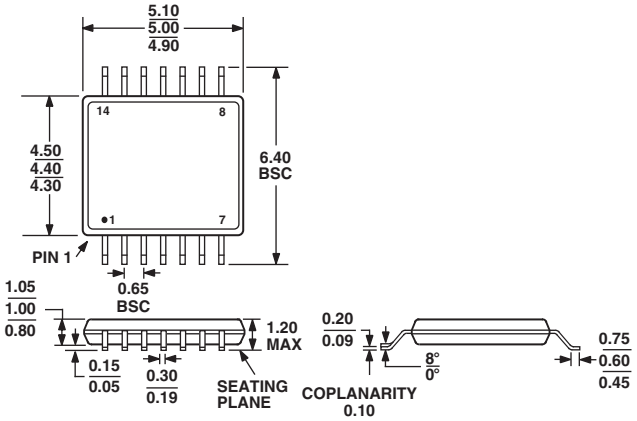
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

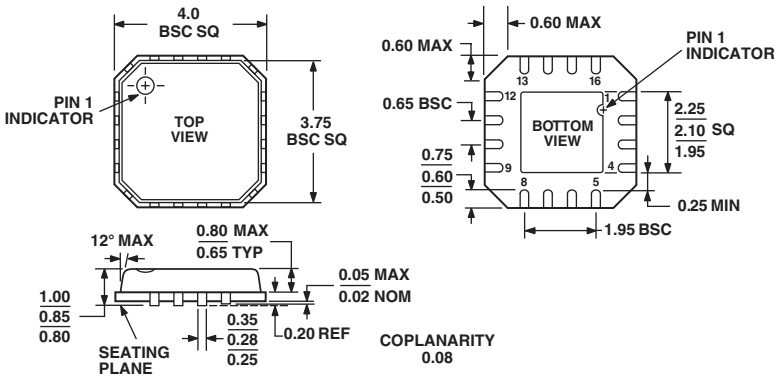
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

OUTLINE DIMENSIONS

16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body
(CP-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

C01909–0–3/04(C)

Revision History

Location	Page
3/04—Data Sheet changed from REV. B to REV. C.	
Changes to SPECIFICATIONS	2
Changes to TPC 4	4
Changes to TPC 10	5
Changes to TPC 14	6
Changes to TPC 20	7
12/03—Data Sheet changed from REV. A to REV. B.	
Updated ORDERING GUIDE	3
Updated OUTLINE DIMENSIONS	11
10/01—Data Sheet changed from REV. 0 to REV. A.	
Edit to 16-Lead CSP and 5-Lead SC70 Pin Configuration	1
Edit to ORDERING GUIDE	3