# AN2546FH-A

## Automotive LCD TV signal processor IC

### ■ Overview

The AN2546FH-A is a video signal processing IC built-in a 5-volt power-supply source driver for TFT color LCD (normally white type), and it supports the NTSC, PAL and PAL-M/PAL-N systems. The main circuitry of this IC includes video-signal processing circuit, color signal processing circuit, interface circuit, synchronizing circuit and many color quality adjusting circuits. This IC converts the composite video signal or separated Y/C signal or RGB signals into RGB signals available for TFT color LCD.

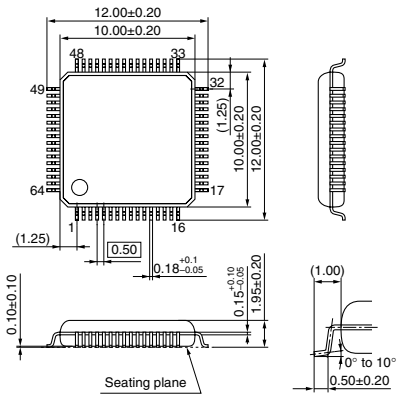
### ■ Features

- Supply voltage: 3 V/5 V/7.5 V
- Built-in a 5-volt power-supply source driver for TFT type LCD
- Low consumption power (typ. 200 mW)
- Supporting the NTSC, PAL, PAL-M and PAL-N
- Supporting composite, component and color differential signal input
- Video signal, analog RGB (2 systems)
  One is for OSD (analog/digital).
- Each mode setting is possible with $I^2C$ Bus control.
- Electronic volume (D/A converter) built in
- Contrast/Brightness/γ correction circuit built in
- Horizontal and vertical display position adjustment are possible by serial control.
- Improvement of weak electric field characteristics (Compared to AN2526FH/AN2526NFH: −5 dB)
- At reverse stop, built-in output gain down function

### ■ Applications

- 4 inches to 7 inches middle size TFT LCD equipment of normally white, of such as an in-car TV and an LCD monitor for car navigation system.

Unit: mm

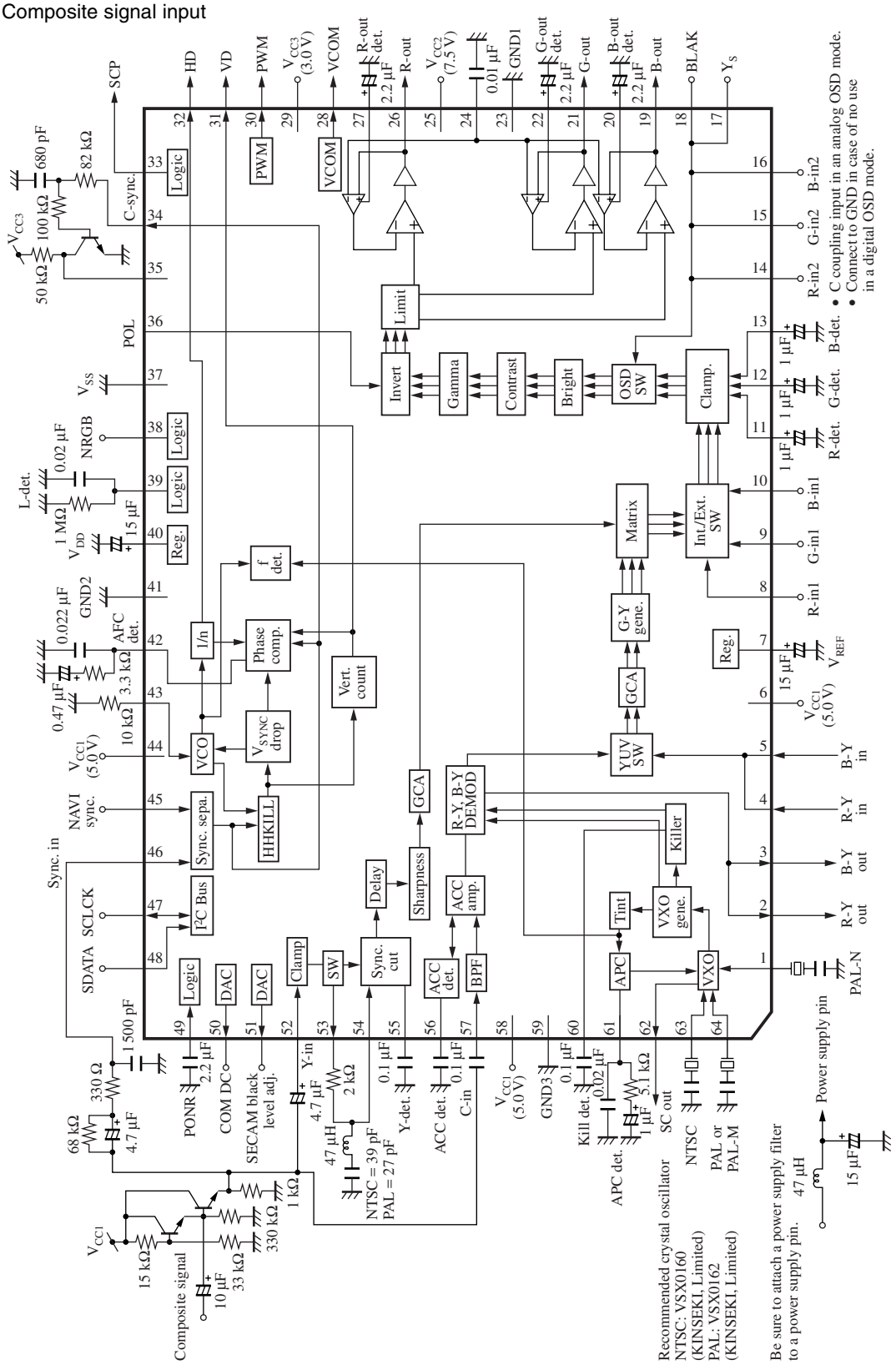



QFP064-P-1010

Note) The package of this product will be changed to lead-free type (QFP064-P-1010A). See the new package dimensions section later of this datasheet.

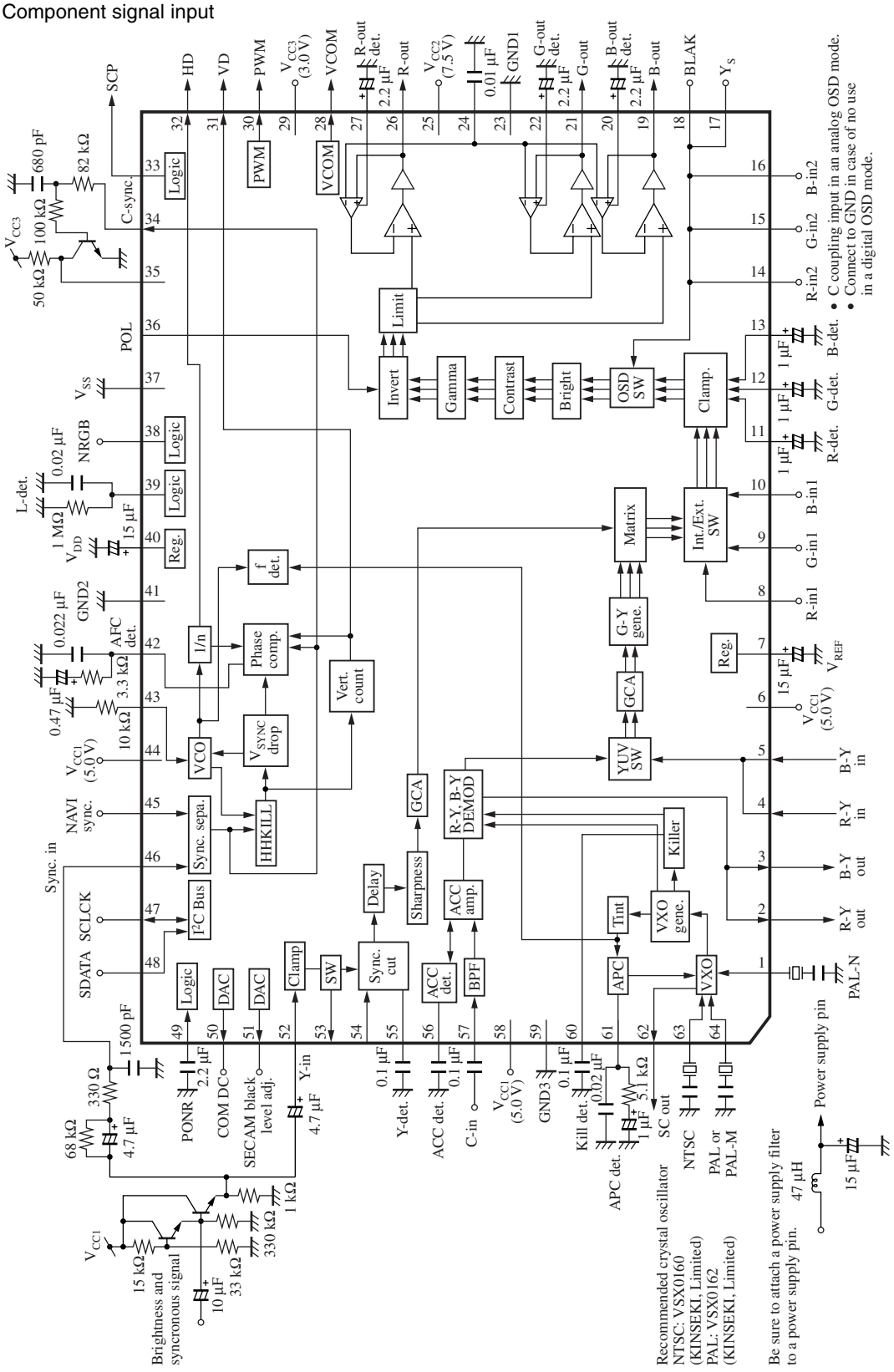
## ■ Application Circuit Examples

1. Composite signal input



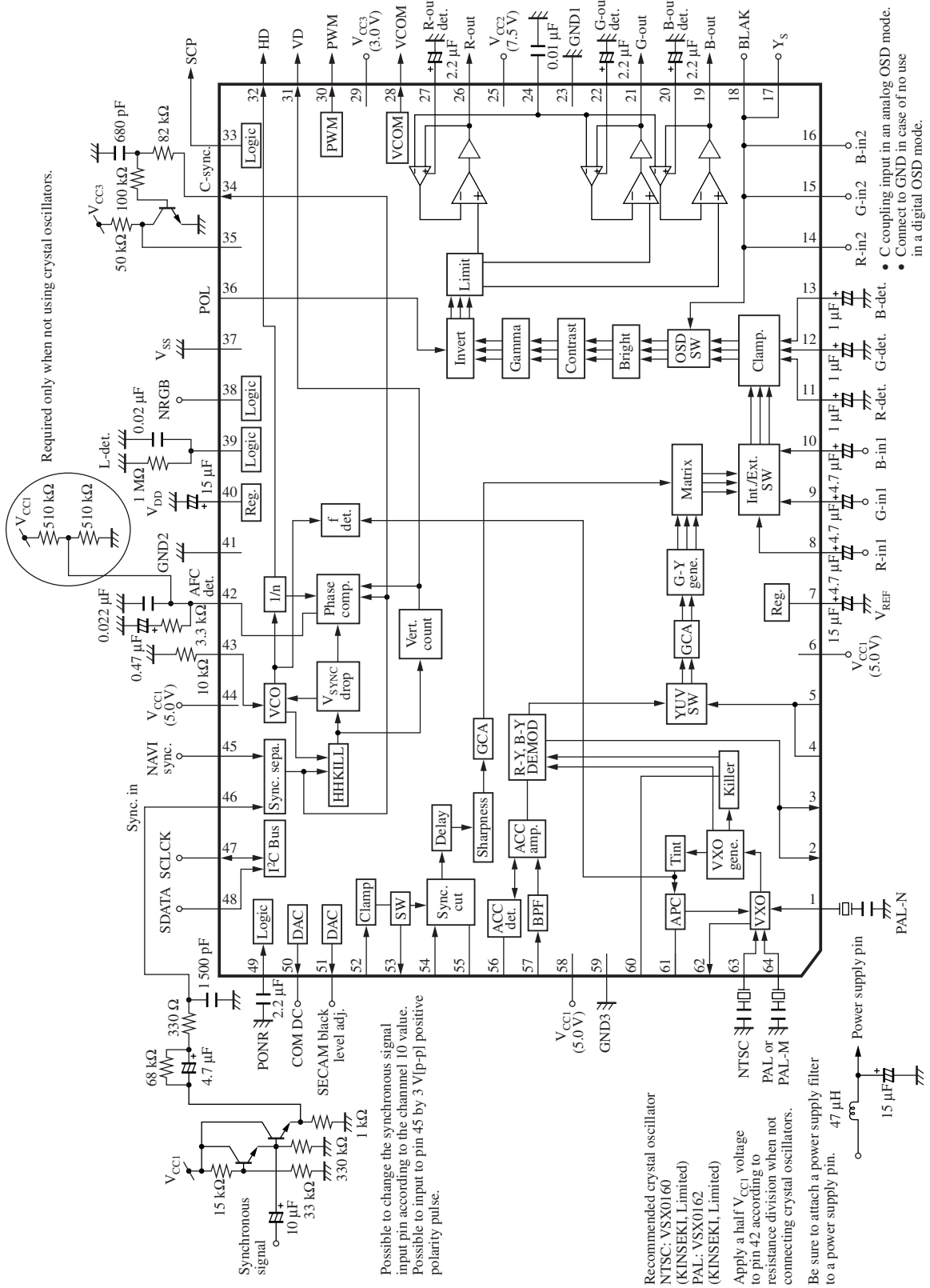
■ Application Circuit Examples (continued)

2. Component signal input



■ Application Circuit Examples (continued)

3. Analog RGB signal input



■ Pin Descriptions

| Pin No. | Description | Pin No. | Description |
|---|---|---|---|
| 1 | Crystal oscillator connecting pin 3 (PAL-N) | 33 | Sand castle pulse output pin |
| 2 | R-Y output pin | 34 | Composite synchronous signal output pin |
| 3 | B-Y output pin | 35 | Vertical synchronous signal input pin |
| 4 | R-Y input pin | 36 | 1H reverse signal input pin |
| 5 | B-Y input pin | 37 | Clock-system GND ($V_{SS}$) |
| 6 | Signal processing system power supply ($V_{CC1}$ = 5.0 V) | 38 | Analog imposing control signal input pin |
| | | 39 | Horizontal clock detection pin |
| 7 | Internal reference power supply detection pin (2.0 V) | 40 | Clock-system power supply (3.0 V) |
| | | 41 | GND 2 |
| 8 | R-ch. analog signal input pin | 42 | AFC loop filter connecting pin |
| 9 | G-ch. analog signal input pin | 43 | VCO frequency adjustment pin |
| 10 | B-ch. analog signal input pin | 44 | Synchronous system power supply ($V_{CC1}$ = 5.0 V) |
| 11 | R-ch. clamp detection pin | | |
| 12 | G-ch. clamp detection pin | 45 | NAVI signal synchronous signal input pin |
| 13 | B-ch. clamp detection pin | 46 | Synchronous signal input pin |
| 14 | R-ch. OSD input pin | 47 | Serial data shift clock input pin |
| 15 | G-ch. OSD input pin | 48 | Serial data input pin |
| 16 | B-ch. OSD input pin | 49 | Power-on reset detection pin |
| 17 | Character picking up pulse input pin | 50 | Common DC adjustment voltage output pin |
| 18 | Side black control signal input pin | 51 | DAC output pin |
| 19 | B-ch. output pin | 52 | Luminance signal input pin |
| 20 | B-ch. output DC feedback detection pin | 53 | Chrominance signal trap filter connection pin 1 |
| 21 | G-ch. output pin | 54 | Chrominance signal trap filter connection pin 2 |
| 22 | G-ch. output DC feedback detection pin | 55 | Y-system clamp detection pin |
| 23 | GND 1 | 56 | ACC detection pin |
| 24 | Drive output reference voltage input pin | 57 | Chrominance signal input pin |
| 25 | Drive system power supply ($V_{CC2}$ = 7.5 V) | 58 | Chrominance processing system power supply ($V_{CC1}$ = 5.0 V) |
| 26 | R-ch. output pin | | |
| 27 | R-ch. output DC feedback detection pin | 59 | GND 3 |
| 28 | Common reverse signal output pin | 60 | Chrominance killer detection pin |
| 29 | Pulse output system power supply ($V_{CC3}$ = 3.0 V) | 61 | APC detection pin |
| | | 62 | Subcarrier output pin |
| 30 | PWM output pin | 63 | Crystal oscillator connecting pin 1 (NTSC) |
| 31 | Vertical synchronous signal output pin | 64 | Crystal oscillator connecting pin 2 (PAL/PAL-M) |
| 32 | Horizontal synchronous signal output pin | | |

## ■ Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC1}$ | 5.5 | V |
| | $V_{CC2}$ | 8.5 | |
| | $V_{CC3}$ | 5.2 | |
| Supply current | $I_{CC}$ | — | mA |
| Power dissipation *2 | $P_D$ | 423 | mW |
| Operating ambient temperature *1 | $T_{opr}$ | −30 to +85 | °C |
| Storage temperature *1 | $T_{stg}$ | −55 to +150 | °C |

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for $T_a$ = 25°C.
∗2: The power dissipation shown is the value in free air for $T_{opr}$ = 85°C.

## ■ Recommended Operating Range

| Parameter | Symbol | Range | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC1}$ | 4.7 to 5.3 | V |
| | $V_{CC2}$ | 7.0 to 8.0 | |
| | $V_{CC3}$ | 2.7 to 3.3 | |

## ■ Electrical Characteristics at $T_a$ = 25°C

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC | | | | | | |
| $V_{CC1}$-system current consumption | $I_{TOTAL1}$ | Refer to product standards | 32 | — | 44 | mA |
| $V_{CC2}$-system current consumption | $I_{TOTAL2}$ | Refer to product standards | 1.0 | — | 9.0 | mA |
| $V_{CC3}$-system current consumption | $I_{TOTAL3}$ | Refer to product standards | — | — | 2.0 | mA |
| Chrominance system | | | | | | |
| R-Y standard gain | $G_{RY}$ | Refer to product standards | 9.0 | — | 15 | dB |
| R-Y/G-Y relative gain | $G_{RYGY}$ | Refer to product standards | −5.0 | — | −1.0 | dB |
| B-Y standard gain | $G_{BY}$ | Refer to product standards | 9.0 | — | 15 | dB |
| B-Y/G-Y relative gain | $G_{BYGY}$ | Refer to product standards | −15 | — | −9.0 | dB |
| High-level APC pull-in | $AP_H$ | Refer to product standards | 500 | — | 540 | Hz |
| Low-level APC pull-in | $AP_L$ | Refer to product standards | −540 | — | −500 | Hz |
| ACC output characteristic 1 | $G_{ACC1}$ | Refer to product standards | −1.0 | — | 1.0 | dB |
| ACC output characteristic 2 | $G_{ACC2}$ | Refer to product standards | −1.0 | — | 1.0 | dB |
| Chrominance killer characteristic 1 | $V_{KILL1}$ | Refer to product standards | 400 | — | — | mV[p-p] |
| Chrominance killer characteristic 2 | $V_{KILL2}$ | Refer to product standards | — | — | 600 | mV[p-p] |
| Subcarrier amplitude | SCV | Refer to product standards | 400 | — | — | mV[p-p] |
| Y-system | | | | | | |
| Sharpness control characteristic | $G_{SH}$ | Refer to product standards | 1.0 | — | — | dB |
| Sharpness frequency characteristic 1 | $f_{SH1}$ | Refer to product standards | 4.0 | — | — | dB |
| R-ch. contrast adjustment range 1 | $CTR_{R1}$ | Refer to product standards | 1.5 | — | — | dB |

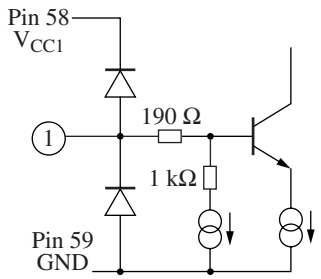
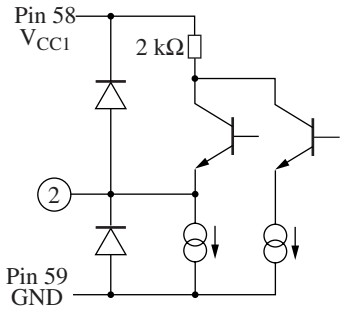
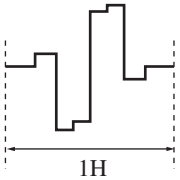
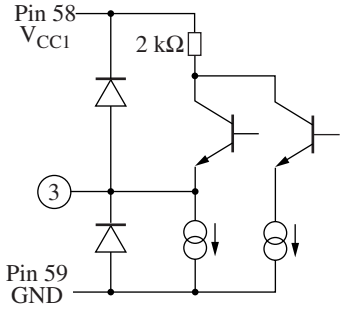
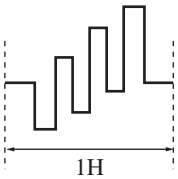
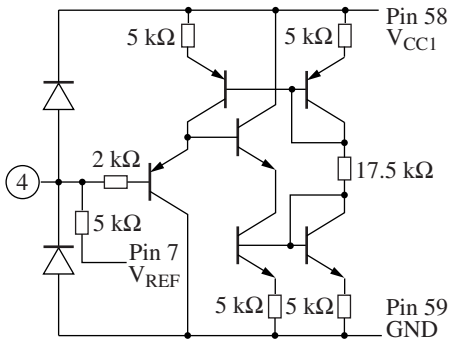
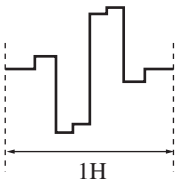
■ Electrical Characteristics at $T_a$ = 25°C (continued)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Y-system (continued) | | | | | | |
| G-ch. contrast adjustment range 1 | $CTR_{G1}$ | Refer to product standards | 1.5 | — | — | dB |
| B-ch. contrast adjustment range 1 | $CTR_{B1}$ | Refer to product standards | 1.5 | — | — | dB |
| R-ch. contrast adjustment range 2 | $CTR_{R2}$ | Refer to product standards | — | — | –2.5 | dB |
| G-ch. contrast adjustment range 2 | $CTR_{G2}$ | Refer to product standards | — | — | –2.5 | dB |
| B-ch. contrast adjustment range 2 | $CTR_{B2}$ | Refer to product standards | — | — | –2.5 | dB |
| R-ch. pedestal amplitude minimum | $V_{PEDRmin}$ | Refer to product standards | — | — | 2.0 | V[p-p] |
| G-ch. pedestal amplitude minimum | $V_{PEDGmin}$ | Refer to product standards | — | — | 2.0 | V[p-p] |
| B-ch. pedestal amplitude minimum | $V_{PEDBmin}$ | Refer to product standards | — | — | 2.0 | V[p-p] |
| R-ch. pedestal amplitude maximum | $V_{PEDRmax}$ | Refer to product standards | 3.0 | — | — | V[p-p] |
| G-ch. pedestal amplitude maximum | $V_{PEDGmax}$ | Refer to product standards | 3.0 | — | — | V[p-p] |
| B-ch. pedestal amplitude maximum | $V_{PEDBmax}$ | Refer to product standards | 3.0 | — | — | V[p-p] |
| G-ch. output DC voltage | $V_{GDC}$ | Refer to product standards | 2.35 | — | 2.85 | V[p-p] |
| R-ch. gamma characteristic 1 | $G_{GAMR1}$ | Refer to product standards | –9.0 | — | –3.0 | dB |
| G-ch. gamma characteristic 1 | $G_{GAMG1}$ | Refer to product standards | –9.0 | — | –3.0 | dB |
| B-ch. gamma characteristic 1 | $G_{GAMB1}$ | Refer to product standards | –9.0 | — | –3.0 | dB |
| R-ch. gamma characteristic 2 | $G_{GAMR2}$ | Refer to product standards | –8.0 | — | — | dB |
| G-ch. gamma characteristic 2 | $G_{GAMG2}$ | Refer to product standards | –8.0 | — | — | dB |
| B-ch. gamma characteristic 2 | $G_{GAMB2}$ | Refer to product standards | –8.0 | — | — | dB |
| R-ch. gamma characteristic 3 | $G_{GAMR3}$ | Refer to product standards | –5.0 | — | 0 | dB |
| G-ch. gamma characteristic 3 | $G_{GAMG3}$ | Refer to product standards | –5.0 | — | 0 | dB |
| B-ch. gamma characteristic 3 | $G_{GAMB3}$ | Refer to product standards | –5.0 | — | 0 | dB |
| R-ch. white limiter high-level | $V_{WRRH}$ | Refer to product standards | — | — | 3.0 | V[p-p] |
| G-ch. white limiter high-level | $V_{WRGH}$ | Refer to product standards | — | — | 3.0 | V[p-p] |
| B-ch. white limiter high-level | $V_{WRBH}$ | Refer to product standards | — | — | 3.0 | V[p-p] |
| R-ch. white limiter low-level | $V_{WRRL}$ | Refer to product standards | 3.2 | — | — | V[p-p] |
| G-ch. white limiter low-level | $V_{WRGL}$ | Refer to product standards | 3.2 | — | — | V[p-p] |
| B-ch. white limiter low-level | $V_{WRBL}$ | Refer to product standards | 3.2 | — | — | V[p-p] |
| R-ch. black limiter low-level | $V_{BRRL}$ | Refer to product standards | 3.0 | — | — | V |
| G-ch. black limiter low-level | $V_{BRGL}$ | Refer to product standards | 3.0 | — | — | V |
| B-ch. black limiter low-level | $V_{BRBL}$ | Refer to product standards | 3.0 | — | — | V |
| R-ch. black limiter high-level | $V_{BRRH}$ | Refer to product standards | — | — | 2.7 | V |
| G-ch. black limiter high-level | $V_{BRGH}$ | Refer to product standards | — | — | 2.7 | V |
| B-ch. black limiter high-level | $V_{BRBH}$ | Refer to product standards | — | — | 2.7 | V |
| R-ch. $Y_S$ threshold 1 | $V_{tYSR1}$ | Refer to product standards | 0.8 | — | — | V[p-p] |
| G-ch. $Y_S$ threshold 1 | $V_{tYSG1}$ | Refer to product standards | 0.8 | — | — | V[p-p] |
| B-ch. $Y_S$ threshold 1 | $V_{tYSB1}$ | Refer to product standards | 0.8 | — | — | V[p-p] |

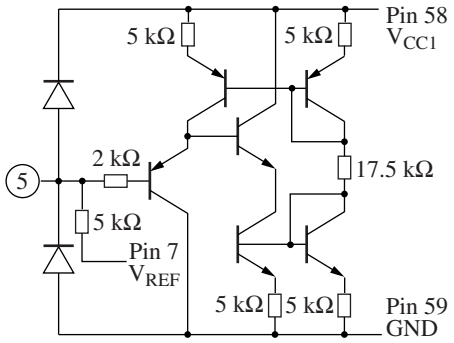
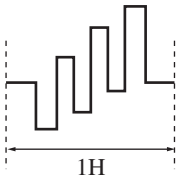
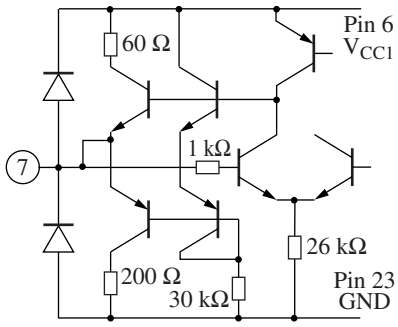
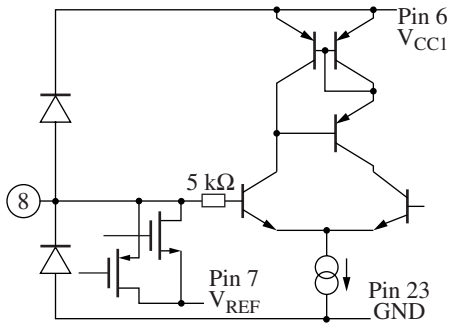
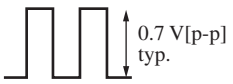
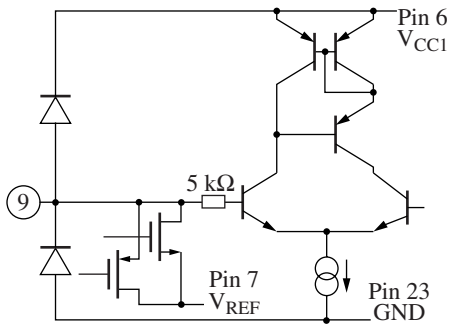
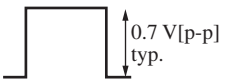
■ Electrical Characteristics at $T_a$ = 25°C (continued)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Y-system (continued) | | | | | | |
| R-ch. $Y_S$ threshold 2 | $V_{tYSR2}$ | Refer to product standards | — | — | 0.5 | V[p-p] |
| G-ch. $Y_S$ threshold 2 | $V_{tYSG2}$ | Refer to product standards | — | — | 0.5 | V[p-p] |
| B-ch. $Y_S$ threshold 2 | $V_{tYSB2}$ | Refer to product standards | — | — | 0.5 | V[p-p] |
| R-ch. black level | $CHR_{RB}$ | Refer to product standards | −1.0 | — | 1.0 | V |
| G-ch. black level | $CHR_{GB}$ | Refer to product standards | −1.0 | — | 1.0 | V |
| B-ch. black level | $CHR_{BB}$ | Refer to product standards | −1.0 | — | 1.0 | V |
| R-ch. black level width | $WCHR_{RB}$ | Refer to product standards | 2.0 | — | 4.0 | µs |
| G-ch. black level width | $WCHR_{GB}$ | Refer to product standards | 2.0 | — | 4.0 | µs |
| B-ch. black level width | $WCHR_{BB}$ | Refer to product standards | 2.0 | — | 4.0 | µs |
| R-ch. CHR threshold 1 | $V_{tCHR1}$ | Refer to product standards | 1.5 | — | — | V[p-p] |
| G-ch. CHR threshold 1 | $V_{tCHG1}$ | Refer to product standards | 1.5 | — | — | V[p-p] |
| B-ch. CHR threshold 1 | $V_{tCHB1}$ | Refer to product standards | 1.5 | — | — | V[p-p] |
| R-ch. CHR threshold 2 | $V_{tCHR2}$ | Refer to product standards | 3.0 | — | — | V[p-p] |
| G-ch. CHR threshold 2 | $V_{tCHG2}$ | Refer to product standards | 3.0 | — | — | V[p-p] |
| B-ch. CHR threshold 2 | $V_{tCHB2}$ | Refer to product standards | 3.0 | — | — | V[p-p] |
| R-ch. white level | $CHR_{RW}$ | Refer to product standards | 2.0 | — | — | V[p-p] |
| G-ch. white level | $CHR_{GW}$ | Refer to product standards | 2.0 | — | — | V[p-p] |
| B-ch. white level | $CHR_{BW}$ | Refer to product standards | 2.0 | — | — | V[p-p] |
| R-ch. white level width | $WCHR_{RW}$ | Refer to product standards | 2.0 | — | 4.0 | µs |
| G-ch. white level width | $WCHR_{GW}$ | Refer to product standards | 2.0 | — | 4.0 | µs |
| B-ch. white level width | $WCHR_{BW}$ | Refer to product standards | 2.0 | — | 4.0 | µs |
| R-ch. RGB2 relative amplitude | $V_{RGB2R}$ | Refer to product standards | – 0.45 | — | 0.45 | V[p-p] |
| B-ch. RGB2 relative amplitude | $V_{RGB2B}$ | Refer to product standards | – 0.45 | — | 0.45 | V[p-p] |
| Synchronous system | | | | | | |
| Horizontal sync. pulse low-level | $V_{HDL}$ | Refer to product standards | — | — | 0.4 | V |
| Horizontal sync. pulse amplitude | $V_{HD}$ | Refer to product standards | 2.4 | — | — | V[p-p] |
| Horizontal sync. pulse width | $t_{HD}$ | Refer to product standards | 3.6 | — | 6.0 | µs |
| Vertical sync. pulse low-level | $V_{VDL}$ | Refer to product standards | — | — | 0.4 | V |
| Vertical sync. pulse amplitude | $V_{VD}$ | Refer to product standards | 2.4 | — | — | V[p-p] |
| Horizontal sync. separation pulse high-level | $V_{HSSH}$ | SG2 (NTSC) | 2.4 | — | — | V |
| Horizontal sync. separation pulse amplitude | $V_{HSS}$ | SG2 (NTSC) | 2.4 | — | — | V[p-p] |
| Horizontal sync. separation pulse width | $t_{HSS}$ | SG2 (NTSC) | 3.6 | — | 6.0 | µs |

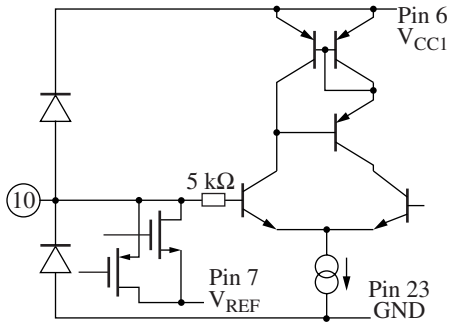
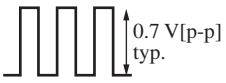
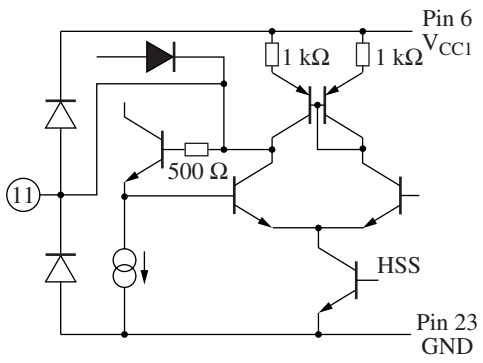
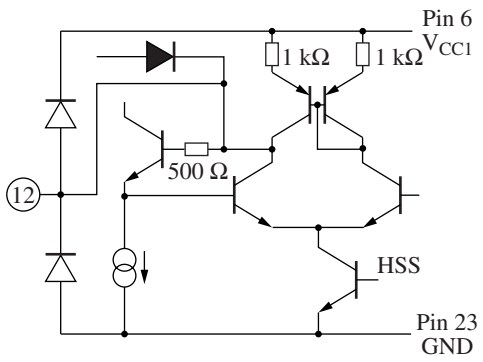
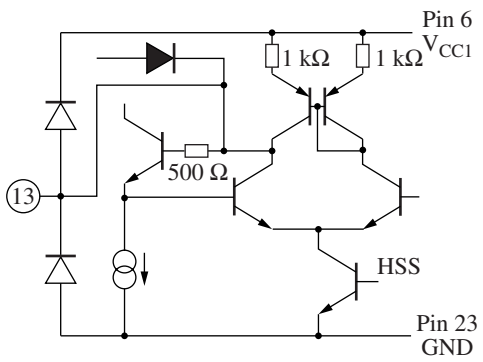
■ Terminal Equivalent Circuits

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 1 |  | VXO3:<br>PAL-N crystal oscillator connecting pin<br>Use the capacitor with temperature characteristics (N750) to connect to the crystal oscillator. | — |
| 2 |  | R-Y out:<br>Output pin of R-Y signal demodulated from video signal | R-Y signal<br>  |
| 3 |  | B-Y out:<br>Output pin of B-Y signal demodulated from video signal | B-Y signal<br>  |
| 4 |  | R-Y in:<br>R-Y signal input pin in a color difference mode and in the standard PAL | R-Y signal<br>  |

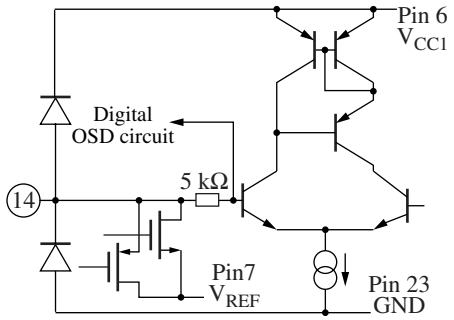
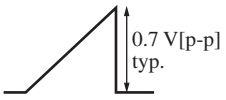
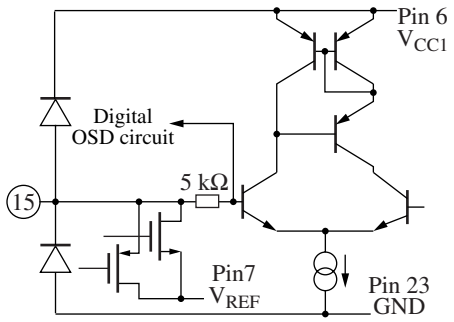
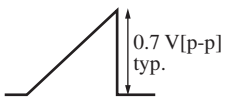
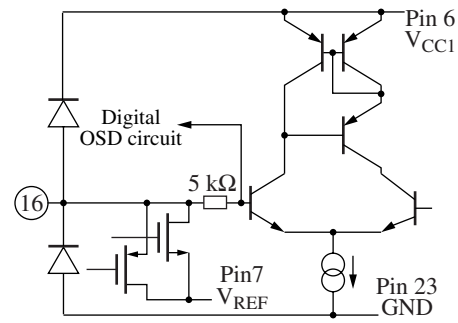
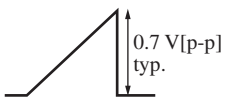
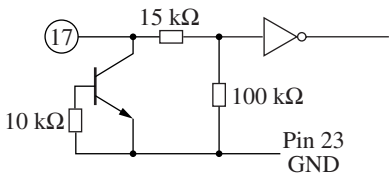
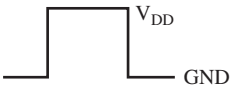
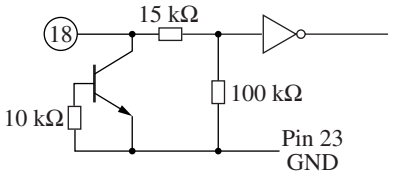
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 5 |  | B-Y in:<br>B-Y signal input pin in a color difference mode and in the standard PAL | B-Y signal<br>  |
| 6 | | $V_{CC1}$:<br>Drive block 5.0 V-system power supply pin | — |
| 7 |  | $V_{REF}$:<br>Reference voltage output pin<br>2.0 V typ. | — |
| 8 |  | R-in 1:<br>Analog R signal input | Analog R signal<br>  |
| 9 |  | G-in 1:<br>Analog G signal input | Analog G signal<br>  |

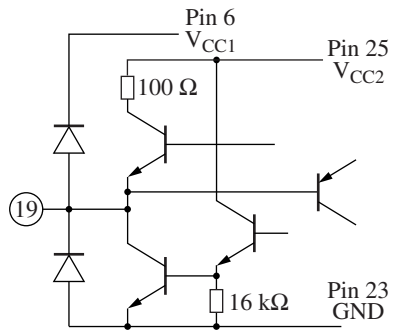
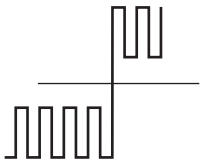
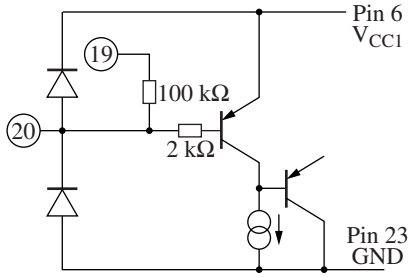
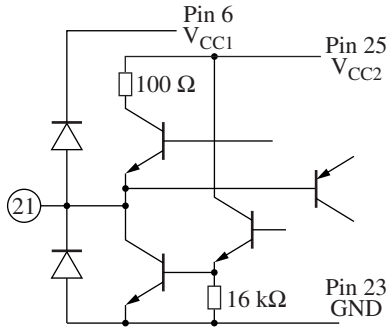
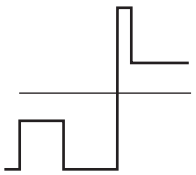
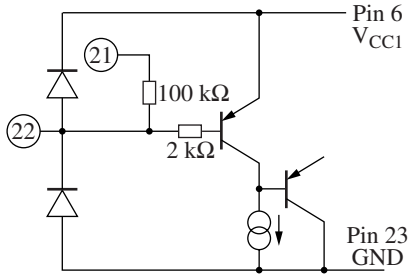
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 10 |  | B-in 1:<br>Analog B signal input | Analog B signal<br>  |
| 11 |  | R-ch. det.:<br>R-ch. clamping capacitor coupling pin | — |
| 12 |  | G-ch. det.:<br>G-ch. clamping capacitor coupling pin | — |
| 13 |  | B-ch. det.:<br>B-ch. clamping capacitor coupling pin | — |

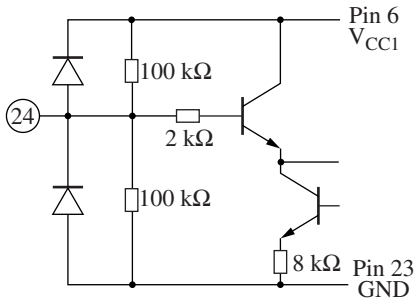
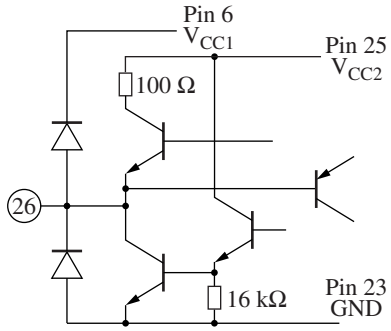
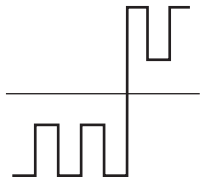
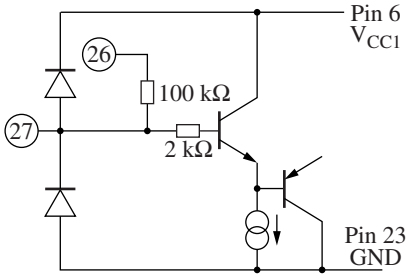
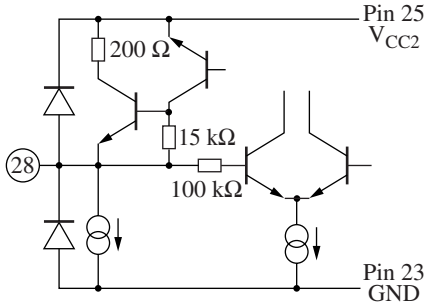
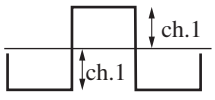
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 14 |  | R-in 2:<br>Character insertion signal input for R-ch., supporting analog and digital OSD | Analog OSD<br>  <br>Digital OSD<br>  |
| 15 |  | G-in 2:<br>Character insertion signal input for G-ch., supporting analog and digital OSD | Analog OSD<br>  <br>Digital OSD<br>  |
| 16 |  | B-in 2:<br>Character insertion signal input for B-ch., supporting analog and digital OSD | Analog OSD<br>  <br>Digital OSD<br>  |
| 17 |  | $Y_S$:<br>Character picking up signal input |  |
| 18 |  | BLAK:<br>Black level indication control signal input pin |  |

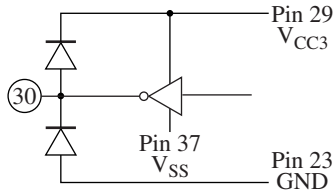
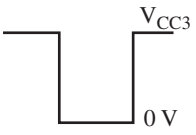
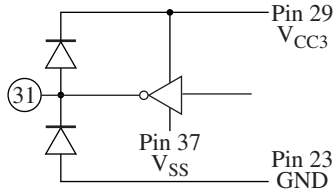
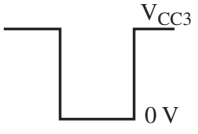
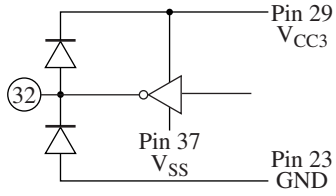
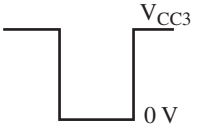
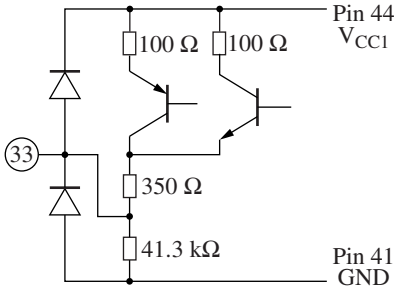
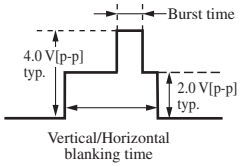
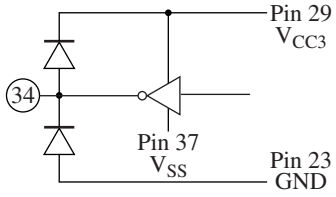
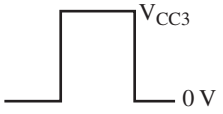
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 19 |  | B-out:<br>B signal output pin |  |
| 20 |  | B-ch. AVE det.:<br>B-ch. output DC feedback detection pin | — |
| 21 |  | G-out:<br>G signal output pin |  |
| 22 |  | G-ch. AVE det.:<br>G-ch. output DC feedback detection pin | — |
| 23 | — | GND 1:<br>Drive circuits system GND | — |

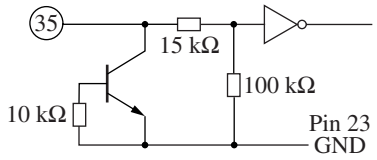
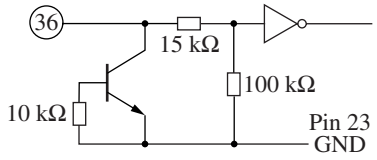
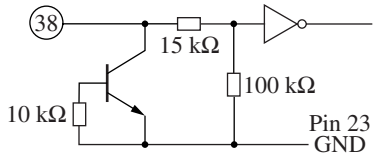
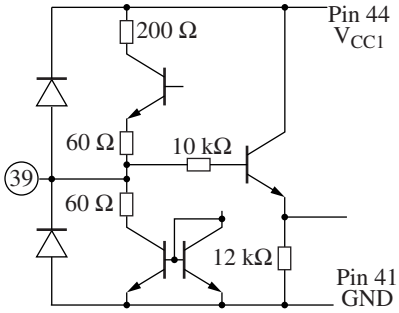
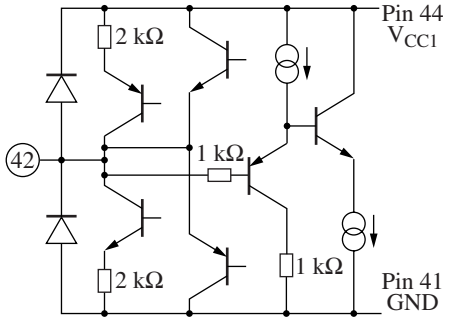
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 24 |  | AVE:<br>R,G,B output DC reference voltage pin | — |
| 25 | — | $V_{CC2}$:<br>7.5 V system power supply | — |
| 26 |  | R-out:<br>R signal output pin |  |
| 27 |  | R-ch. AVE det.:<br>R-ch. output DC feedback detection pin | |
| 28 |  | Common out:<br>Voltage output pin for common.<br>Output impedance; Approx. 150 Ω |  |

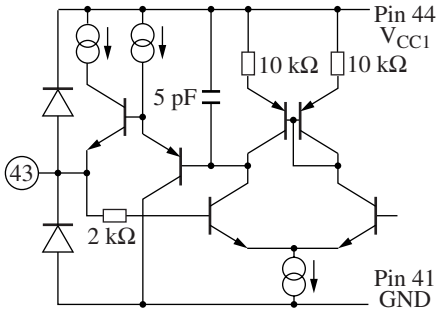
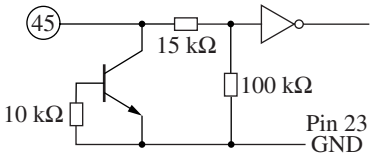
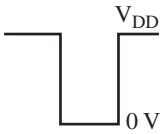
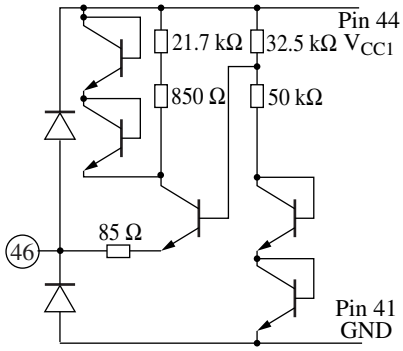
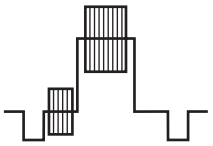
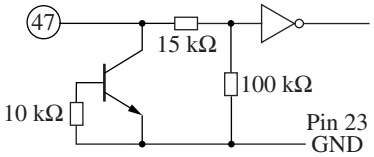
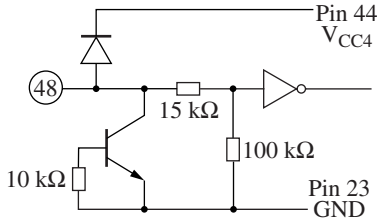
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 29 | — | $V_{CC3}$:<br>Logic output circuits system power supply 3.0 V typ. | — |
| 30 |  | PWM:<br>PWM signal output pin | Output waveform<br>  |
| 31 |  | VD:<br>Vertical synchronous signal output pin | Output waveform<br>  |
| 32 |  | HD:<br>Horizontal synchronous signal output pin | Output waveform<br>  |
| 33 |  | SCP out:<br>Sand castle pulse output pin |  |
| 34 |  | HSS:<br>Composite synchronous signal output pin | Output waveform<br>  |

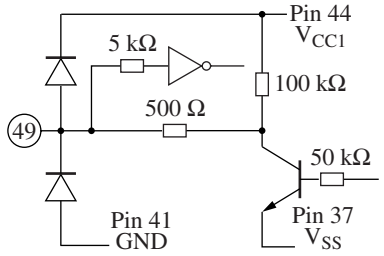
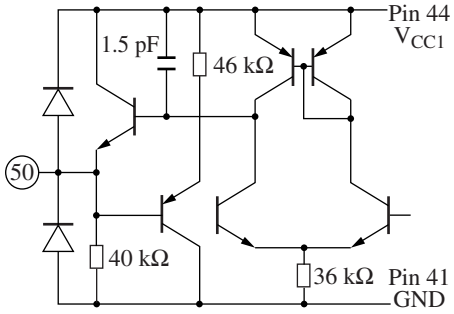
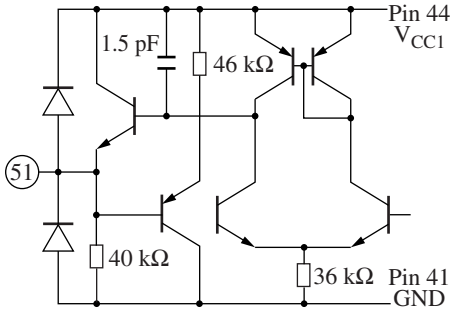
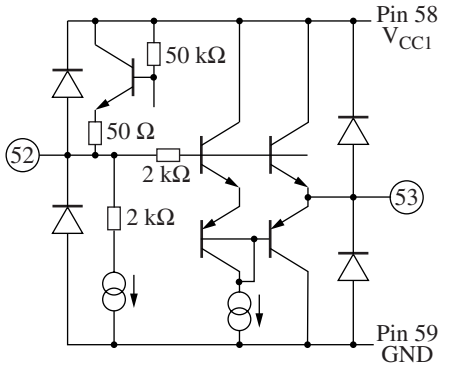
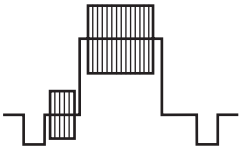
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 35 |  | VDB in:<br>Vertical synchronous pulse input pin | High or Low |
| 36 |  | Ext. pol.:<br>1H reverse signal input pin | High or Low |
| 37 | — | $V_{SS}$ : MOS system GND | — |
| 38 |  | PRGB:<br>Analog OSD signal input<br>Mode start-up signal input pin<br>Valid only in the analog OSD mode<br>High = Analog OSD start up | High or Low |
| 39 |  | LDET:<br>Capacitor coupling pin for the horizontal unlock detecting circuit | — |
| 40 | — | $V_{DD}$:<br>Capacitor connection pin for MOS part power supply<br>3.0 V typ. | — |
| 41 | — | GND 2: Pulse system GND | — |
| 42 |  | AFC det.:<br>AFC filter connecting pin<br>Input impedance; 100 kΩ or more |  |

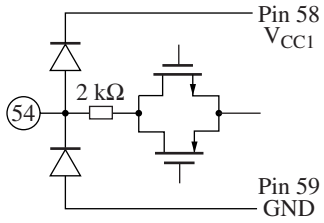
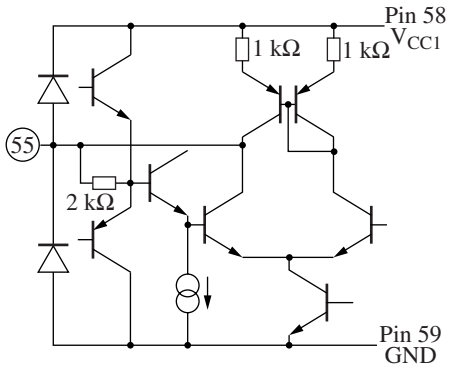
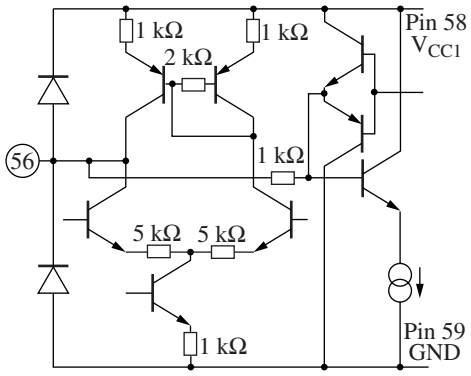
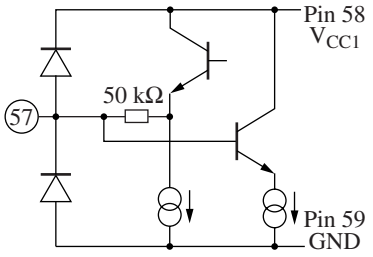
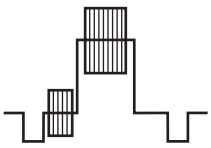
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 43 |  | H $f_O$:<br>VCO oscillation frequency adjusting resistor connection pin | — |
| 44 | — | $V_{CC1}$:<br>Pulse system power supply<br>5.0 V | — |
| 45 |  | NAVI sync-in:<br>Synchronous signal input pin for the signal of car navigation system<br>Negative polarity input |  |
| 46 |  | HSS in:<br>Sync. signal input pin<br>Separates a sync. signal from luminance signal (video signal) | Input signal example:<br>Video signal<br>  |
| 47 |  | SCLK:<br>Serial clock input pin |  |
| 48 |  | DAT:<br>Serial data input pin |  |

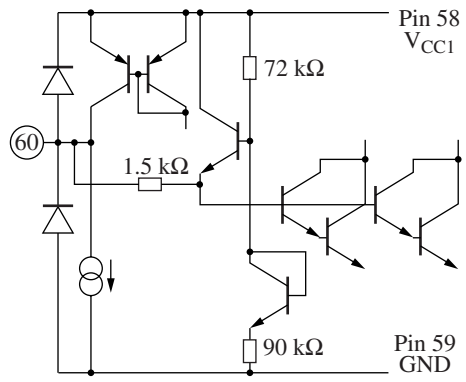
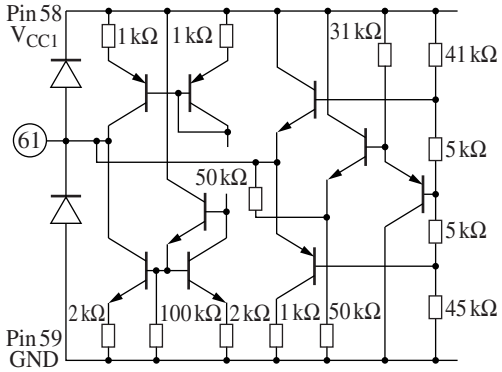
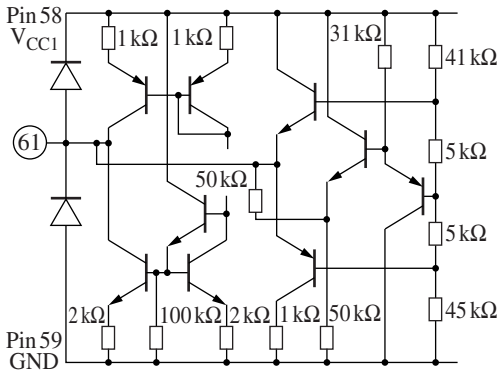
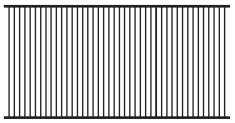
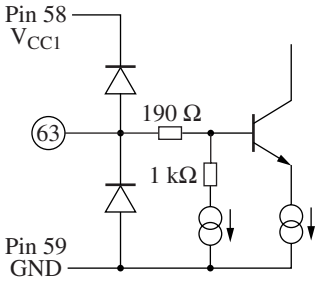
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 49 |  | RST:<br>Capacitor coupling pin for power-on reset | — |
| 50 |  | Com. DC:<br>DC voltage output pin | DC |
| 51 |  | DAC-out:<br>DC voltage output pin | DC |
| 52 |  | Y-in:<br>Luminance signal input pin<br>Input luminance signal (video signal) | Input signal example:<br>Video signal<br>  |
| 53 | | Trap-out:<br>Trap connecting pin<br>Trapping a chrominance signal by connecting external inductor and capacitor. Not necessary in case that an input signal is a component. | — |

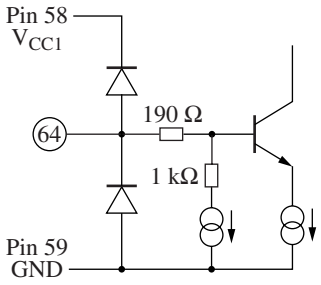
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 54 |  | Trap-in:<br>Trap connecting pin<br>The pair with pin 53 | — |
| 55 |  | Y-det.:<br>Capacitor coupling pin for luminance signal clamping | — |
| 56 |  | ACC det.:<br>ACC capacitor connecting pin, adjusting the amplitude of a burst signal automatically | — |
| 57 |  | C-in:<br>Chrominance signal input pin<br>Input chrominance signal (video signal) | Input signal example:<br>Video signal<br>  |
| 58 | — | $V_{CC1}$:<br>Power supply 5.0 V typ.<br>Chrominance and luminance signal processing system. | — |
| 59 | — | GND 3:<br>GND for chrominance and luminance signal processing system | — |

■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 60 |  | Kill det.:<br>Killer capacitor coupling pin<br>To prevent degradation of image in a small amplitude of a burst signal, this pin stops a chrominance signal and the mode changes to black and white mode. | — |
| 61 |  | APC det.:<br>APC capacitor coupling pin<br>Matching the phase of a crystal oscillation to that of burst signal | — |
| 62 |  | SCP out:<br>Subcarrier pulse output pin | NTSC 3.58 MHz<br>PAL 4.43 MHz<br>  |
| 63 |  | VXO1:<br>NTSC crystal oscillator connecting pin<br>Use the capacitor with temperature characteristics (N750) to connect to the crystal oscillator. | — |

■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | Voltage · Waveform |
|---|---|---|---|
| 64 |  | VXO2:<br>PAL and PAL-M crystal oscillator connecting pin<br>Use the capacitor with temperature characteristics (N750) to connect to the crystal oscillator. | — |

## ■ Usage Notes

- The supply voltage applied to pin 6, pin 25, pin 29, pin 44, and pin 58 must be brought up at the same time.
- The crystal oscillator used must be evaluated thoroughly, because chrominance signal processing system characteristics change by the crystal oscillator type.
- The conversion of the analog RGB signals and the analog OSD signals with synchronous signals is not supported.
- Input the analog RGB signals and the analog OSD signals after filtering the pedestal parts of these signals.
- Evaluated thoroughly on the application of this device in the PAL.

## ■ Technical Data

### 1. Serial interface description

1) $I^2C$ bus control mode

A serial data is capable of transferring 9-bit unit of 8-bit transfer data and 1-bit answering data using two kinds of signal lines of data and shift clock.

When a slave address after setting a start condition matches the address on the IC side, you can receive the data to be transmitted from then. Once the stop condition is set up, the next transmitting data will be ignored until the start condition is set up.

There are two kinds of transfer mode: an auto-increment mode which does not transmit subaddress, and data upgrade mode which transmits subaddress + data by 2 bytes.

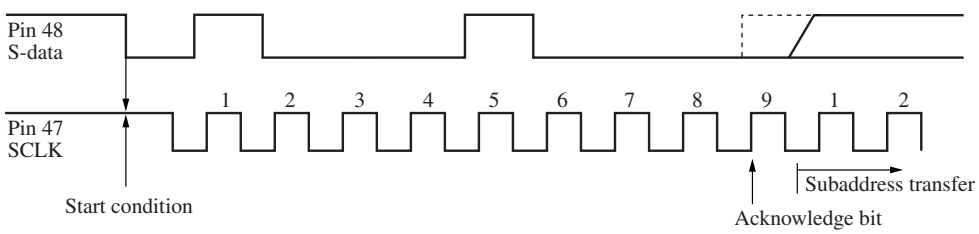
The typical models of communication sequence are shown below:

(1) Start condition

When the S-data changes from high level to low level at SCLK = high level, a data receiving mode becomes available.

(2) Slave address transfer

The slave address of the AN2546FH-A is 88h.



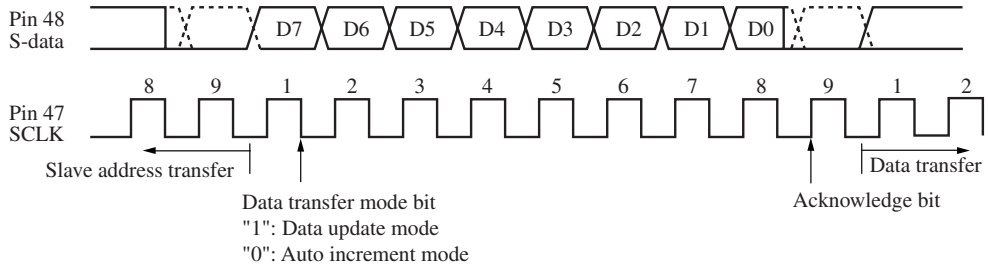
## ■ Technical Data (continued)

### 1. Serial interface description (continued)

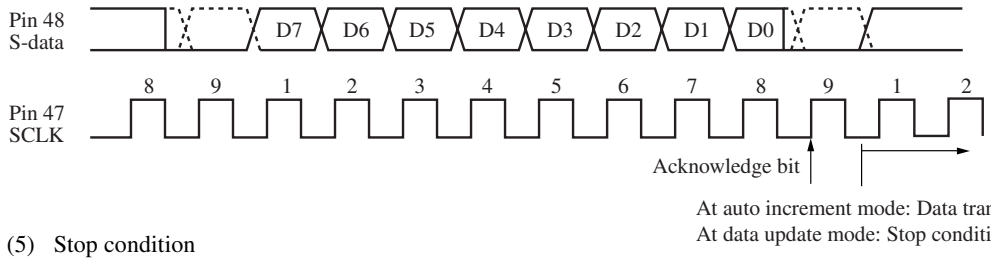
1) I²C bus control mode (continued)

(3) Subaddress transfer

When a data transfer mode bit is 0, all the serial data columns transferred until a stop condition is set is regarded as the data block.




(4) Data transfer

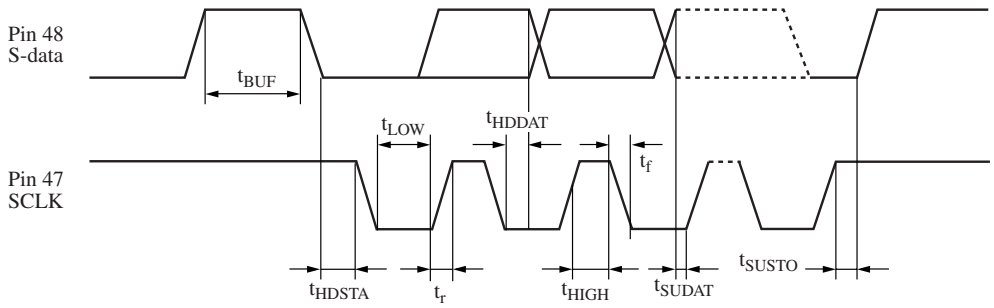



(5) Stop condition

When S-data changes from low level to high level at SCLK = high level, data reception is halted.

(6) Pulse timing

Timing chart expanded diagram




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCLK clock frequency | $t_{SCL}$ | 0 | — | 400 | kHz |
| Bus free-time for stop condition and start condition | $t_{BUF}$ | 1.3 | — | — | µs |
| Hold time start condition | $t_{HDSTA}$ | 0.6 | — | — | µs |
| SCLK clock low-state hold time | $t_{LOW}$ | 1.3 | — | — | µs |
| SCLK clock high-state hold time | $t_{HIGH}$ | 0.6 | — | — | µs |
| Data hold time | $t_{HDDAT}$ | 0 | — | — | µs |
| Data setup time | $t_{SUDAT}$ | 100 | — | — | ns |
| S-data and SCLK signal rise time | $t_r$ | — | — | 300 | ns |
| S-data and SCLK signal fall time | $t_f$ | — | — | 300 | ns |
| Stop condition setup time | $t_{SUSTO}$ | 0.6 | — | — | µs |

■ Technical Data (continued)

1. Serial interface description (continued)

2) Mode setting channel bits table

| ch. | Sub-address | Initial value (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 01 | 80 | Common amplitude | | | | | | | |
| 2 | 02 | 80 | Luminance gain | | | | | | | |
| 3 | 03 | 80 | Color gain | | | | | | | |
| 4 | 04 | 80 | Hue | | | | | | | |
| 5 | 05 | 40 | HGA | Black limiter | | | | | | |
| 6 | 06 | 80 | Brightness | | | | | | | |
| 7 | 07 | 80 | DBOSC | Aperture | | | | | | |
| 8 | 08 | 80 | R-ch. sub-brightness | | | | | | | |
| 9 | 09 | 80 | B-ch. sub-brightness | | | | | | | |
| 10 | 0A | C0 | DCLP | White peak limiter | | | | | | |
| 11 | 0B | 80 | Gamma 1 | | | | | | | |
| 12 | 0C | 80 | Gamma 2 | | | | | | | |
| 13 | 0D | 80 | Contrast | | | | | | | |
| 14 | 0E | 80 | R-ch. sub-contrast | | | | | | | |
| 15 | 0F | 80 | B-ch. sub-contrast | | | | | | | |
| 16 | 10 | 80 | VCO free-run *1 | | | | | | | |
| 17 | 11 | 03 | DFVD | DFSC | DPALM | DPALN | DSECAM | DVMODE | DUV | DCINT |
| 18 | 12 | 00 | MACRON | PLL stop position adjustment | | | | Vertical position adjustment | | |
| 19 | 13 | 80 | HOSEI | PWMT4 | KOTEI | Horizontal position adjustment | | | | |
| 20 | 14 | 80 | PWM frequency adjustment | | | | BLAK | Burst cleaning pulse position adjustment | | |
| 21 | 15 | 80 | PWM duty | | | | | | | |
| 22 | 16 | 7F | EXTTEST | DHTS | EXCHFI | POLSW | DMOSD | DSC | DCPS | DQPAL |
| 23 | 17 | 80 | Common DC *2 | | | | | | | |
| 24 | 18 | 80 | DC output adjustment | | | | | | | |

Note) ∗1: VCO free-run adjustment; ch.23 = 02h or more, EXTTEST = High

∗2: 00h, 01h are prohibition of use because of test mode.

## ■ Technical Data (continued)

### 1. Serial interface description (continued)

2) Mode setting channel bits table (continued)

(1) ch.5: Black limiter adjustment

| Sub-address | D7 HGA | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 05 | 0 | Output gain down mode | | | | | | |
| | 1 | Gain mode | | | | | | |

(2) ch.7: Aperture adjustment

| Sub-address | D7 DCLP | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 07 | 0 | VD free-run: NTSC = 265H, PAL = 315H | | | | | | |
| | 1 | VD free-run : NTSC = 263H, PAL = 313H | | | | | | |

(3) ch.10: White peak limiter adjustment

| Sub-address | D7 DCLP | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0A | 0 | NAVI sync. mode (Pin 45) | | | | | | |
| | 1 | Video sync. mode (Pin 46) | | | | | | |

(4) ch.17: Mode setup 1

| Sub-address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 11 | DFVD | DFSC | DPALM | DPALN | DSECAM | DVMODE | DUV | DCINT |

| Mode | Function | |
|---|---|---|
| DFVD | 0 | VD cycle: 60 Hz |
| | 1 | VD cycle: 50 Hz |
| DFSC | 0 | Subcarrier: 3.58 MHz |
| | 1 | Subcarrier: 4.43 MHz |
| DPALM | High = PALM mode on | |
| DPALN | High = PALN mode on | |
| DSECAM | High = SECAM mode on | |
| DVMODE | High = Burst swing off | |
| DUV | 0 | Chrominance input |
| | 1 | Color difference signal input |
| DCINT | 0 | RGB signal input |
| | 1 | Video signal input |

- at NTSC selection
  DFVD/DFSC/DPALM/DPALN/DSECAM = Low
  DVMODE = High
- at PAL selection
  DFVD/DFSC = High
  DPALM/DPALN/DSECAM/DVMODE = Low
- at PALM selection
  DPALM/DFVD = High
  DPALN/DSECAM/DVMODE = Low
- at PALN selection
  DPALN = High
  DPALM/DSECAM/DVMODE/DFVD = Low

(5) ch.18: PLL stop position and vertical sync. output position adjustment

| Sub-address | D7 MACRON | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| | | PLL stop position adjustment | | | | Vertical position adjustment | | |
| 12 | 0 | AFC normal operation | | | | | | |
| | 1 | Copy guard signal correspondence | | | | | | |

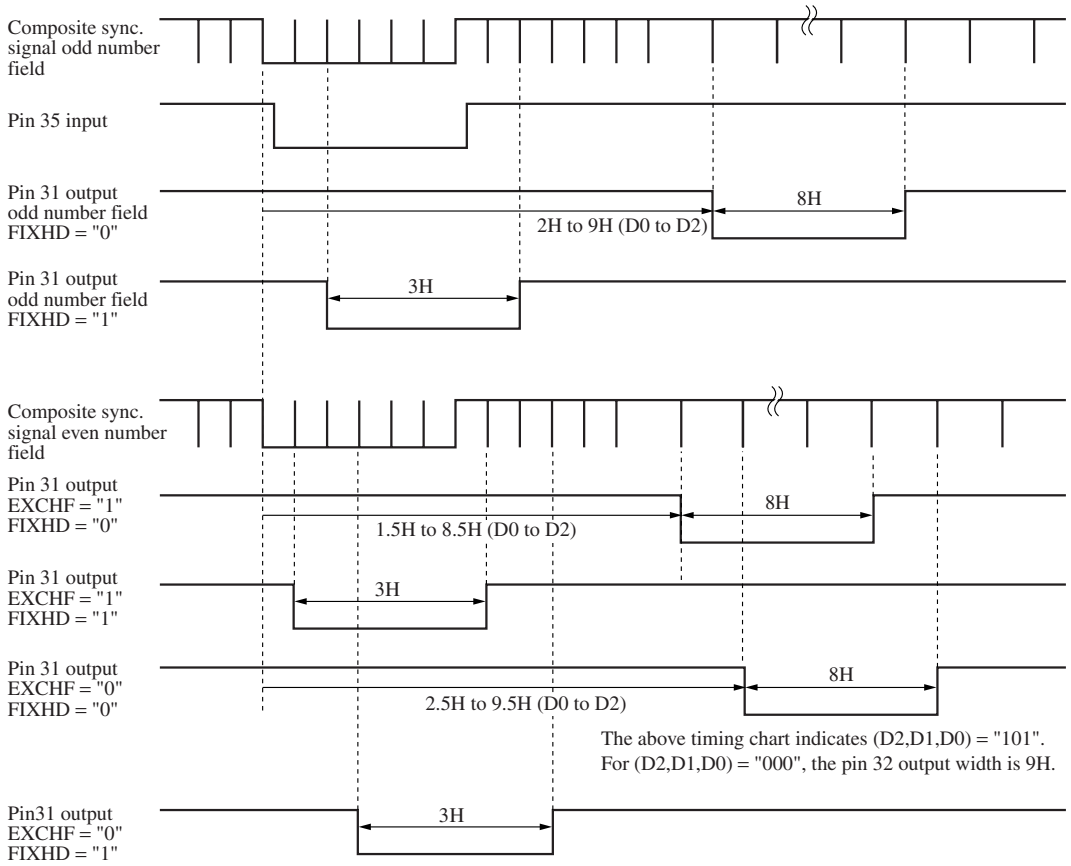
■ Technical Data (continued)

1. Serial interface description (continued)

2) Mode setting channel bits table (continued)

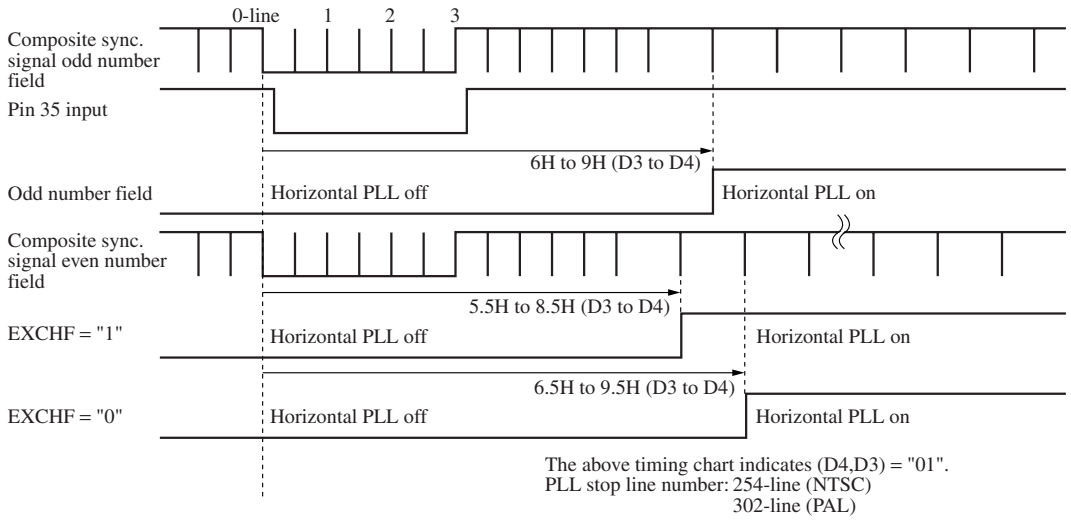
(5) ch.18: PLL stop position and vertical sync. position adjustment (continued)

<Vertical synchronous output timing adjustment range>




The pin 31 timing is synchronous with the pin 35 input timing. The above timing chart is just for reference

<Horizontal PLL start position adjustment range>



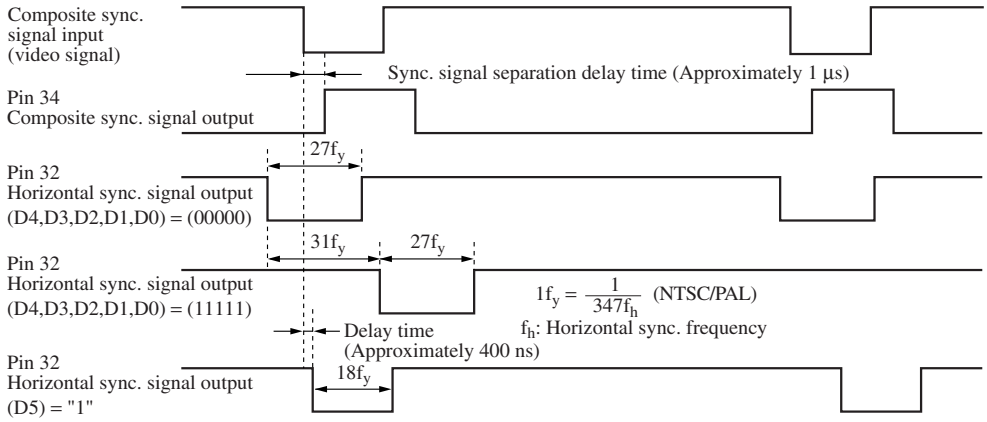
■ Technical Data (continued)

1. Serial interface description (continued)

2) Mode setting channel bits table (continued)

(6) ch.19: Horizontal sync. output position adjustment

| Sub-address | D7 HOSEI | D6 PWMT4 | D5 KOTEI | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 13 | | | 0 | Sync. output variable mode | | | | |
| | | | 1 | Sync. output fixation mode | | | | |
| | | — | PWM frequency adjustment | | | | | |
| | 0 | VCO automatic adjustment off | | | | | | |
| | 1 | VCO automatic adjustment on | | | | | | |




The delay time of pin 34 output to video signal is likely to vary according to an external constant connected to pin 46. For an external constant, the characteristics in weak electric field must be evaluate adequately.

Though the horizontal sync. signal output adjustment range is designed by referring to the center of pin 34 output pulse, there would be some error according to VCO free-run frequency.

(7) ch.20: PWM frequency and burst cleaning pulse width adjustment

| Sub-address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| | PWM frequency adjustment | | | | BLAK | Burst cleaning pulse adjustment | | |
| 14 | | | | | 0 | Black level variable mode | | |
| | | | | | 1 | Black level fixation mode | | |

## ■ Technical Data (continued)

### 1. Serial interface description (continued)

2) Mode setting channel bits table (continued)

(8) ch.22: Mode setup 2

| Sub-address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 16 | EXTTEST | DHTS | EXCHFI | POLSW | DMOSD | DSC | DCPS | DQPAL |

| Mode | Function | |
|---|---|---|
| EXTTEST | 0 | Normal mode |
| | 1 | Test mode |
| DHTS | 0 | 1H reverse stop |
| | 1 | 1H reverse |
| EXCHFI | 0 | Odd number field: Advance phase |
| | 1 | Even number field: Advance phase |
| POLSW | 0 | Internal POL 1H reverse mode |
| | 1 | External POL 1H reverse mode |
| DMOSD | 0 | Analog OSD signal input |
| | 1 | Digital OSD signal input |
| DSC | 0 | Subcarrier output stop |
| | 1 | Subcarrier output |
| DCPS | 0 | Component input mode |
| | 1 | Composite input mode |
| DQPAL | 0 | STD PAL mode |
| | 1 | Quasi PAL mode |

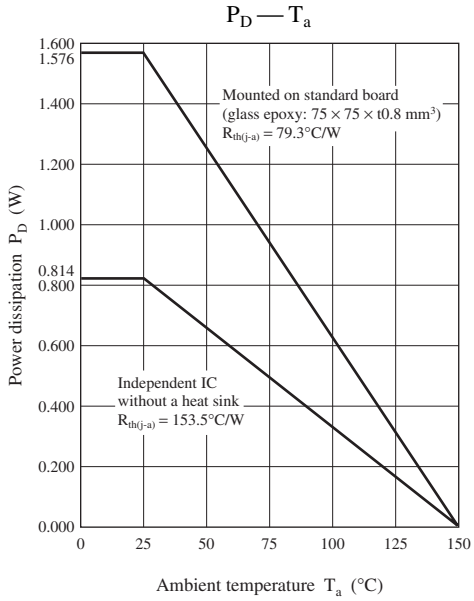
### 2. Recommended Operating Conditions

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Composite video input signal | $Y_{IN}$ | Sync. chip - White | 0.9 | 1.0 | 1.1 | V[p-p] |
| Y-input signal voltage | $Y_{IN}$ | Pedestal - White | 0.6 | 0.7 | 0.8 | V[p-p] |
| C-input signal voltage | $C_{IN}$ | Burst signal amplitude | 200 | 300 | 400 | mV[p-p] |
| MOS input signal low-level voltage | $V_{MOSL}$ | | 0 | — | 0.9 | V |
| MOS input signal high-level voltage | $V_{MOSH}$ | | 2.1 | — | ∗1 | V |
| Sync. signal input | $H_{SYNC}$ | Pedestal - Sync. chip | 0.2 | 0.3 | 0.4 | V[p-p] |
| Analog RGB signal input | $RGB_{IN}$ | Pedestal - White | 0.6 | 0.7 | 0.8 | V[p-p] |

Note) ∗1: Set it lower than $V_{CC1}$ (Pin 6 voltage).

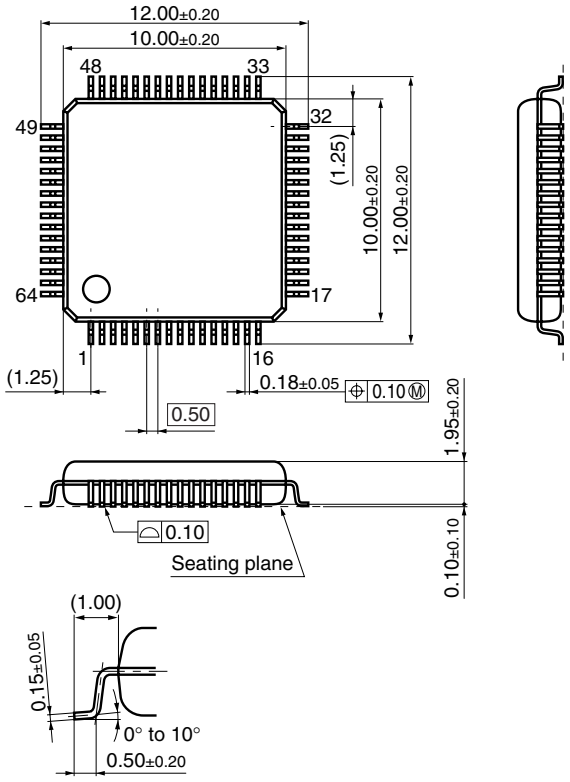
■ Technical Data (continued)

3. Power dissipation of package QFP064-P-1010




■ New Package Dimensions (Unit: mm)

• QFP064-P-1010A (Lead-free package)



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