



# PD55015 - PD55015S

## RF POWER TRANSISTORS

### The *LdmoST* Plastic FAMILY

PRELIMINARY DATA

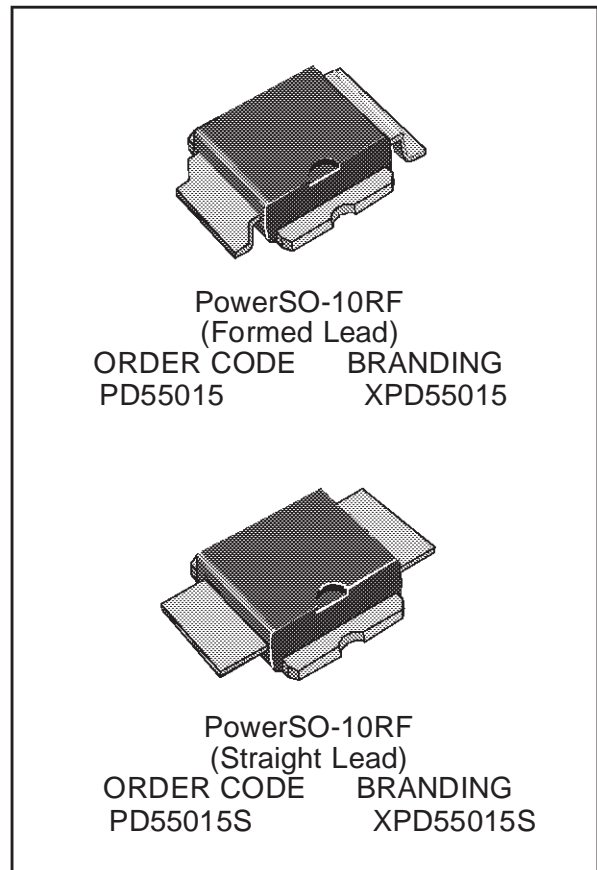
#### N-CHANNEL ENHANCEMENT-MODE LATERAL MOSFETs

- EXCELLENT THERMAL STABILITY
- COMMON SOURCE CONFIGURATION
- POUT = 15 W with 13.5 dB gain @ 500 MHz / 12.5V
- NEW RF PLASTIC PACKAGE

#### DESCRIPTION

The PD55015 is a common source N-Channel, enhancement-mode, lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 12V in common source mode at frequencies of up to 1GHz. PD55015 boasts the excellent gain, linearity and reliability of ST's latest LDMOS technology mounted in the first true SMD plastic RF power package, PowerSO-10RF. PD55015's superior linearity performance makes it an ideal solution for car mobile radio.

The PowerSO-10 plastic package, designed to offer high reliability, is the first ST JEDEC approved, high power SMD package. It has been specially optimized for RF needs and offers excellent RF performances and ease of assembly.



#### ABSOLUTE MAXIMUM RATINGS ( $T_{CASE} = 25^{\circ}C$ )

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current	5	A
$P_{DISS}$	Power Dissipation (@ $T_c = 70^{\circ}C$ )	73	W
$T_j$	Max. Operating Junction Temperature	165	$^{\circ}C$
$T_{STG}$	Storage Temperature	-65 to 165	$^{\circ}C$

#### THERMAL DATA

$R_{th(j-c)}$	Junction-Case Thermal Resistance	1.3	$^{\circ}C/W$
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**PD55015 - PD55015S**

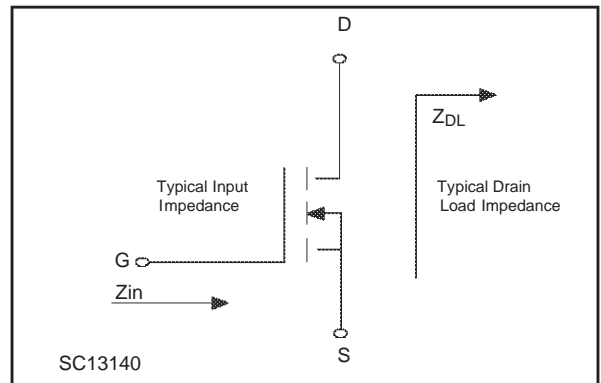
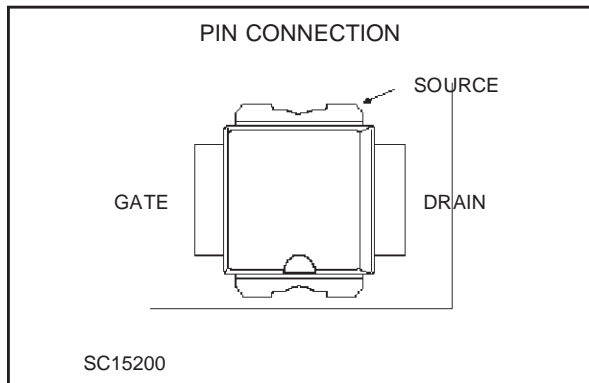
**ELECTRICAL SPECIFICATION**( $T_{CASE} = 25\text{ }^{\circ}\text{C}$ )

**STATIC**

Symbol	Parameter		Min.	Typ.	Max.	Unit
$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$			1	$\mu\text{A}$
$V_{GS(Q)}$	$V_{DS} = 10\text{ V}$	$I_D = 150\text{ mA}$	2.0		5.0	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.5\text{ A}$			0.8	V
$g_{FS}$	$V_{DS} = 10\text{ V}$	$I_D = 2.5\text{ A}$	2.0	2.5		mho
$C_{ISS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 12.5\text{ V}$	$f = 1\text{ MHz}$		89	pF
$C_{OSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 12.5\text{ V}$	$f = 1\text{ MHz}$		60	pF
$C_{RSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 12.5\text{ V}$	$f = 1\text{ MHz}$		6.5	pF

**DYNAMIC**

Symbol	Parameter				Min.	Typ.	Max.	Unit
$P_{OUT}$	$f = 500\text{ MHz}$	$V_{DD} = 12.5\text{ V}$	$I_{DQ} = 150\text{ mA}$		15			W
$G_{PS}$	$f = 500\text{ MHz}$	$V_{DD} = 12.5\text{ V}$	$P_{OUT} = 15\text{ W}$	$I_{DQ} = 150\text{ mA}$		13.5		dB
$\eta_D$	$f = 500\text{ MHz}$	$V_{DD} = 12.5\text{ V}$	$P_{OUT} = 15\text{ W}$	$I_{DQ} = 150\text{ mA}$		50		%
LOAD Mismatch	$f = 500\text{ MHz}$	$V_{DD} = 15.5\text{ V}$	$P_{OUT} = 15\text{ W}$	$I_{DQ} = 150\text{ mA}$	20:1			VSWR



**IMPEDANCE DATA**

**PD55015**

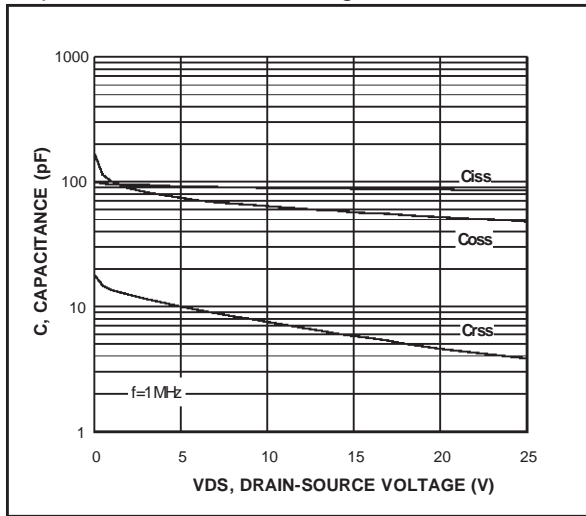
Frequency MHz	$Z_{in}$ $\Omega$	$Z_{dl}$ $\Omega$
480	$2.13 - j1.09$	$1.55 + j.34$
500	$1.95 - j.31$	$1.63 - j.25$
520	$1.83 - j.70$	$1.43 + j.30$

**PD55015S**

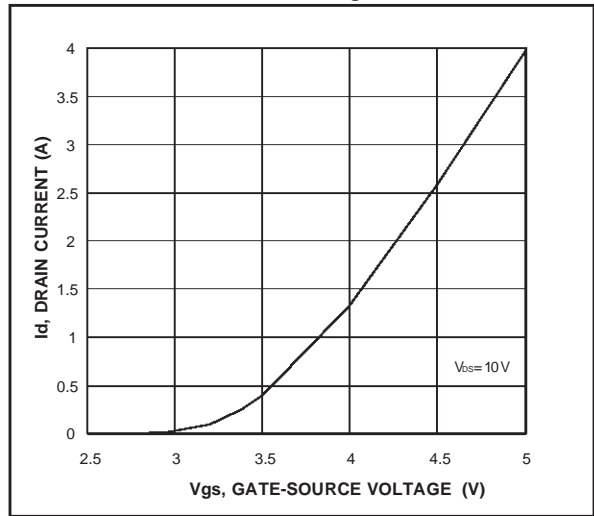
Frequency MHz	$Z_{in}$ $\Omega$	$Z_{dl}$ $\Omega$
480	$1.43 - j1.27$	$1.47 + j.65$
500	$1.62 - j1.05$	$1.49 + j.58$
520	$1.57 - j.91$	$1.35 + j.36$

TYPICAL PERFORMANCE

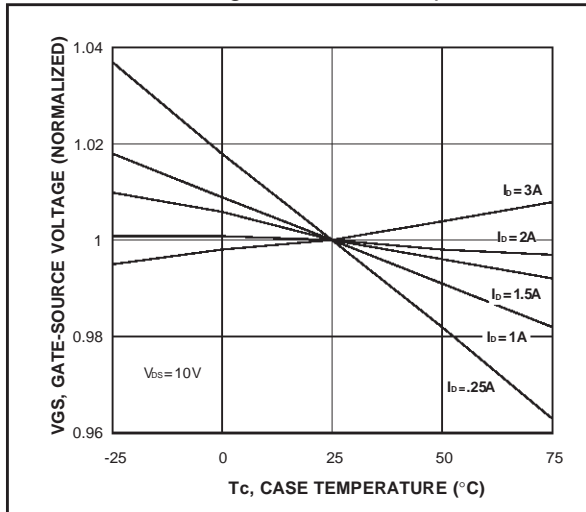
Capacitance vs. Drain Voltage



Drain Current vs. Gate Voltage



Gate-Source Voltage vs. Case Temperature

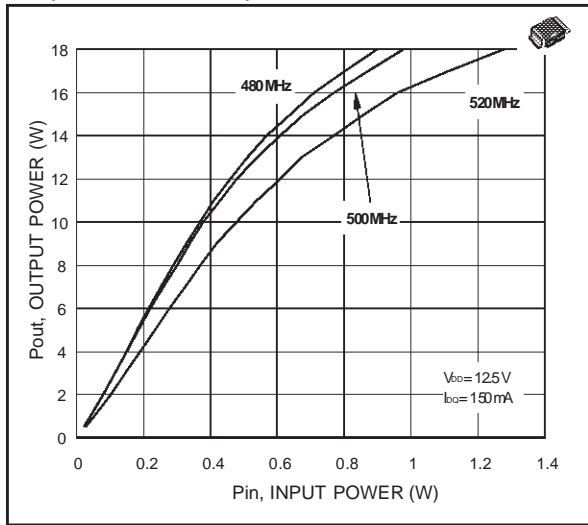


**PD55015 - PD55015S**

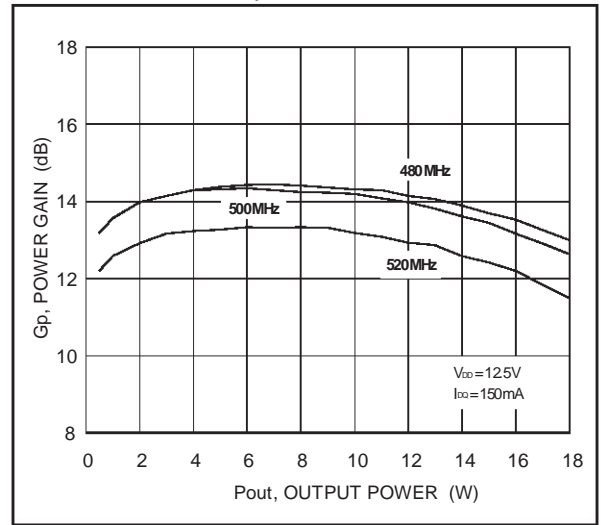
**TYPICAL PERFORMANCE**

**Output Power vs. Input Power**

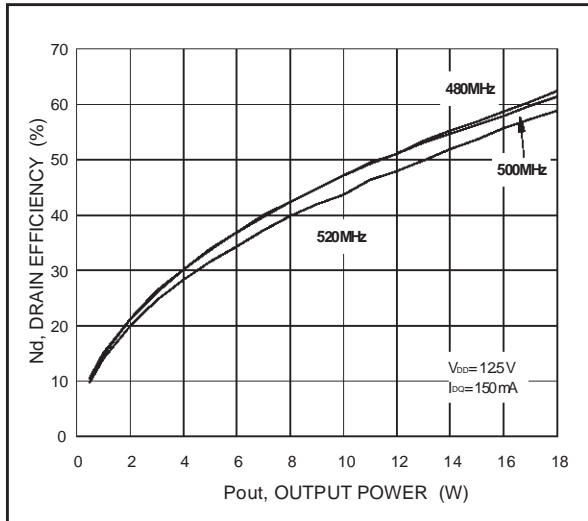
**PD55015**



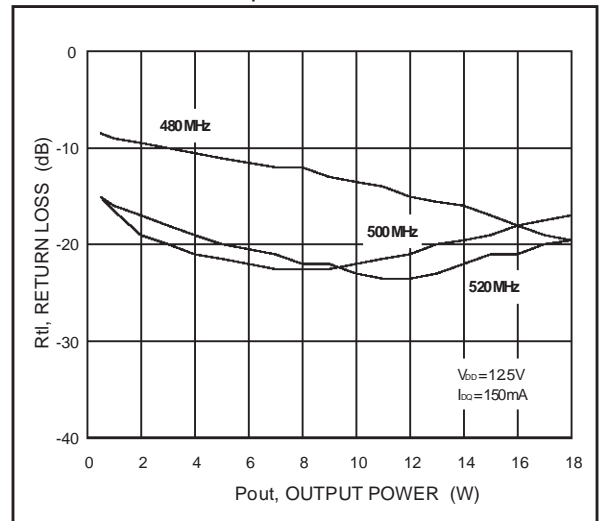
**Power Gain vs. Output Power**



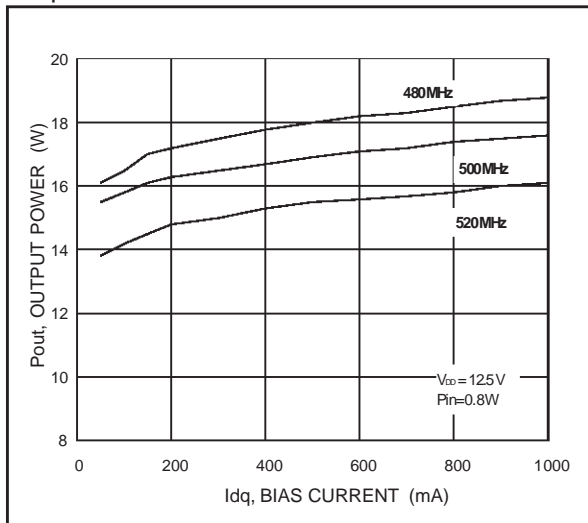
**Drain Efficiency vs. Output Power**



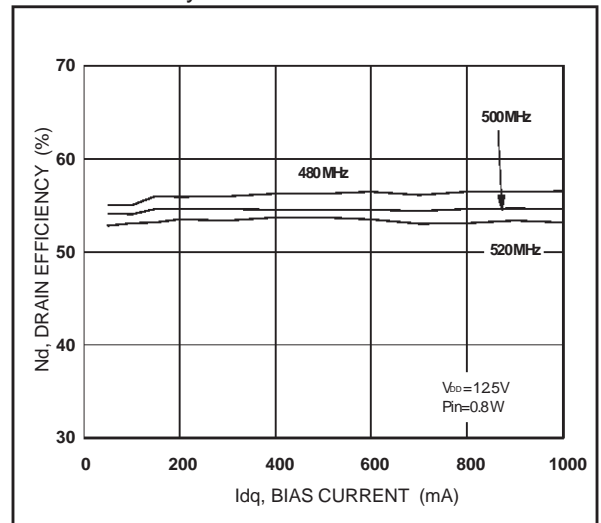
**Return Loss vs. Output Power**



**Output Power vs. Bias Current**

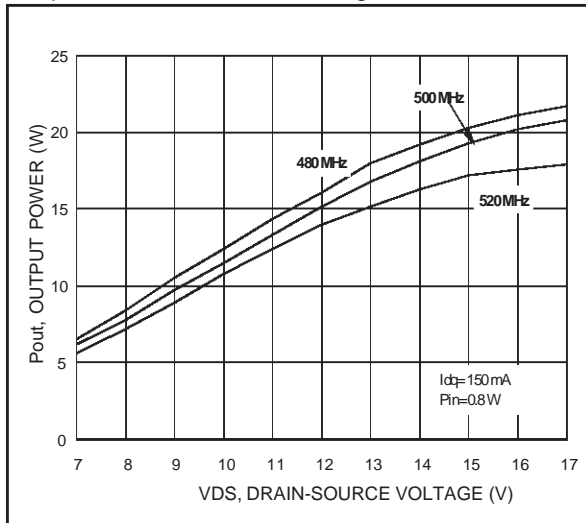


**Drain Efficiency vs. Bias Current**

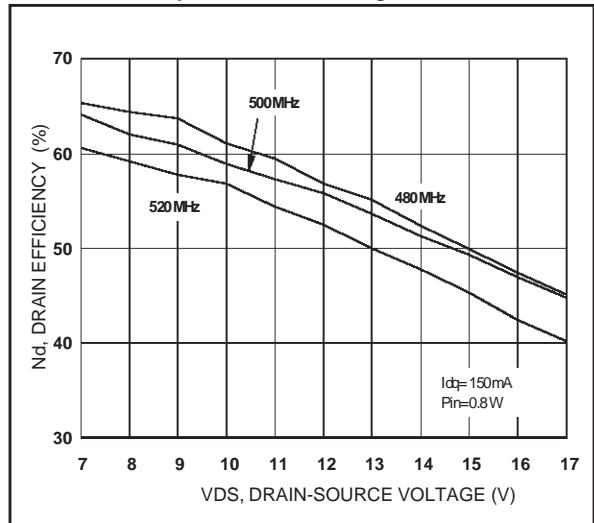


TYPICAL PERFORMANCE

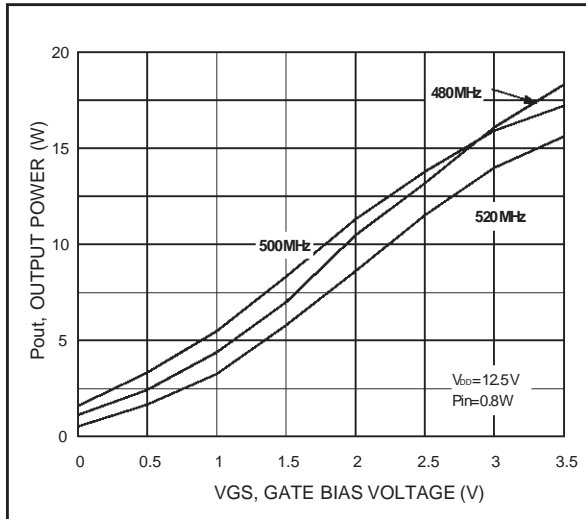
Output Power vs. Drain Voltage



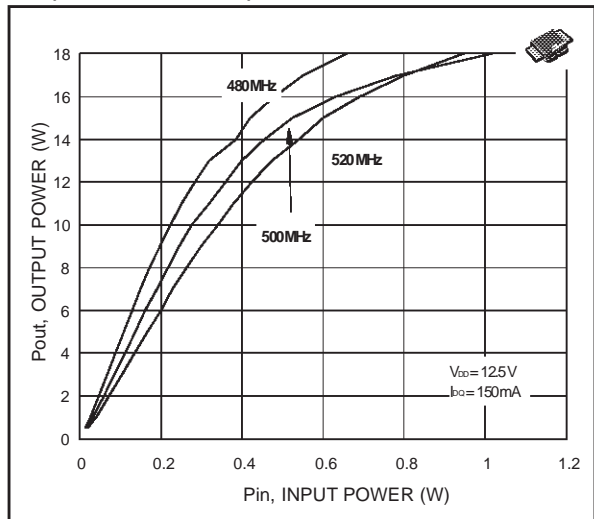
Drain Efficiency vs. Drain Voltage



Output Power vs. Gate Bias Voltage

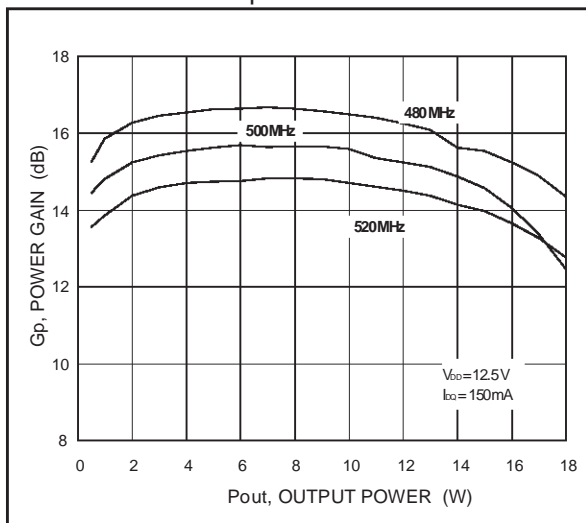


Output Power vs. Input Power

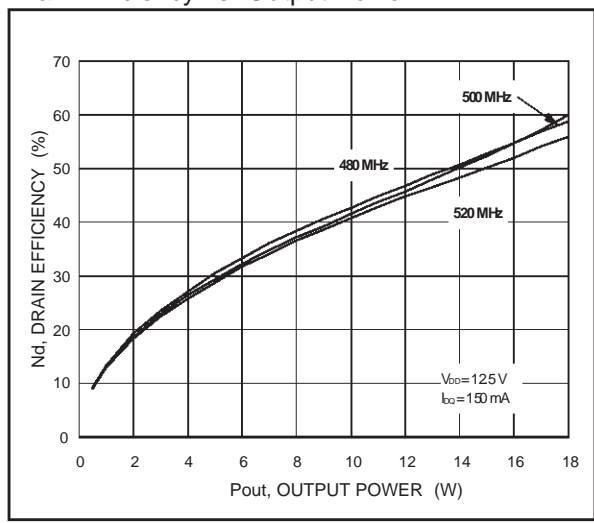


PD55015S

Power Gain vs. Output Power



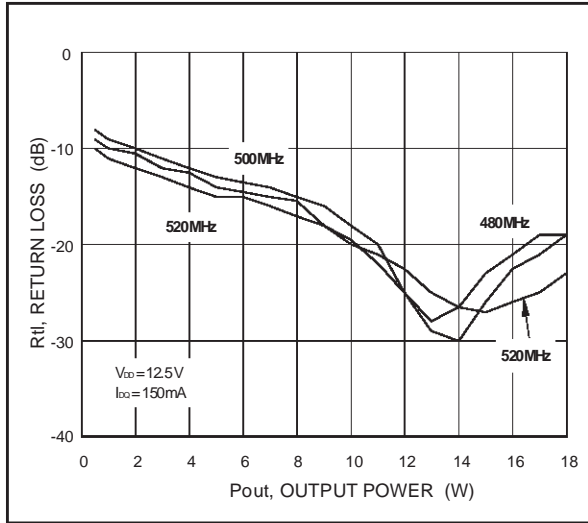
Drain Efficiency vs. Output Power



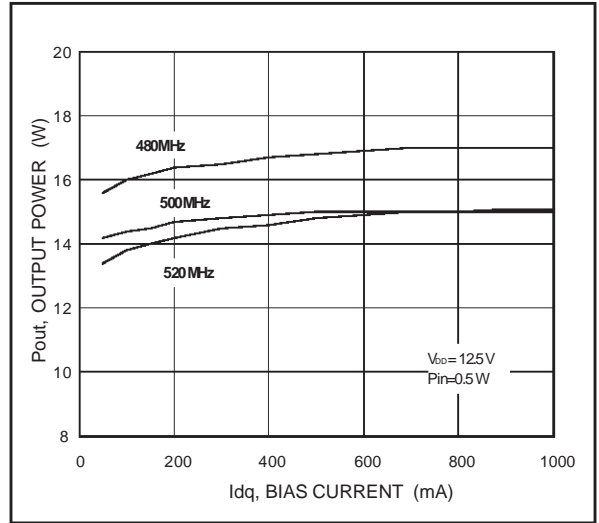
**PD55015 - PD55015S**

**TYPICAL PERFORMANCE**

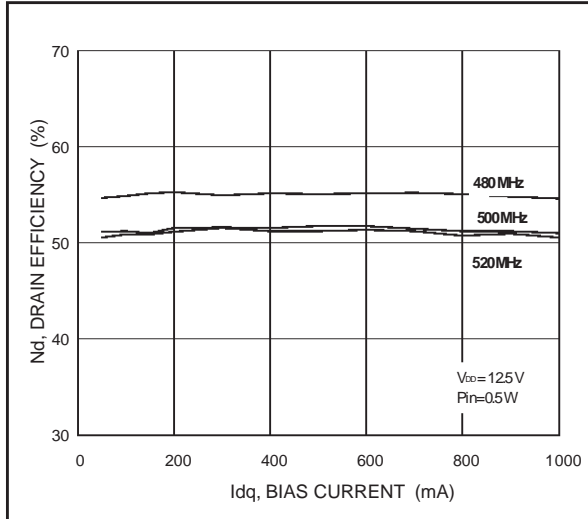
Return Loss vs. Output Power



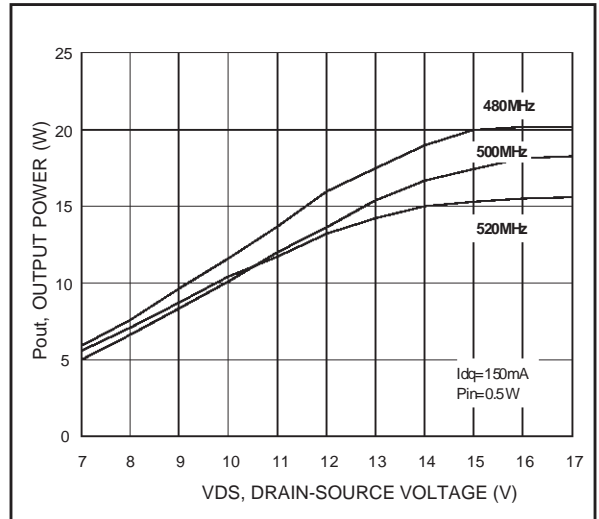
Output Power vs. Bias Current



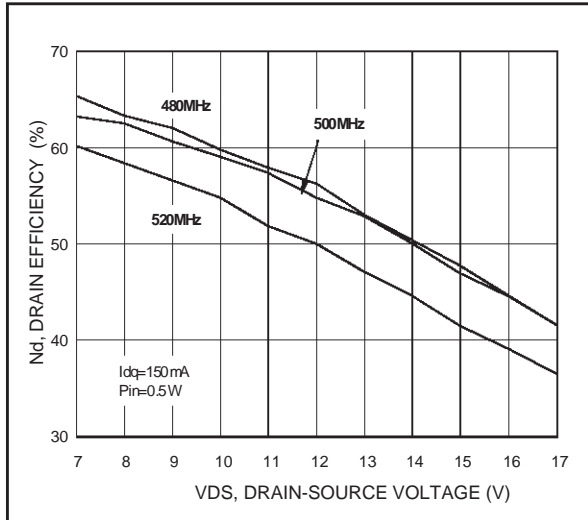
Drain Efficiency vs. Bias Current



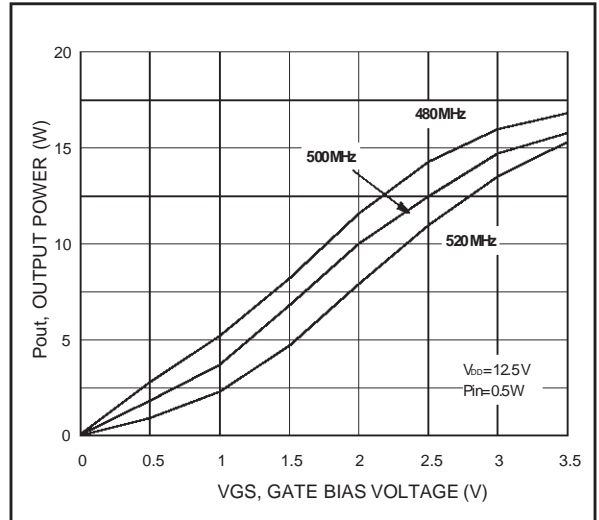
Output Power vs. Drain Voltage



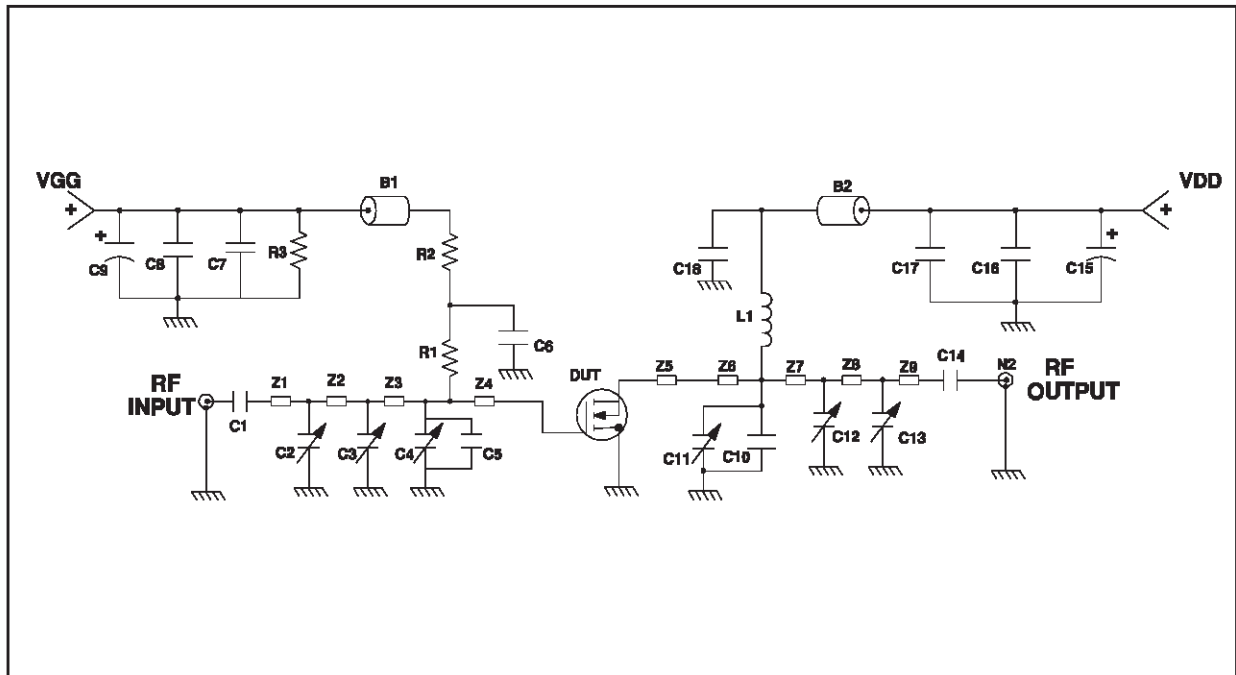
Drain Efficiency vs. Drain Voltage



Output Power vs. Gate Bias Voltage



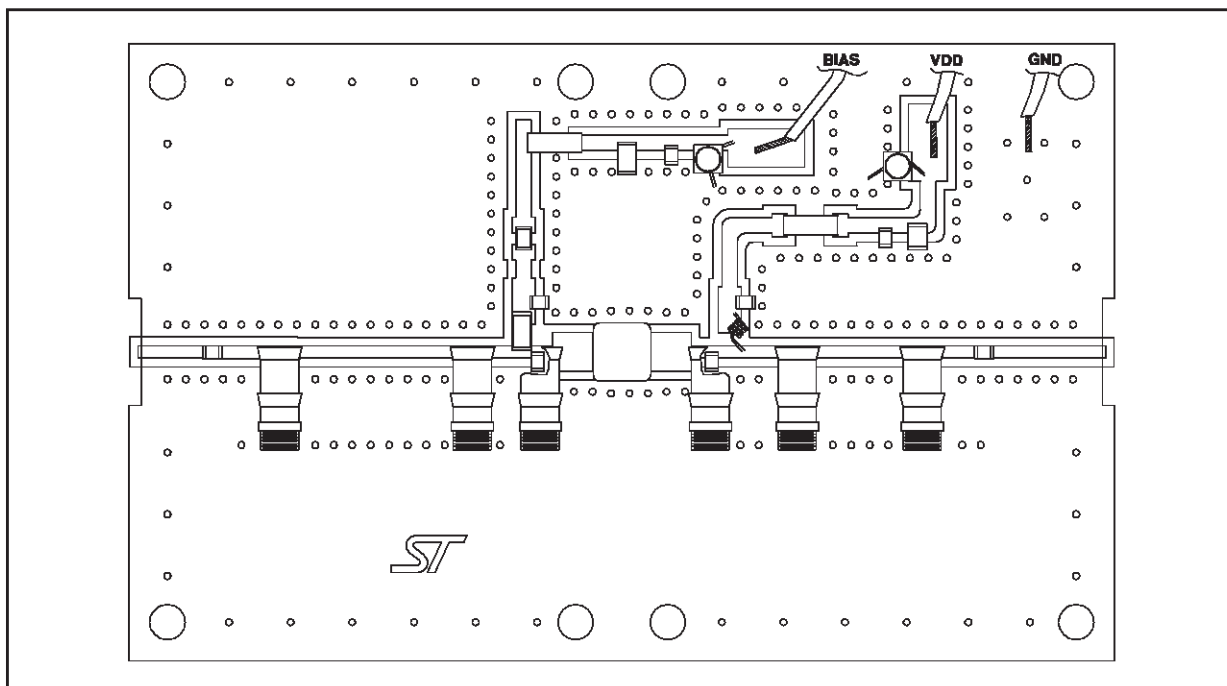
TEST CIRCUIT SCHEMATIC



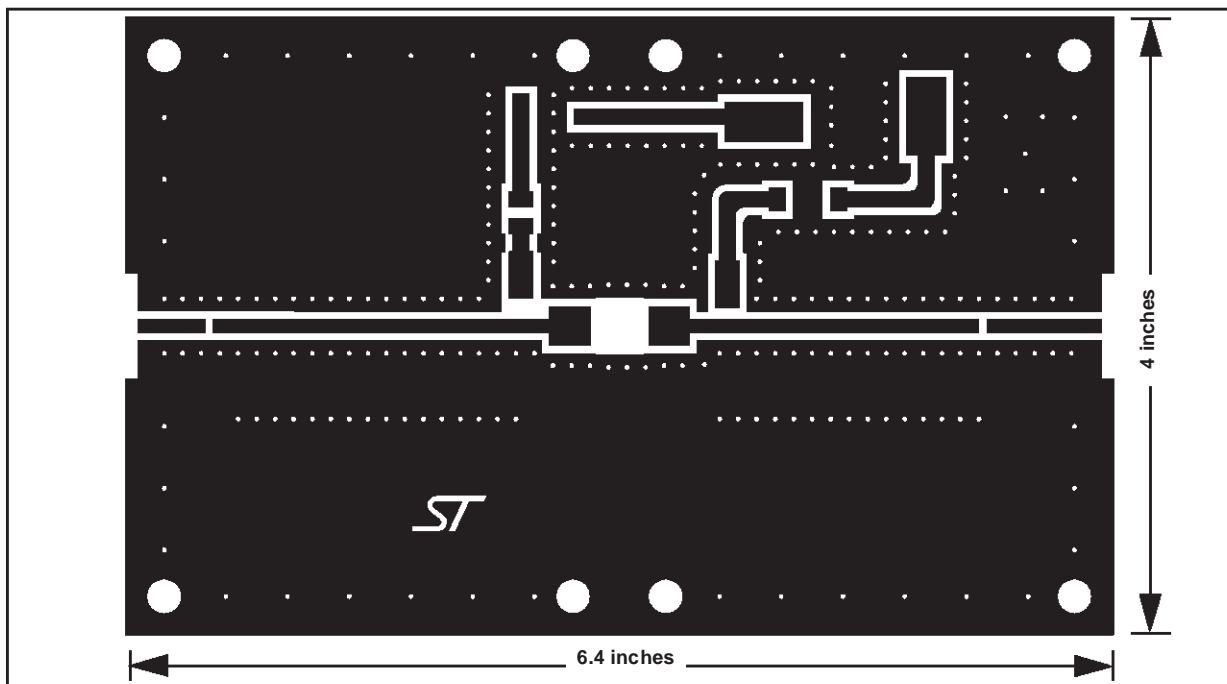
TEST CIRCUIT COMPONENT PART LIST

B1,B2	FERRITE BEAD	R2	1 k $\Omega$ , 1W CHIP RESISTOR
C1,C12	300pF, 100 mil CHIP CAPACITOR	R3	33 k $\Omega$ , 1W CHIP RESISTOR
C2,C3,C4,C11, C12,C13	1 TO 20 pF TRIMMER CAPACITOR	Z1	0.471" X 0.080" MICROSTRIP
C6,C18	pF 100 mil CHIP CAP	Z2	1.082" X 0.080" MICROSTRIP
C9,C15	10 $\mu$ F, 50V ELECTROLYTIC CAPACITOR	Z3	0.372" X 0.080" MICROSTRIP
C8,C16	0.1mF, 100 mil CHIP CAP	Z4,Z5	0.260" X 0.223" MICROSTRIP
C7,C17	1,000pF 100 mil CHIP CAP	Z6	0.050" X 0.080" MICROSTRIP
C5, C10	33pF, 100 mil CHIP CAP	Z7	0.551" X 0.080" MICROSTRIP
L1	56nH, 7 TURN, COILCRAFT	Z8	0.825" X 0.080" MICROSTRIP
N1,N2	TYPE N FLANGE MOUNT	Z9	0.489" X 0.080" MICROSTRIP
R1	15 $\Omega$ , 1W CHIP RESISTOR	BOARD	ROGER, ULTRA LAM 2000 THK 0.030" $\epsilon_r = 2.55$ 2oz ED Cu 2 SIDES

TEST CIRCUIT

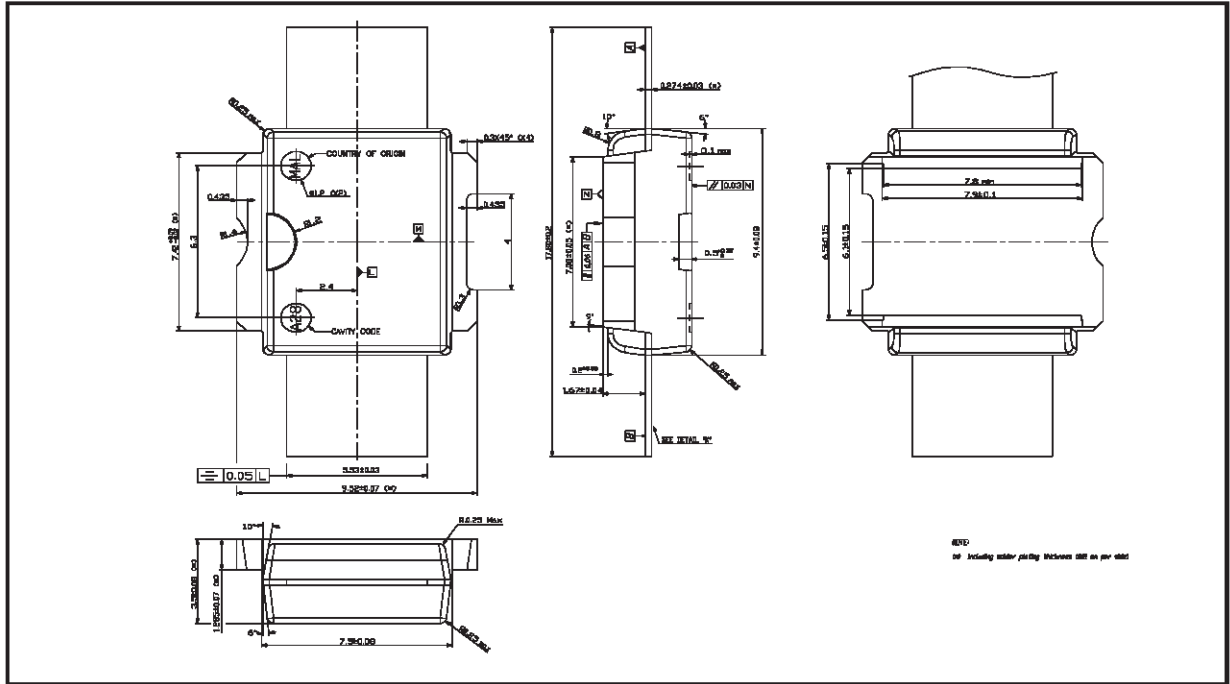


TEST CIRCUIT PHOTOMASTER

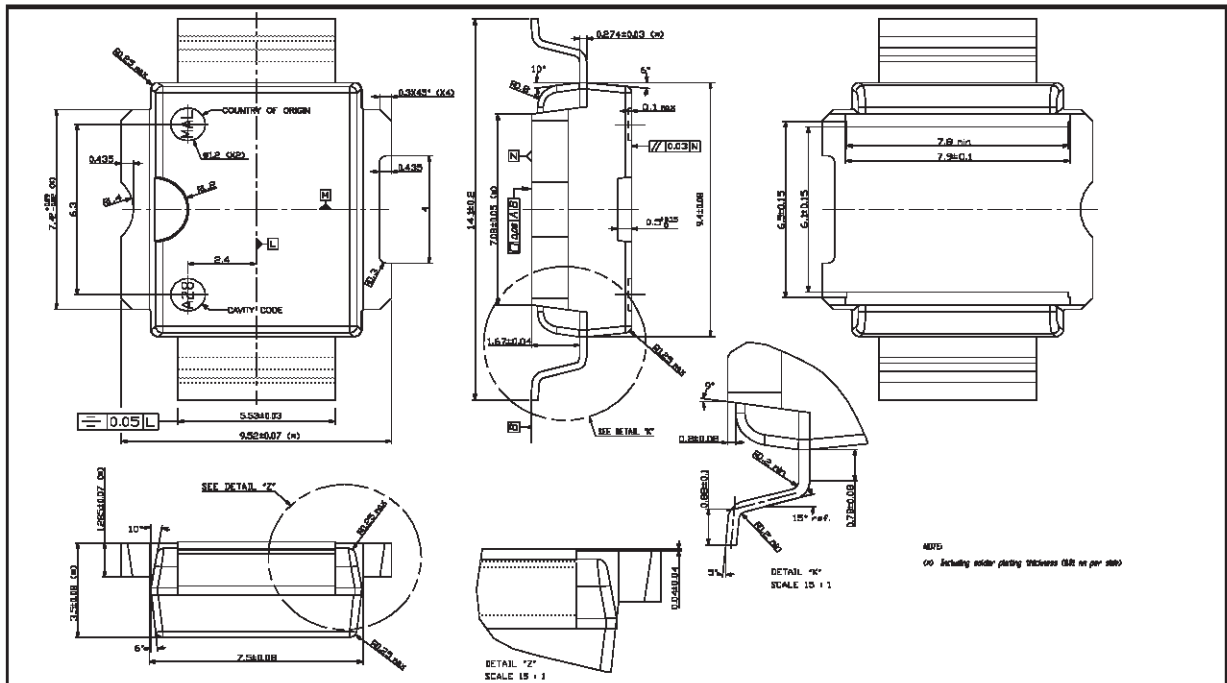




PowerSO-10RF (Straight Lead) MECHANICAL DATA



PowerSO-10RF (Formed Lead) MECHANICAL DATA



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