MOTOROLA

SN54/74LS298

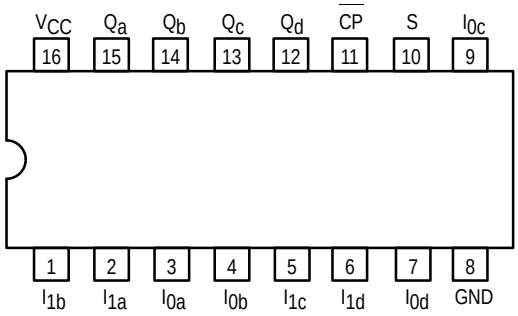
QUAD 2-INPUT MULTIPLEXER WITH STORAGE

The SN54/74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

- Select From Two Data Sources
- Fully Edge-Triggered Operation
- Typical Power Dissipation of 65 mW
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

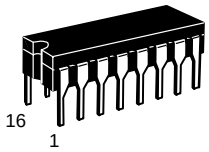
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$\overline{S}$	Common Select Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$I_{0a}-I_{0d}$	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
$I_{1a}-I_{1d}$	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
Q_a-Q_d	Register Outputs (Note b)	10 U.L.	5 (2.5) U.L.

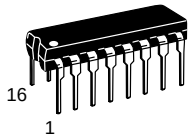
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

QUAD 2-INPUT MULTIPLEXER WITH STORAGE

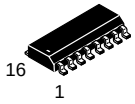
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

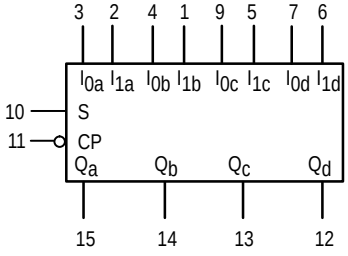


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

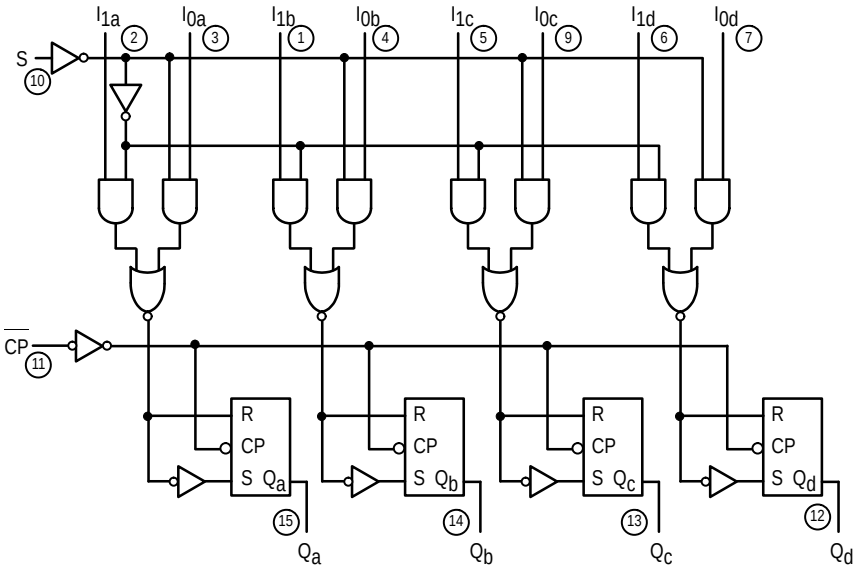
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC OR BLOCK DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
◯ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports)under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one setup time prior to the HIGH to LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	**I_0**	**I_1**	**Q**
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one setup time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one setup time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				21	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Propagation Delay, Clock to Output		18	27	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}			21	32	ns	

AC SET-UP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

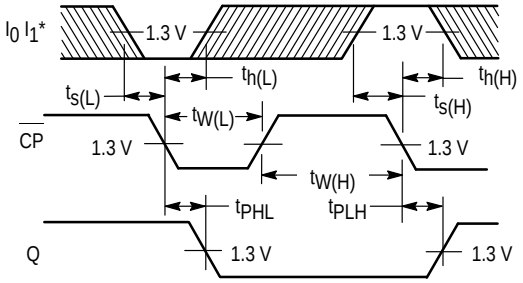
Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_W	Clock Pulse Width	20			ns	V_{CC} = 5.0 V
t_s	Data Setup Time	15			ns	
t_s	Select Setup Time	25			ns	
t_h	Data Hold Time	5.0			ns	
t_h	Select Hold Time	0				

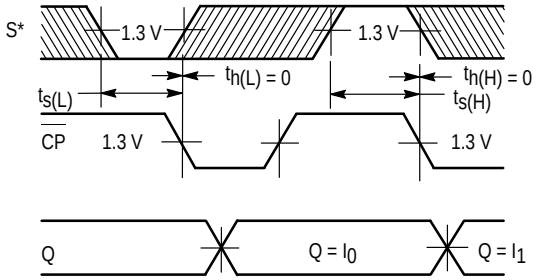
DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS





*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1

Figure 2