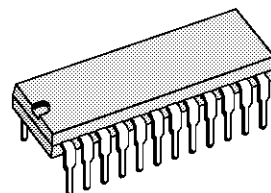


HORIZONTAL AND VERTICAL PROCESSOR

- 503kHz REFERENCE OSCILLATOR
- 5.5V SUPPLY VOLTAGE INTERNALLY REGULATED
- VERY SOPHISTICATED SYNC. SEPARATOR
- COUNT DOWN TIMING LOGIC
- ADAPTS AUTOMATICALLY TO 625 LINE/50Hz AND 525 LINE/60Hz STANDARDS
- 50/60 Hz IDENTIFICATION OUTPUT
- AUTOMATIC VERTICAL AMPLITUDE CORRECTION 50/60Hz
- CRT PROTECTION CIRCUIT
- PHASE-CORRECTED HORIZONTAL OUTPUT WITH CONSTANT DUTY CYCLE



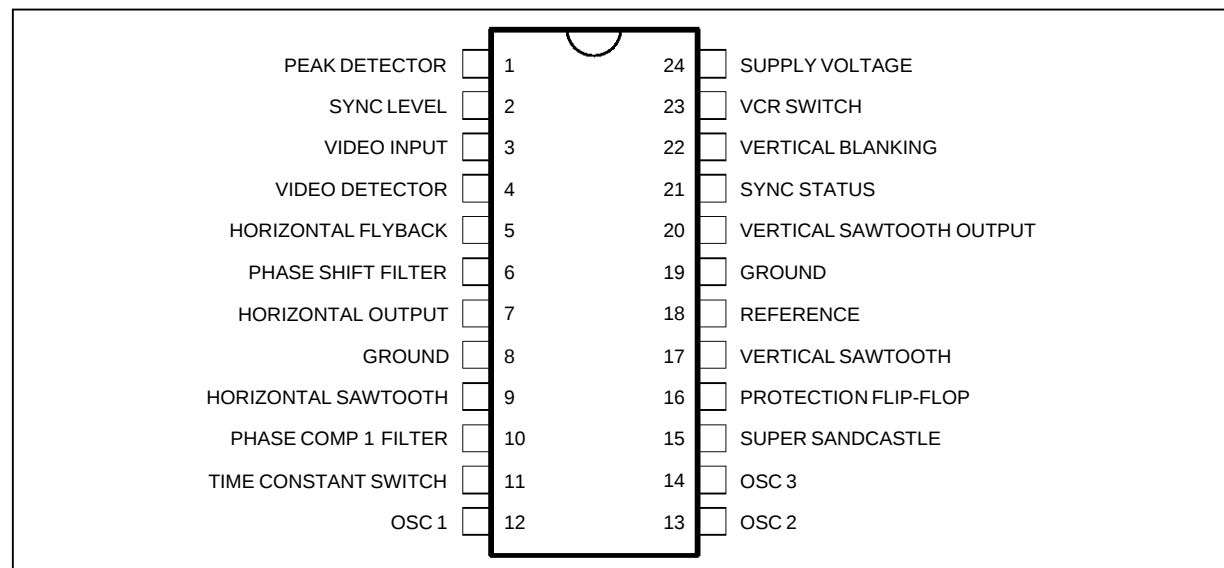
DIP24
(Plastic Package)

ORDER CODE : TDA8185I

DESCRIPTION

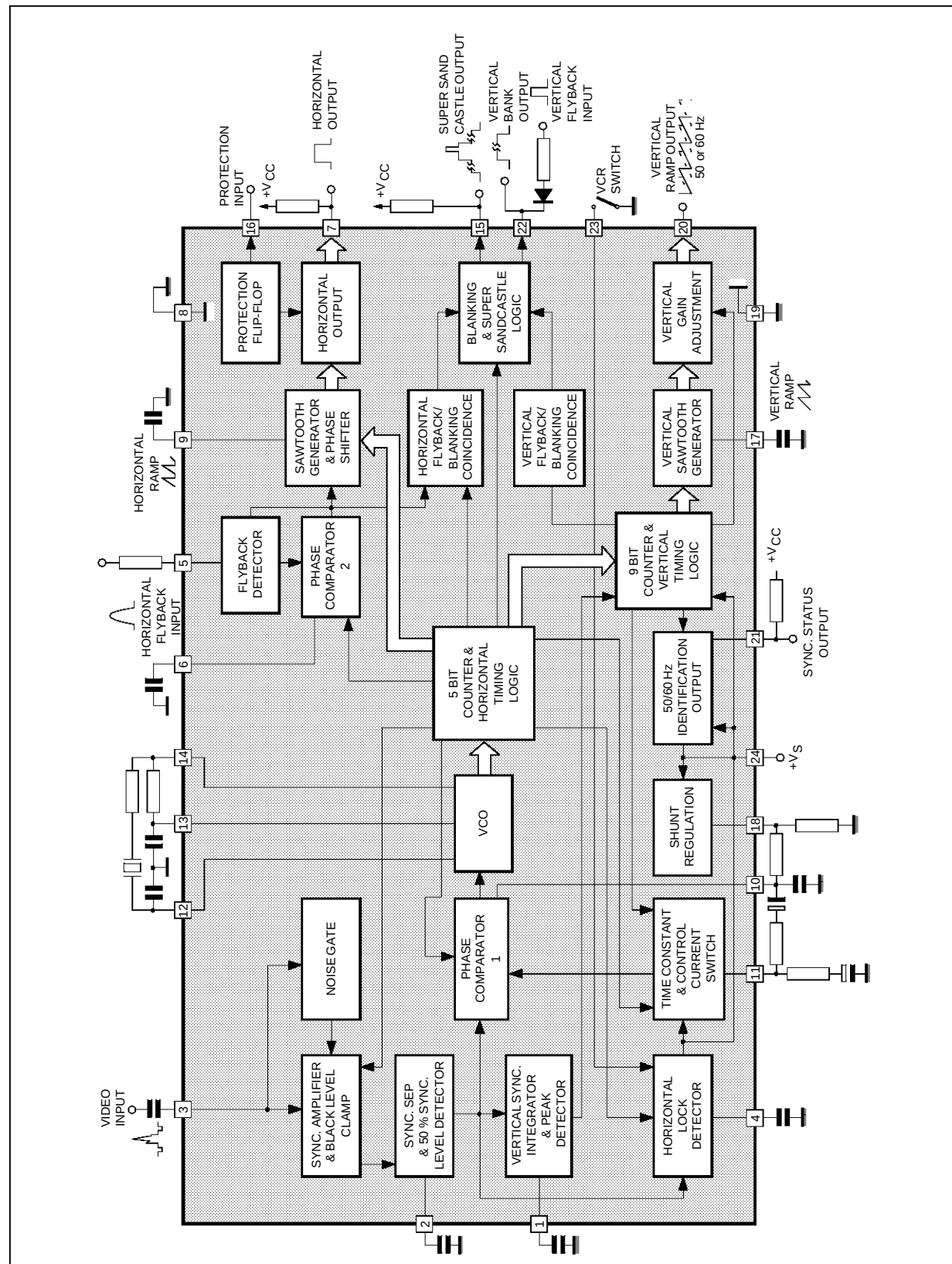
The TDA8185I is a monolithic integrated circuit in 24 pins dual in line plastic package intended for TV signal processing and driving Horizontal and Vertical output stages. It was specially designed for VCR working conditions.

PIN CONNECTIONS



8185I-01.EPS

BLOCK DIAGRAM



8185I-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _S	Supply Voltage at Pin 24 (low impedance)	5.25	V
V _{CC}	Voltage at Pins, 7, 15, 21	20	V
V _I	Input Signals	5	V
P _{tot}	Total Power Dissipation (T _{amb} = 70 °C)	1	W
T _j , T _{stg}	Storage and Junction Temperature	– 40 to 150	°C

8185I-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-pins}	Thermal Resistance Junction-pins Max	80	°C

8185I-02.TBL

ELECTRICAL CHARACTERISTICS

(V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _S	Supply Voltage (pin 24)		4.75	5	5.25	V
I _S	Supply Current (pin 24)		30	60	85	mA
V ₂₄	Stabilized Voltage at Pin 24			5.6		V

SYNC. SEPARATOR

V ₃	Peak to Peak Input Signal (negative video signal)		0.3	1	4	V
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VIDEO IDENTIFICATION AND VCR SWITCH

V ₂₃	VCR Switch Voltage		1.6	2.1	2.4	V
V ₄	Threshold Voltage for Time Constant Switching			2.3		V
I ₄	Peak Output Current	Lock		1		mA
– I ₄	Output Current			20		µA

OSCILLATOR

F _O	Free Running Frequency			500		kHz
S _O	Frequency Control Sensitivity			1.0		kHz/V
V ₁₀	Control Voltage Range			2.6 to 4		V

SYNC-OSCILLATOR PHASE COMPARATOR

I ₁₀	Control Peak Current			± 0.3		mA
I ₁₀	VCR Control Peak Current			± 0.6		mA
Δf	Catching and Holding Range			± 400		Hz

FLYBACK – OSCILLATOR PHASE COMPARATOR

V ₆	Control Voltage Range			2.8 to 3.7		V
I ₅	Flyback Input Current		0.1			
	Flyback Input Threshold			5		mA
I ₆	Peak Control Current			± 0.5		mA
	Static Control Error			1		%
t _d	Permissible Delay between Output Pulse and Flyback Pulse	t _{flyback} = 12 µs		17		µs

8185I-03.TBL

ELECTRICAL CHARACTERISTICS (continued)(V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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COMPOSITE BLANKING AND KEY PULSE (supersandcastle)

V _K	Key Pulse Output Peak Voltage			10		V
V _L	Line Blanking Voltage		4.25	4.5	4.75	V
V _F	Frame Blanking Voltage		2.38	2.5	2.63	V
t _{KS}	Phase Relationship between Leading Edge of Key Pulse and Middle of Sync. Pulse			2.5		μs
t _K	Key Pulse Duration			4		μs
t _F	Vertical Blanking Duration			1.4		ms

FRAME

V ₂₀	Output p.p. Sawtooth Voltage	50Hz and 60Hz		2.7		V
V ₂₀	Pedestal Voltage			0.3		V

LINE

I ₇	Output Current			50		mA
V ₇	Saturation Voltage	I ₇ = 50mA		0.4		V
t _L	Output Pulse Duration			29		μs

SYNC. STATUS OUTPUT

V ₂₁	Output Voltage	50Hz 60Hz Unlock	6.25	12 7	7.45 0.3	V V V
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OVERALL PHASE RELATION SHIP

t _o	Phase Difference between Middle of Flyback and Middle of Sync. Pulses			2		μs
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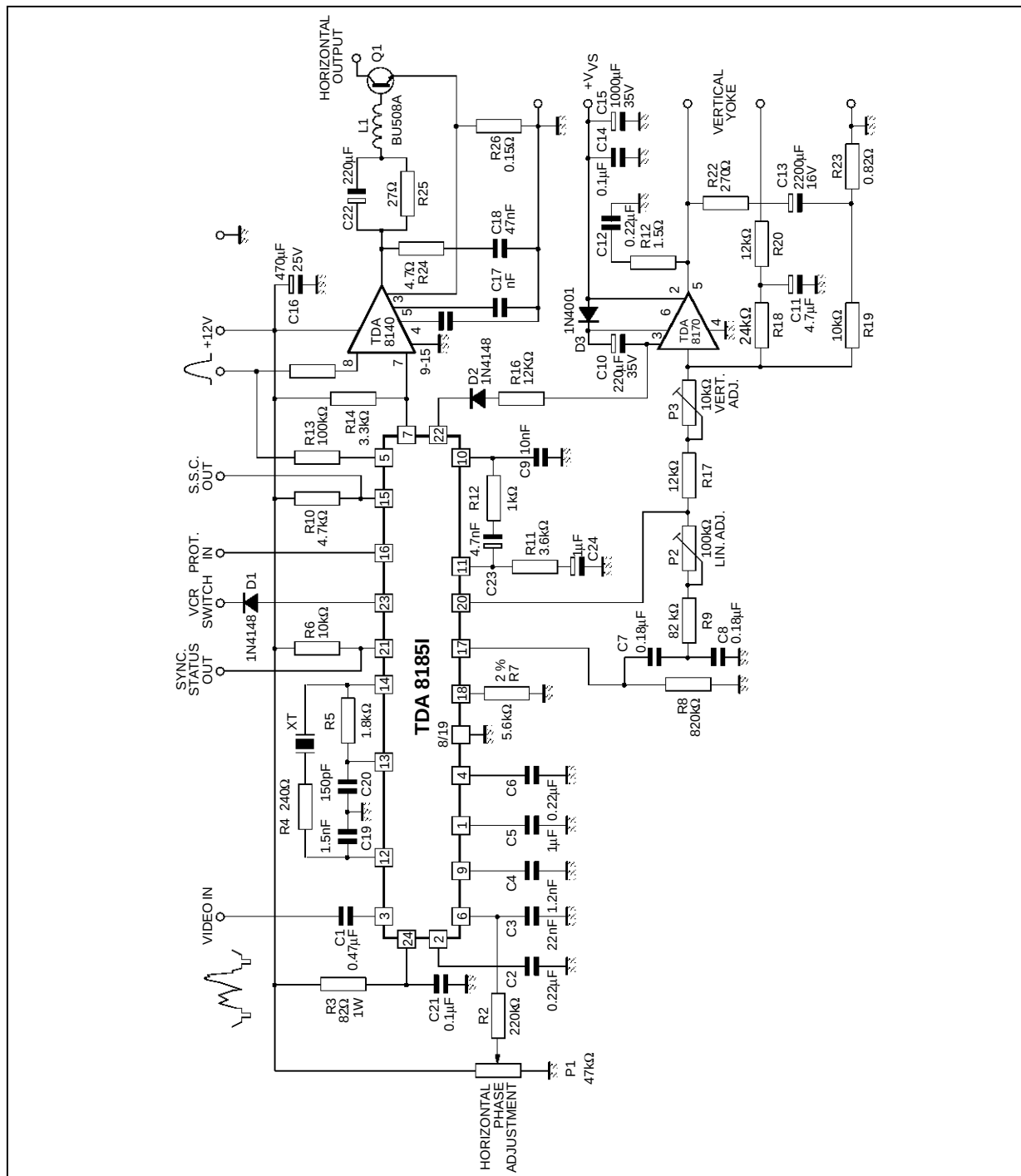
VERTICAL BLANKING OUT AND FLY. INPUT

V ₂₂	Blanking Output Voltage			4		V
V ₂₂	Flyback Threshold Input			5.7		V
I ₂₂	Flyback Current Input		0.1			mA

- Notes :**
1. With t_{fly} = 12 μs and t_i = 29 μs.
 2. The TDA8185I may be operated on a 5V supply directly. A 5.5 V shunt regulator is available internally for operation on higher supply voltage ; in this case an external limiting resistor is required.
Without the external limiting resistor care must be taken to ensure that the supply voltage does not exceed 5.5V or the regulator will intervene and the device could be damaged.

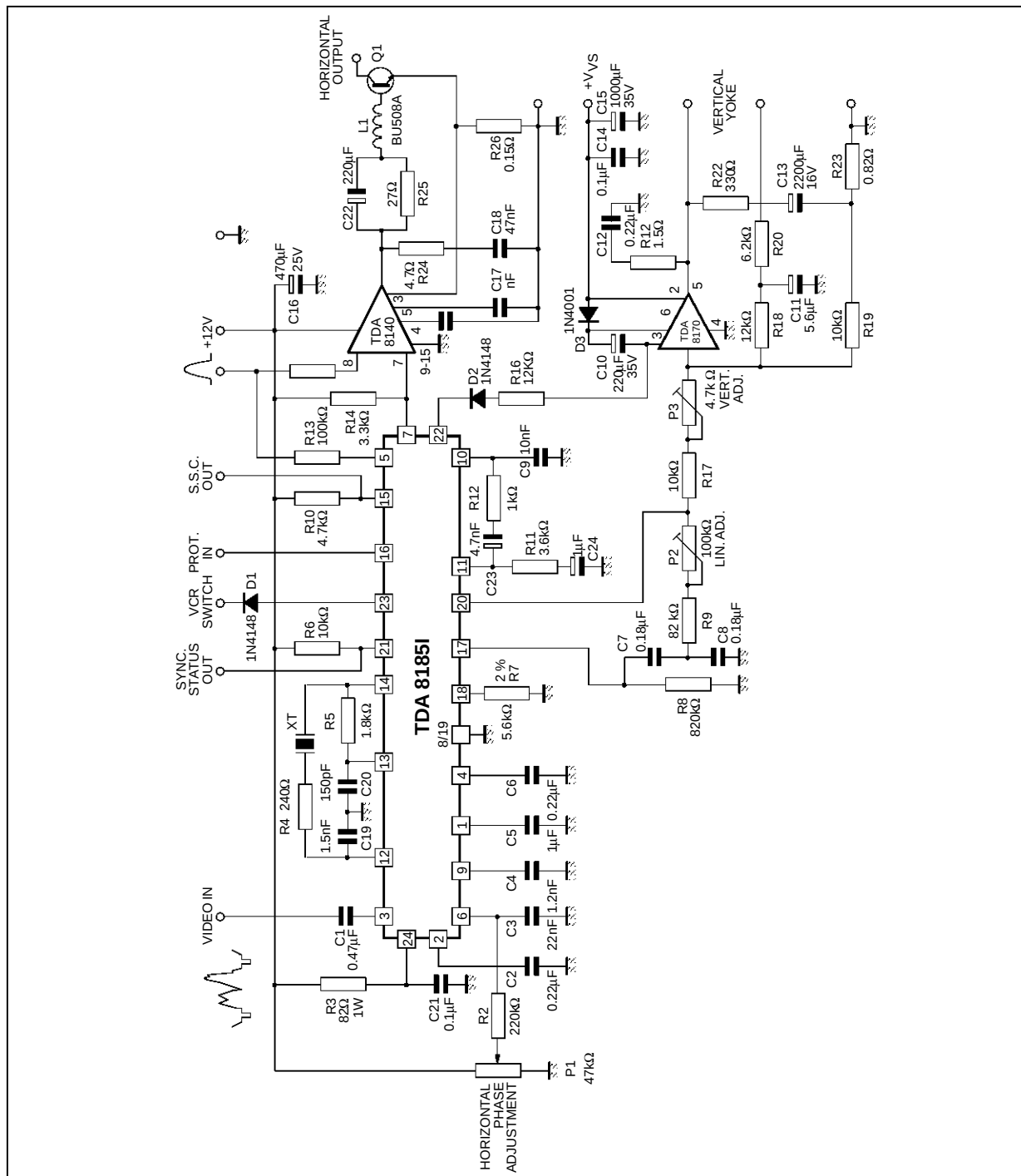
8185I-04.TBL

Figure 1 : Horizontal and Vertical Deflections for 30AX C.R.T.

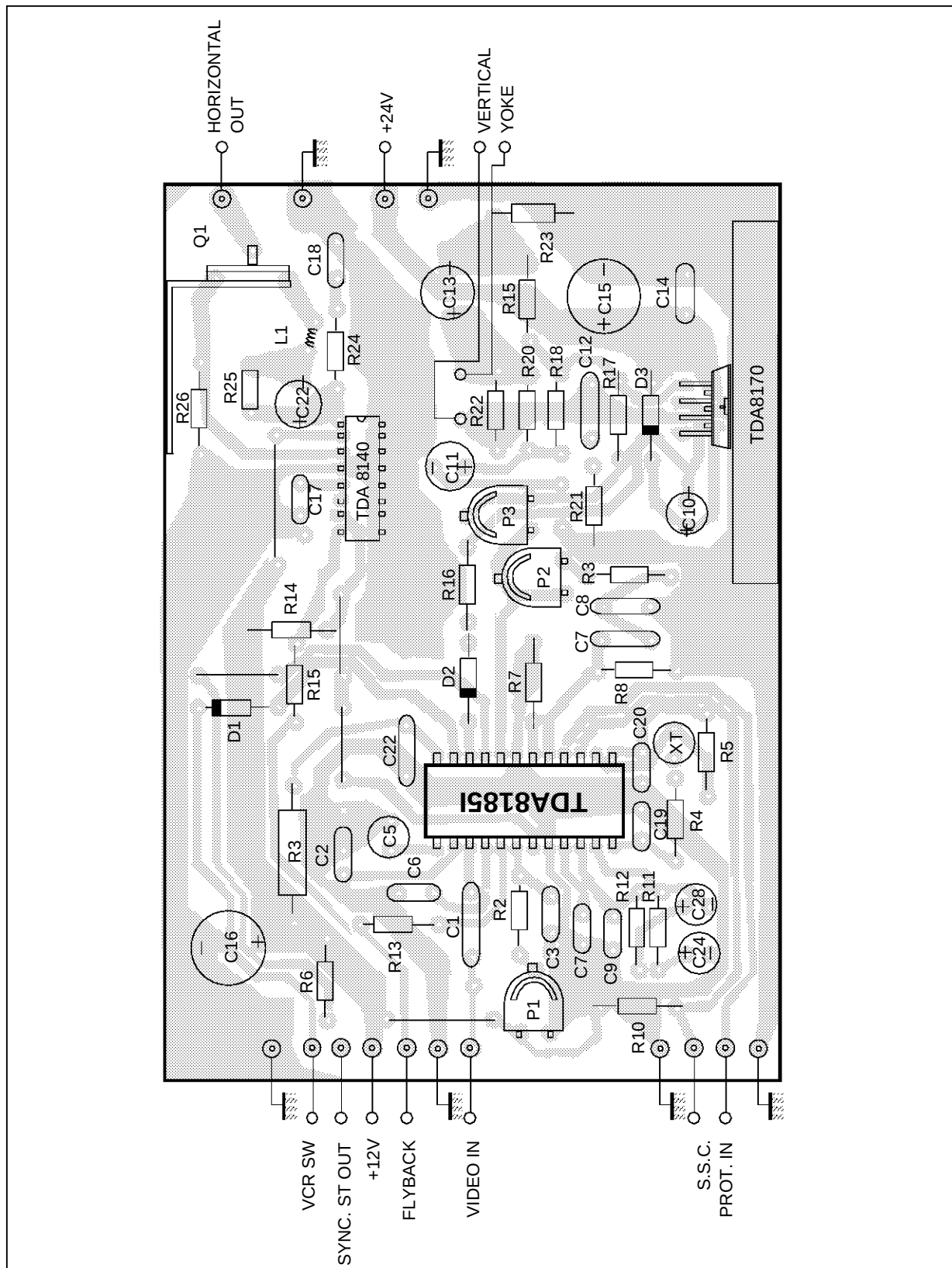


8185I-03.EPS

Figure 2 : Horizontal and Vertical Deflections for S4 C.R.T.



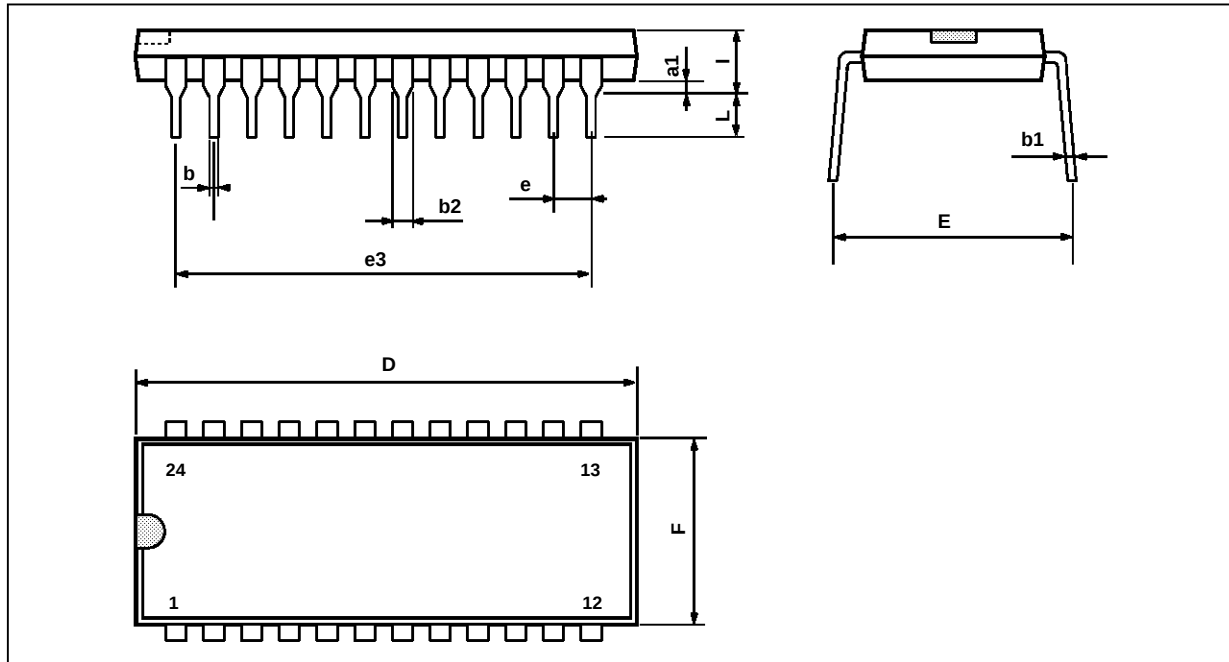
8185I-04 EPS

Figure 3 : P.C. Board and Components Layout of the Circuit of Figure 2 (1 : 1 scale)

8185I-05 EPS

PACKAGE MECHANICAL DATA

24 PINS - PLASTIC DIP



PM-DIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP24.TBL

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