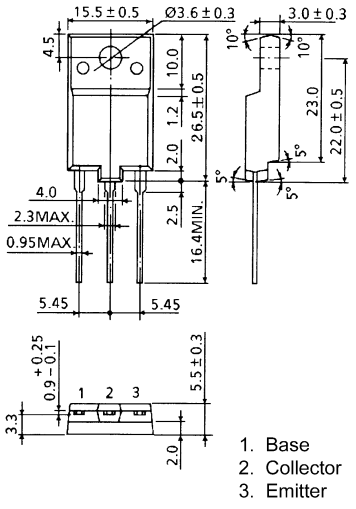
TOSHIBA TRANSISTOR SILICON NPN TRIPLE DIFFUSED MESA TYPE

2SC5855

HORIZONTAL DEFLECTION OUTPUT FOR SUPER HIGH RESOLUTION DISPLAY, COLOR TV, DIGITAL TV HIGH SPEED SWITCHING APPLICATIONS

- High Voltage : V_{CBO} = 1500 V
- Low Saturation Voltage : $V_{CE\ (sat)}$ = 3 V (max)
- High Speed : $t_{f(2)}$ = 0.1 μs (typ.)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-16E3A

Weight: 5.5 g (typ.)

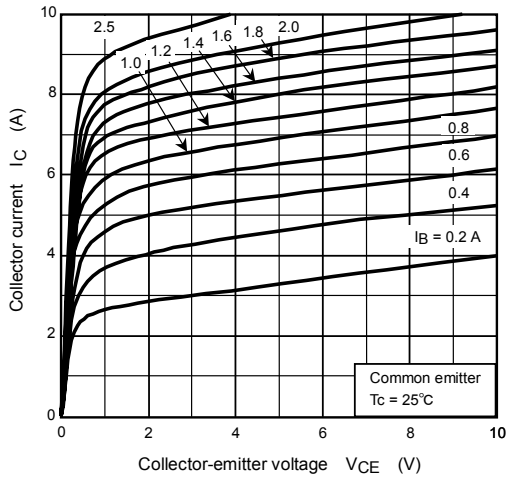
MAXIMUM RATINGS (Tc = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector−Base Voltage		V_{CBO}	1500	V
Collector−Emitter Voltage		V_{CEO}	700	V
Emitter−Base Voltage		V_{EBO}	5	V
Collector Current	DC	I_C	10	A
	Pulse	I_{CP}	20	
Base Current		I_B	5	A
Collector Power Dissipation		P_C	50	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

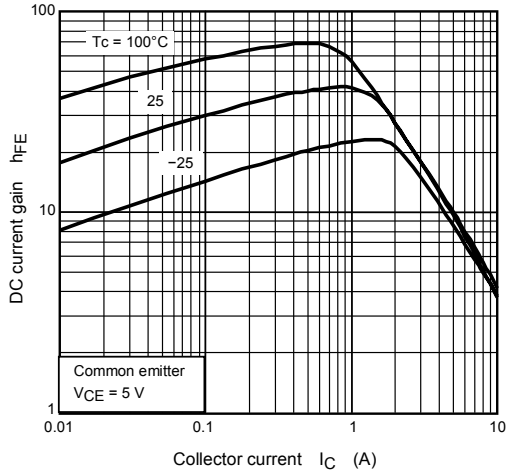
ELECTRICAL CHARACTERISTICS (Tc = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	Min	Typ.	Max	UNIT
Collector Cut−off Current		I_{CBO}	V_{CB} = 1500 V, I_E = 0	—	—	1	mA
Emitter Cut−off Current		I_{EBO}	V_{EB} = 5 V, I_C = 0	—	—	100	μA
Collector − Emitter Breakdown Voltage		$V_{(BR)\ CEO}$	I_C = 10 mA, I_B = 0	700	—	—	V
DC Current Gain		$h_{FE\ (1)}$	V_{CE} = 5 V, I_C = 1 A	28	—	60	—
		$h_{FE\ (2)}$	V_{CE} = 5 V, I_C = 6 A	6.2	—	10	
		$h_{FE\ (3)}$	V_{CE} = 5 V, I_C = 8 A	4.3	—	6.7	
Collector−Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 8 A, I_B = 2 A	—	—	3	V
Base−Emitter Saturation Voltage		$V_{BE\ (sat)}$	I_C = 8 A, I_B = 2 A	—	1.0	1.4	V
Transition Frequency		f_T	V_{CE} = 10 V, I_C = 0.1 A	—	2	—	MHz
Collector Output Capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	—	120	—	pF
Switching Time	Storage Time	$t_{stg(1)}$	I_{CP} = 6 , I_{B1} (end) = 0.8 A f_H = 32 kHz	—	2.8	—	μs
	Fall Time	$t_{f(1)}$		—	0.2	—	
	Storage Time	$t_{stg(2)}$	I_{CP} = 5.5 A, I_{B1} (end) = 0.8 A f_H = 80 kHz	—	2.3	—	μs
	Fall Time	$t_{f(2)}$		—	0.1	—	

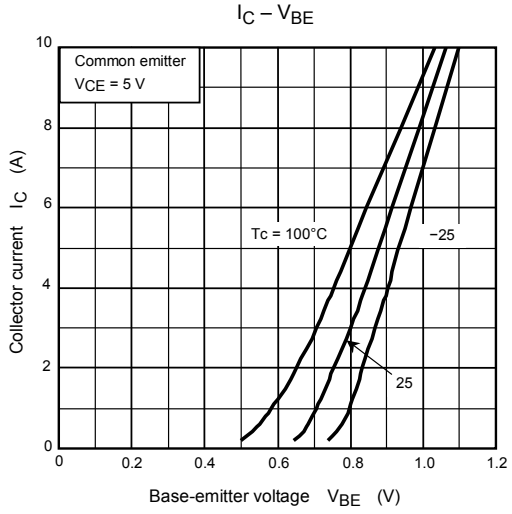
$I_C - V_{CE}$



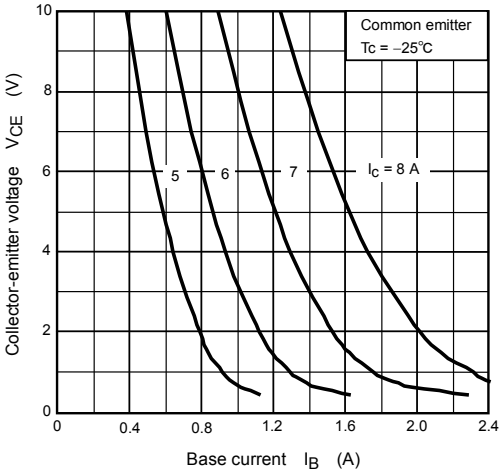
$h_{FE} - I_C$



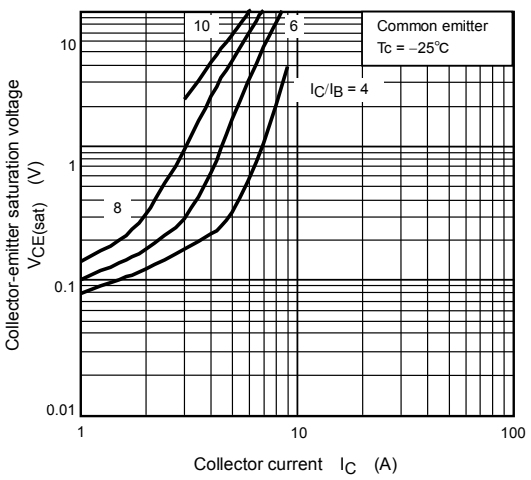
$I_C - V_{BE}$



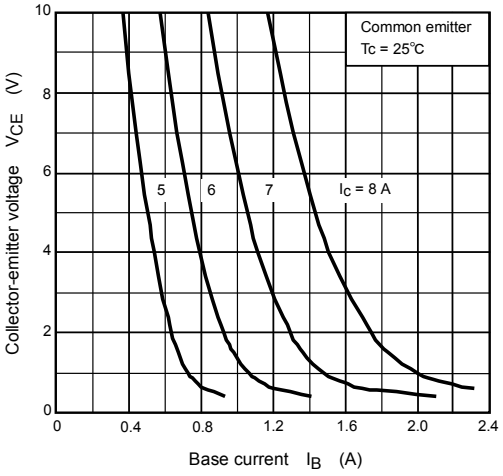
$V_{CE} - I_B$



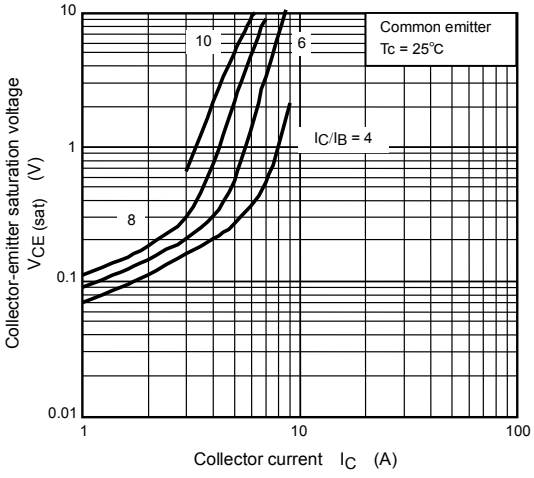
$V_{CE(sat)} - I_C$



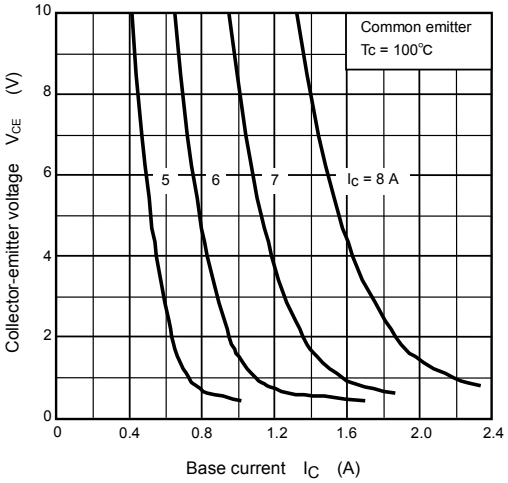
$V_{CE} - I_B$



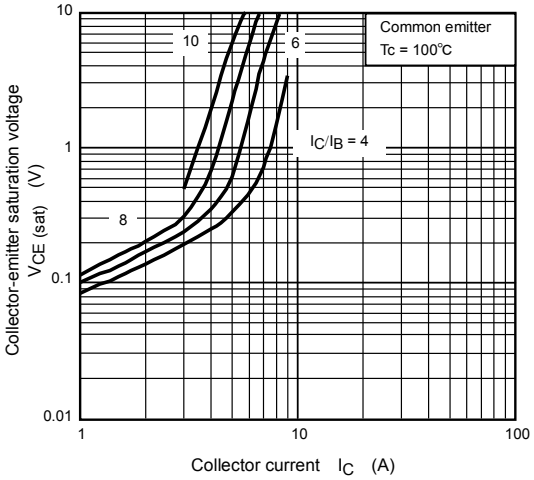
$V_{CE\ (sat)} - I_C$



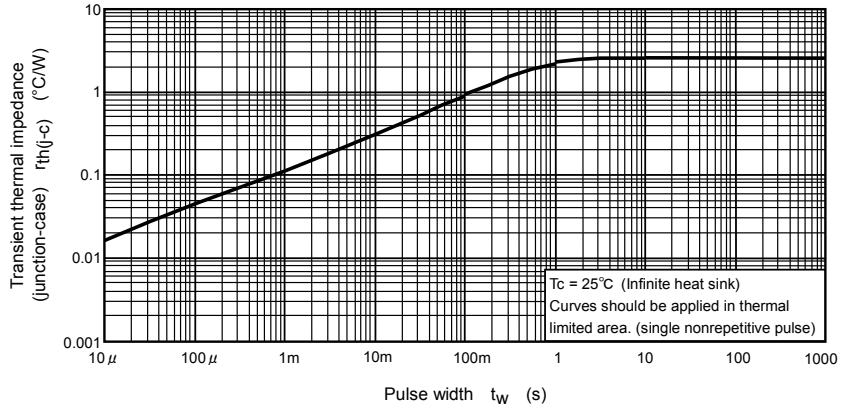
$V_{CE} - I_B$



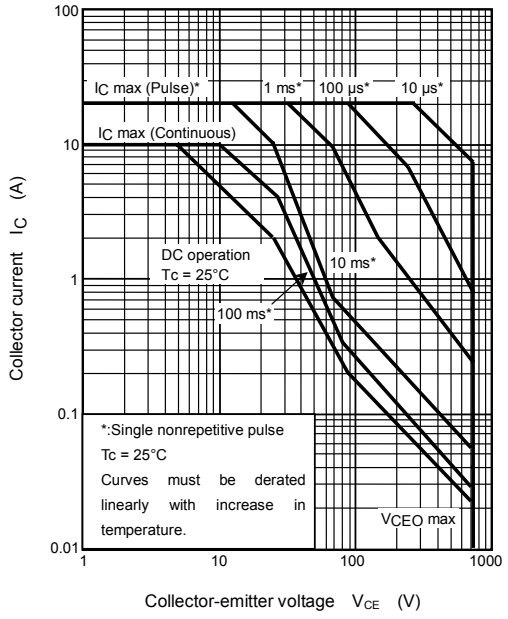
$V_{CE\ (sat)} - I_C$



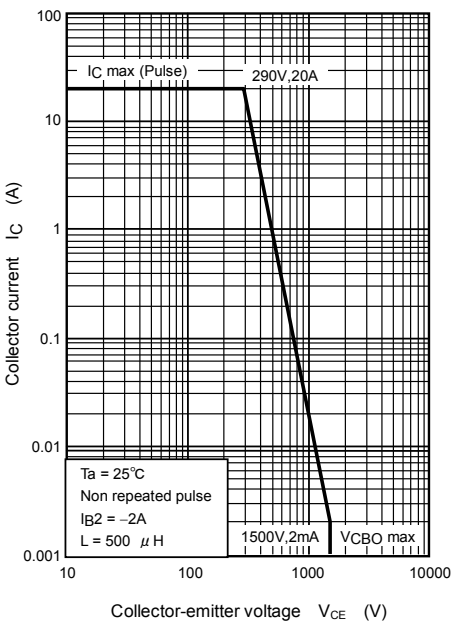
$r_{th(j-c)} - t_w$



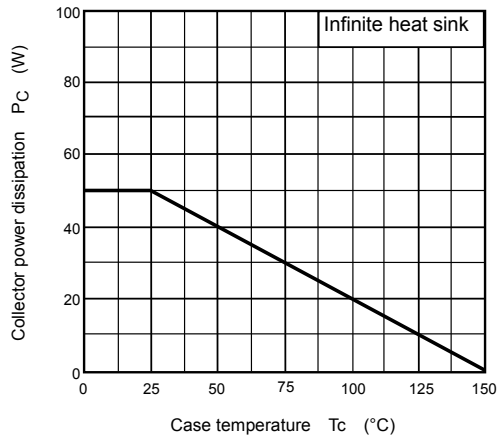
Safe Operating Area



Reverse Bias – Safe Operating Area



$P_C - Tc$



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