DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

2SK3481

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3481 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

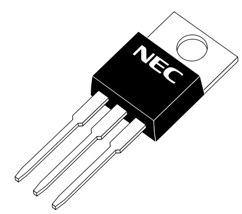
- Super low on-state resistance:
  $R_{DS(on)1}$ = 50 mΩ MAX. (V_{GS} = 10 V, I_D = 15 A)
  $R_{DS(on)2}$ = 58 mΩ MAX. (V_{GS} = 4.5 V, I_D = 15 A)
- Low C_{iss}: C_{iss} = 2300 pF TYP.
- Built-in gate protection diode

ORDERING INFORMATION

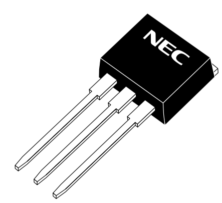
PART NUMBER	PACKAGE
2SK3481	TO-220AB
2SK3481-S	TO-262
2SK3481-ZJ	TO-263
2SK3481-Z	TO-220SMD [Note]

Note TO-220SMD package is produced only in Japan.

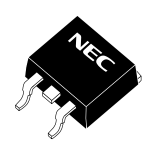
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	100	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±30	A
Drain Current (pulse) [Note1]	$I_{D(pulse)}$	±60	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	56	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current [Note2]	I_{AS}	26	A
Single Avalanche Energy [Note2]	E_{AS}	68	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 50 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.23	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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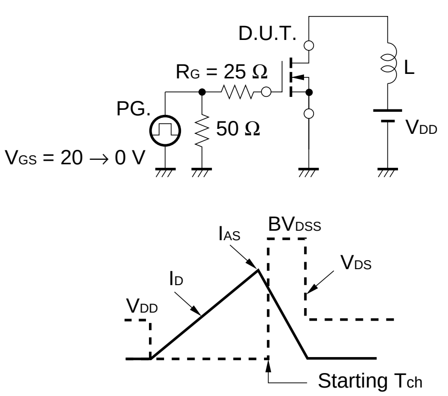
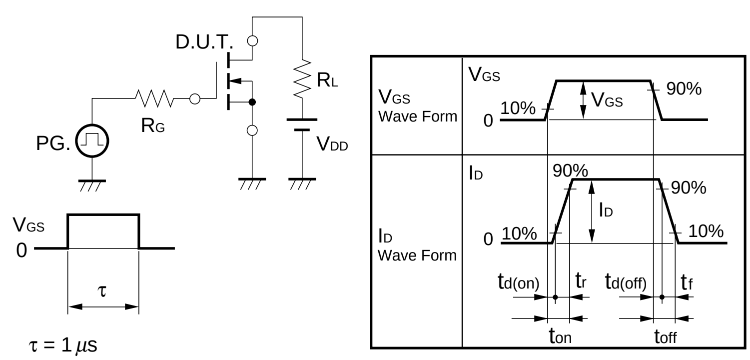
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 15 A	9	18		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 15 A		40	50	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 15 A		44	58	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		2300		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		230		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		120		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 15 A		13		ns
Rise Time	t_r	V_{GS} = 10 V		10		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		53		ns
Fall Time	t_f			5.0		ns
Total Gate Charge	Q_G	V_{DD} = 80 V		48		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		7.0		nC
Gate to Drain Charge	Q_{GD}	I_D = 30 A		12		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 30 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 30 A, V_{GS} = 0 V		70		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/ μs		160		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

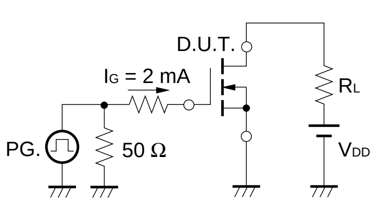


TEST CIRCUIT 2 SWITCHING TIME

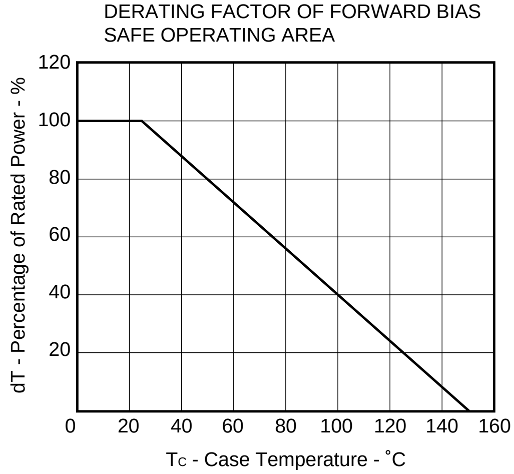


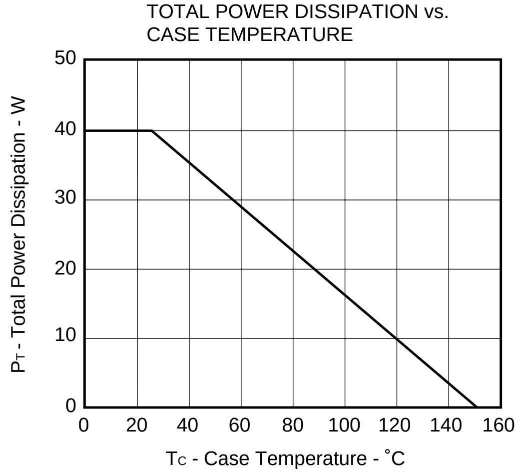
τ = 1 μs
Duty Cycle ≤ 1%

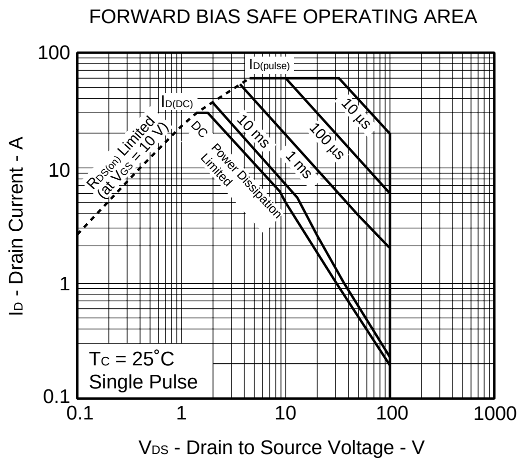
TEST CIRCUIT 3 GATE CHARGE

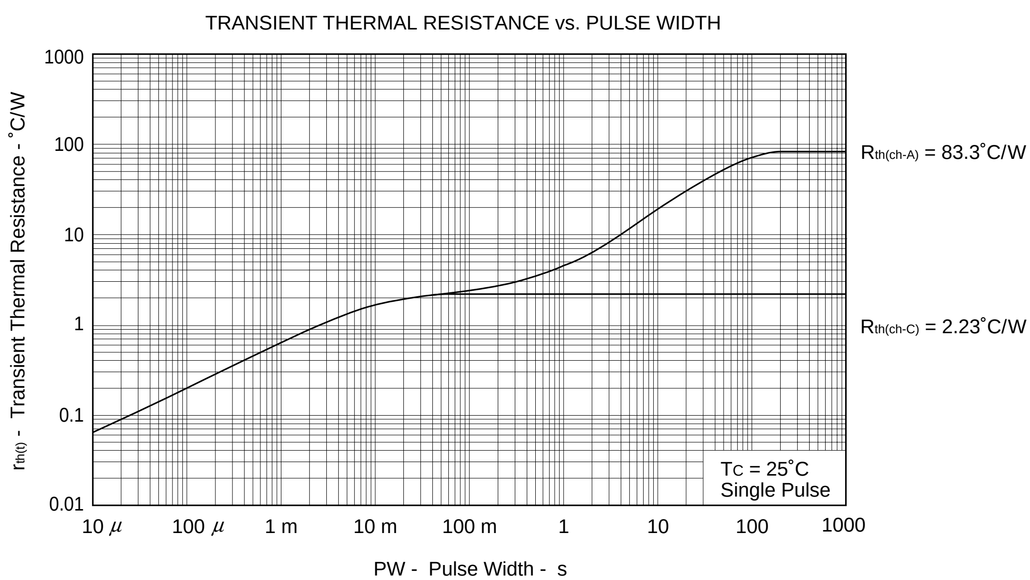


TYPICAL CHARACTERISTICS (T_A = 25°C)

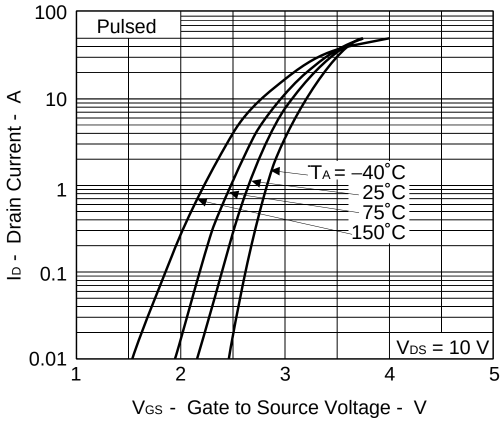




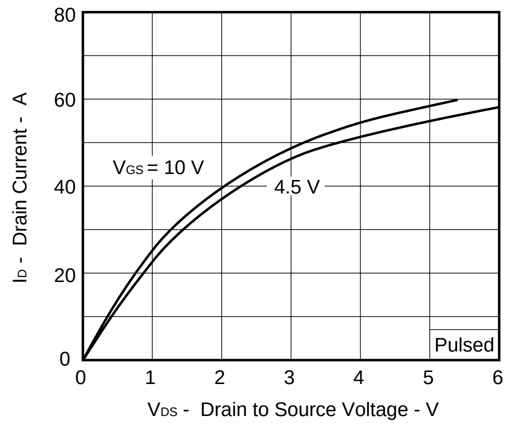




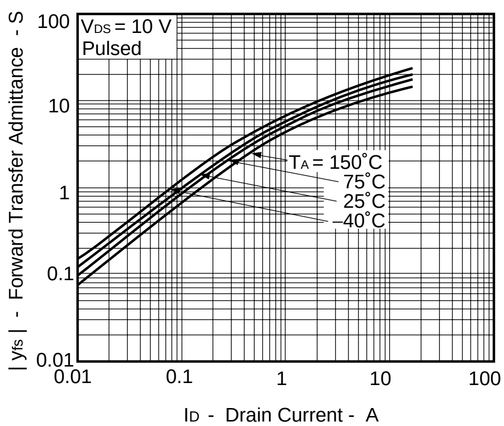
FORWARD TRANSFER CHARACTERISTICS



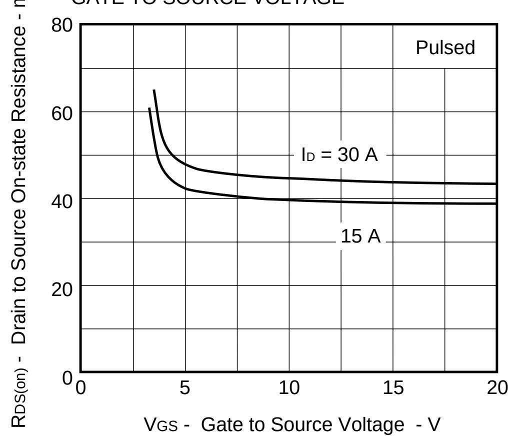
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



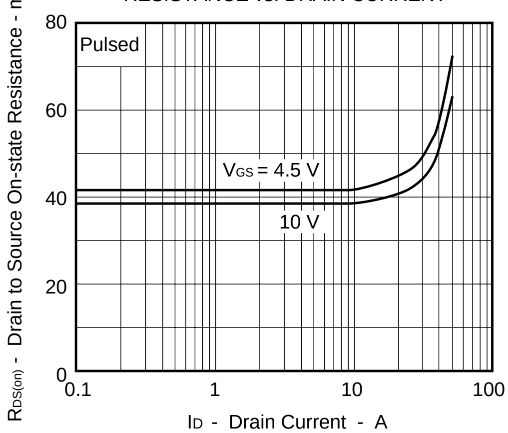
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



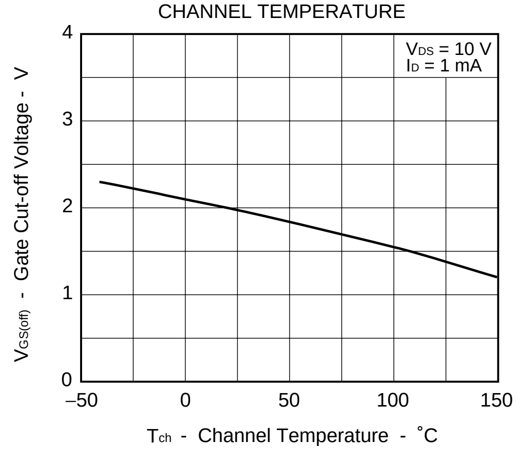
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



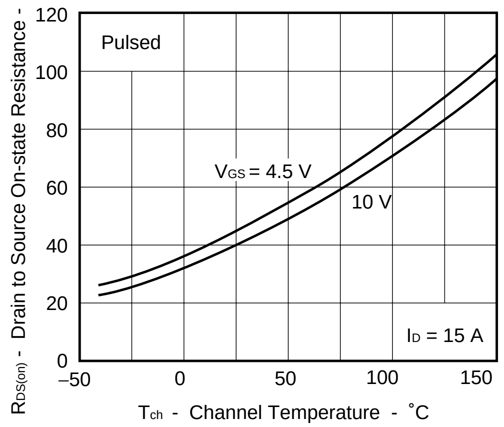
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



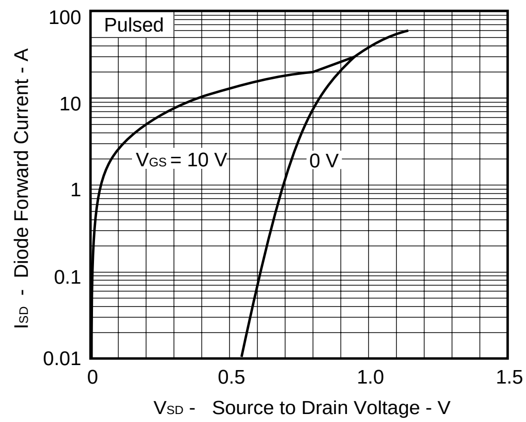
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



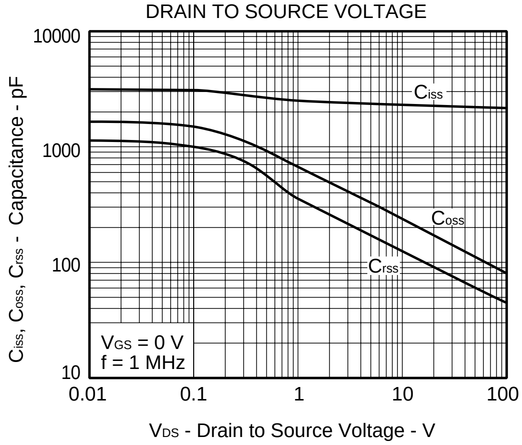
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



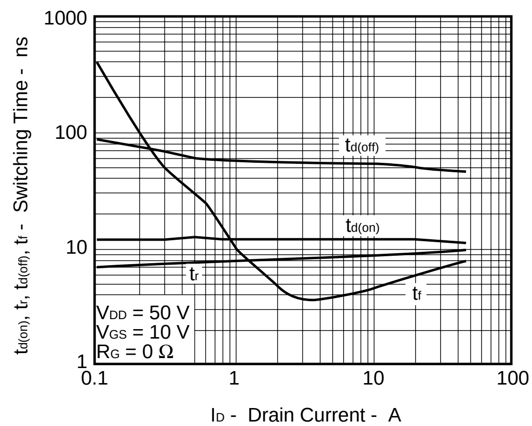
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



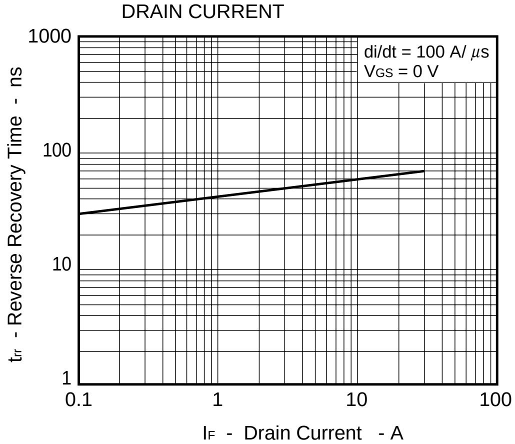
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



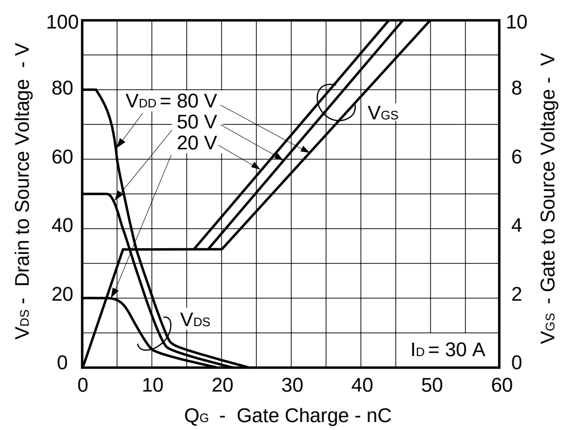
SWITCHING CHARACTERISTICS



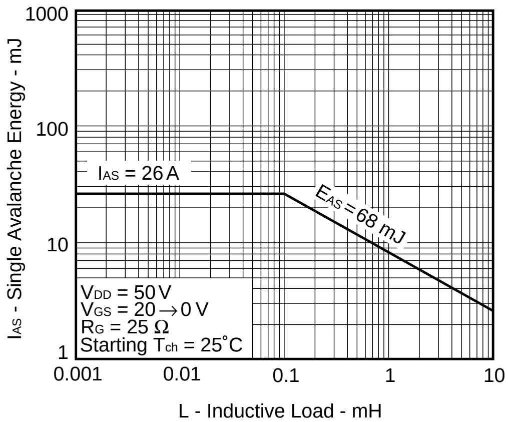
REVERSE RECOVERY TIME vs. DRAIN CURRENT



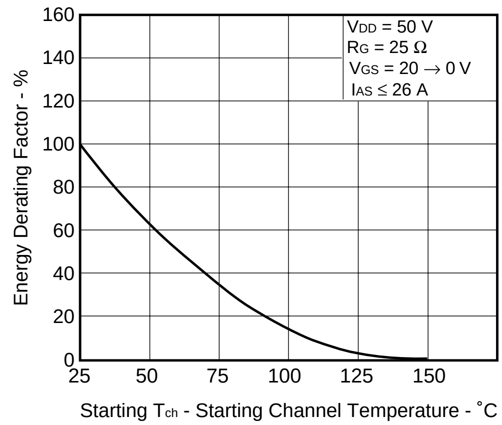
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

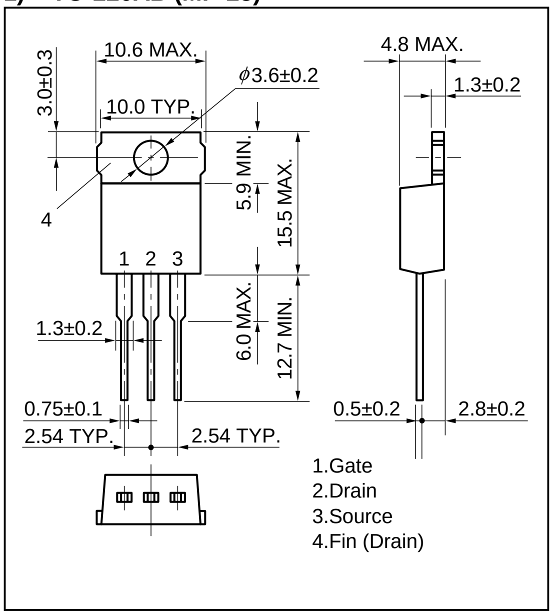


SINGLE AVALANCHE ENERGY DERATING FACTOR

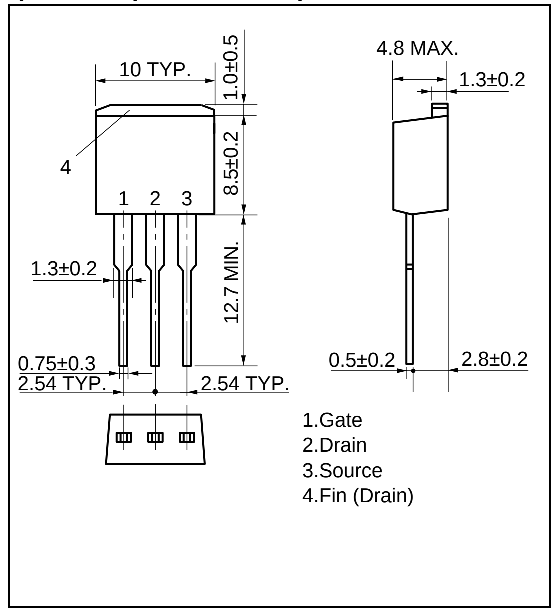


PACKAGE DRAWINGS (Unit: mm)

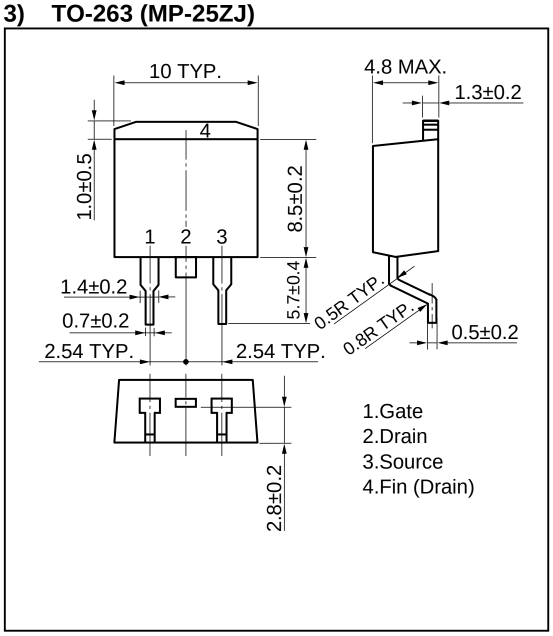
1) **TO-220AB (MP-25)**



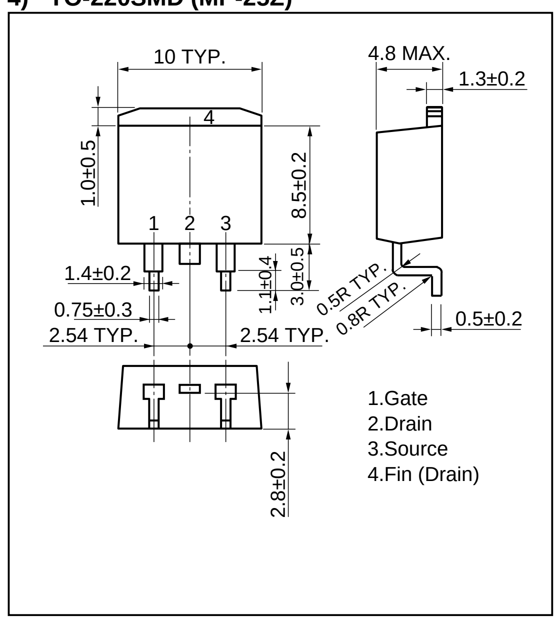
2) **TO-262 (MP-25 Fin Cut)**



3) **TO-263 (MP-25ZJ)**

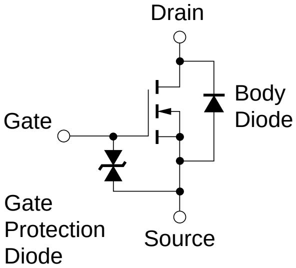


4) **TO-220SMD (MP-25Z)**Note



Note This package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.