

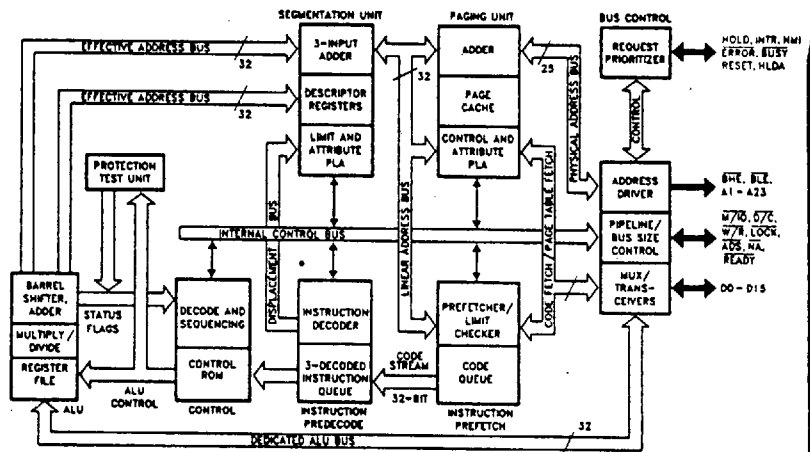
# Radiation Hardened 80386DXRP

High Speed CMOS  
32-Bit Microproces-  
sor

## For Space Applica- tions

SEI's 80386DXRP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® pack-

aging technology, the 80386DXRP is fully equivalent to the commercial 80386DX from Intel. This device is a 32-bit microprocessor which is designed for applications needing very high performance and optimized for multitasking operating systems. The 32-bit registers and data paths support 32-bit addresses and data types. The 80386DXRP addresses up to four gigabytes of physical memory and 64 terabytes of virtual memory. The architecture of this device includes address translation registers, advanced multitasking hardware, and a protection mechanism to support operating systems. Furthermore, this device also supports the simultaneous running of multiple operating systems. Capable of surviving space environments, the 80386DXRP is ideal for satellite, spacecraft, and space probe missions. SEI's RAD-PAK® advanced technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. This device provides a total dose survivability of greater than 100 krad(Si). It is available in Class S packaging and screening.



SPACE  
ELECTRONICS  
INCORPORATED

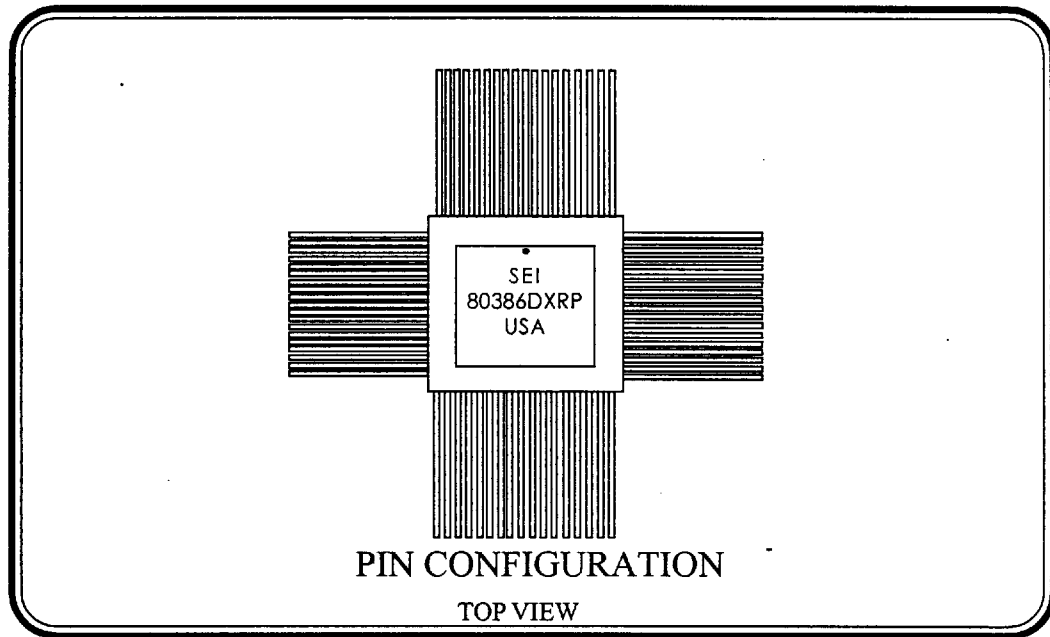
Tel: (619) 452-4167 Fax: (619) 452-5499  
INTERNET: 102005.1635@COMPUSERVE.COM

SEI  
80386DXRP  
32-BIT  
MICROPROCESSOR

# Radiation Hardened

## 80386DXRP

High Speed CMOS  
32-Bit Microprocessor



### Features

- Pin Compatible with Intel 80386DX
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- SEU Performance
  - LET Threshold = 6
  - Latchup Cross Section = 1E-5cm<sup>2</sup>
- Package:
  - 164 Pin RAD-PAK® quad flat pack (1.12 in. x 1.12 in.)
  - Weight – 12 grams
- High Speed CMOS IV Technology
- 8, 16, 32 Bit Data Types
- 8 General Purpose 32 Bit Registers
- Very Large Address Space
  - 4 Gigabyte Physical
  - 64 Terabyte Virtual
- 5 V Only Power
- Integrated Memory Management
  - On-Chip Paging Option
  - 4 Protection Modes
- Object Code Compatible with All 80X86 Microprocessors
- Optimal System Performance
  - Pipelined Instructions
  - 32 Mbytes/Sec Bandwidth
  - On-Chip Caches Support Address Translation
- Self Test Capability
- On-Chip Debugging Aides
- 11 Addressing Modes
- Class S Screening per TM 5004
- QCI per TM5005

Specifications and design are subject to change without notice.



Sept. 1995

For Further Information Contact:

**Space Electronics Inc.**

4031 Sorrento Valley Blvd., San Diego, CA 92121  
(619) 452-4167 Fax (619) 452-5499

**80386DXRP ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	$V_{CC}$	-0.5	6.5	V
Voltage, Any Pin		-0.5	$V_{CC}+0.5$	V
Storage Temperature	$T_s$	-65	+150	°C
Operating Temperature	$T_A$	-55	+125	°C

**80386DXRP DC ELECTRICAL CHARACTERISTICS<sup>1</sup>**

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Low Voltage	$V_{IL}$	-0.3	0.8	V
Input High Voltage	$V_{IH}$	2.0	$V_{CC}+0.3$	V
CLK2 Input Low Voltage	$V_{ILC}$	-0.3	0.8	V
CLK2 Input High Voltage	$V_{IHC}$	$V_{CC}-0.8$	$V_{CC}+0.3$	V
Output Low Voltage $I_{OL}=4mA, A2-A31, D0-D31$ $I_{OL}=5mA, BE0-BE3, WR, DC,$ MIO, LOCK, ADS, HLDA	$V_{OL}$		0.45 0.45	V V
Output High Voltage $I_{OL}=4mA, A2-A31, D0-D31$ $I_{OL}=5mA, BE0-BE3, WR, DC,$ MIO, LOCK, ADS, HLDA	$V_{OH}$	2.4 2.4		V V
Input Leakage Current (for all pins except BS16, PEREQ, BUSY, ERROR) $0V < V_{IN} < 5V$	$I_{IN}$	$\pm 15$		$\mu A$
Input Leakage Current (PEREQ pin) @ $V_{IH}=2.4V$	$I_{IH}$		200	$\mu A$
Input Leakage Current (BS16, BUSY, ERROR pins) $V_{IL}=0.45V$	$I_{IL}$		-400	$\mu A$
Output Leakage Current @ $.45 \leq V_{OUT} \leq 5V$	$I_{OL}$		$\pm 15$	$\mu A$
Supply Current	$I_{CC}$		460	mA
Input Capacitance <sup>2</sup> @ $f=1MHz$	$C_{IN}$		20	pF
Output Capacitance <sup>2</sup> @ $f=1MHz$	$C_{OUT}$		20	pF
CLK2 Capacitance <sup>2</sup> @ $f=1MHz$	$C_{CLK}$		20	pF



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SAN DIEGO, CA 92121  
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## Notes:

1.  $V_{CC}=4.75$  to  $5.25$  Volts;  $T_A=-55$  to  $+125$  °C.
2. Guaranteed by design.

80386DXRP AC ELECTRICAL CHARACTERISTICS<sup>1</sup>

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Frequency		4	16	MHz
CLK2 Period	$t_1$	31	125	ns
CLK2 High Time @ 2V	$t_{2a}$	9		ns
CLK2 High Time @ $V_{CC}-0.8V$	$t_{2b}$	7		ns
CLK2 Low Time @ 2V	$t_{3a}$	9		ns
CLK2 Low Time @ 0.8V	$t_{3b}$	7		ns
CLK2 Rise Time @ 0.8 to $V_{CC}-0.8V$	$t_r$		7	ns
CLK2 Fall Time @ $V_{CC}-0.8$ to 0.8V	$t_f$		7	ns
A2-A31 Valid Delay @ $C_L=120pF$	$t_6$	4	20	ns
A2-A31 Float Delay <sup>2</sup>	$t_7$	4	30	ns
BE0-BE3 Valid Delay @ $C_L=75pF$	$t_8$	4	24	ns
BE0-BE3, LOCK Float Delay <sup>2</sup>	$t_9$	4	30	ns
WR,MIO,DC,ADS Valid Delay @ $C_L=75pF$	$t_{10}$	6	19	ns
WR,MIO,DC,ADS Float Delay <sup>2</sup>	$t_{11}$	6	30	ns
D0-D31 Write Data Valid Delay @ $C_L=120pF$	$t_{12}$	8	27	ns
D0-D31 Write Data Float Delay <sup>2</sup>	$t_{13}$	4	22	ns
HLDA Valid Delay @ $C_L=75pF$	$t_{14}$	6	22	ns
NA Setup Time <sup>4</sup>	$t_{15}$	11		ns
NA Hold Time <sup>4</sup>	$t_{16}$	14		ns
BS16 Setup Time <sup>4</sup>	$t_{17}$	13		ns
BS16 Hold Time <sup>4</sup>	$t_{18}$	21		ns
READY Setup Time <sup>4</sup>	$t_{19}$	21		ns
READY Hold Time <sup>4</sup>	$t_{20}$	4		ns



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**80386DXRP AC ELECTRICAL CHARACTERISTICS<sup>1</sup> (Cont'd)**

PARAMETER	SYMBOL	MIN	MAX	UNIT
D0-D31 Read Setup Time <sup>4</sup>	$t_{21}$	11		ns
D0-D31 Read Hold Time <sup>4</sup>	$t_{22}$	6		ns
HOLD Setup Time <sup>4</sup>	$t_{23}$	26		ns
HOLD Hold Time <sup>4</sup>	$t_{24}$	5		ns
RESET Setup Time <sup>4</sup>	$t_{25}$	13		ns
RESET Hold Time <sup>4</sup>	$t_{26}$	4		ns
NMI, INTR Setup Time <sup>4,5</sup>	$t_{27}$	16		ns
NMI, INTR Hold Time <sup>4,5</sup>	$t_{28}$	16		ns
PEREQ, ERROR, BUSY Setup Time <sup>4,5</sup>	$t_{29}$	16		ns
PEREQ, ERROR, BUSY Hold Time <sup>4,5</sup>	$t_{30}$	5		ns

- Notes:
1.  $V_{CC}=4.75$  to  $5.25$  Volts;  $T_A=-55$  to  $+125$  °C.
  2. Float condition occurs when maximum output current becomes less than  $I_{LO}$  in magnitude.
  3. Guaranteed by design.
  4. Tested by application of the specific timing signal.
  5. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to assure recognition within a specific CLK2 period.

**80386RP Package Ordering Guide**

Package Style	Case Outline	1/	Description
Q	Q-164		164 Pin Quad Flat Package

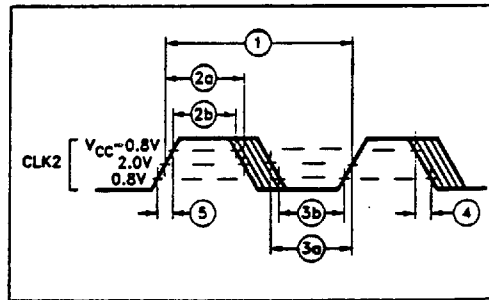
- Note:
- 1/ For outline information, see Appendix A (Package Information - Outline Dimension)



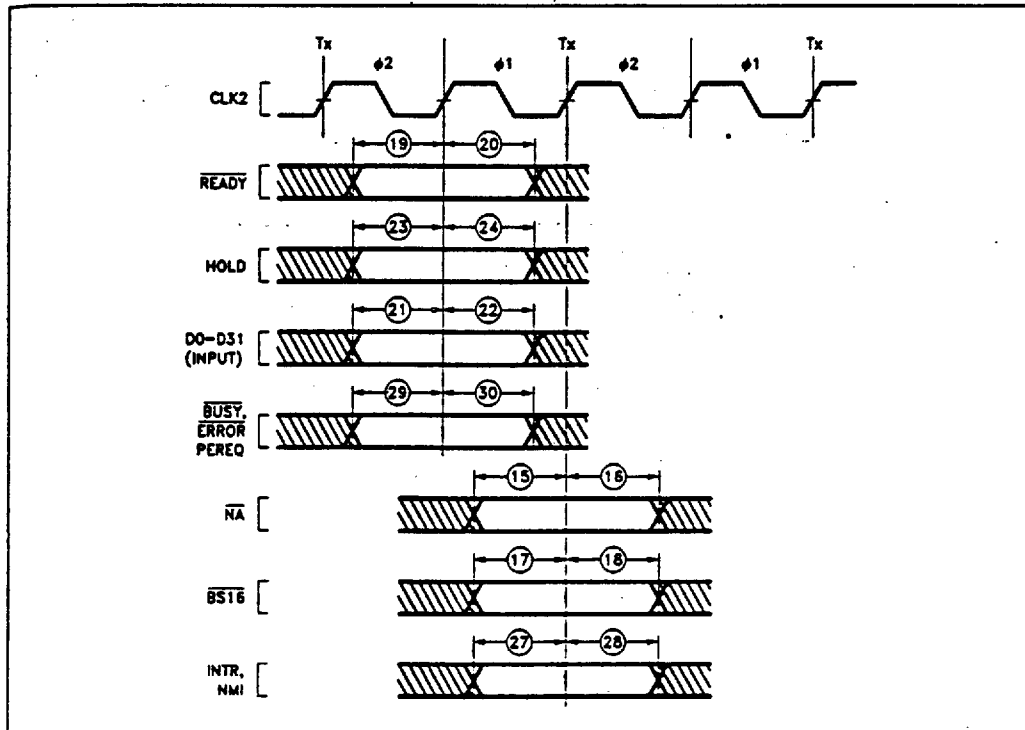
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### A.C. Timing Waveforms



CLK2 Timing

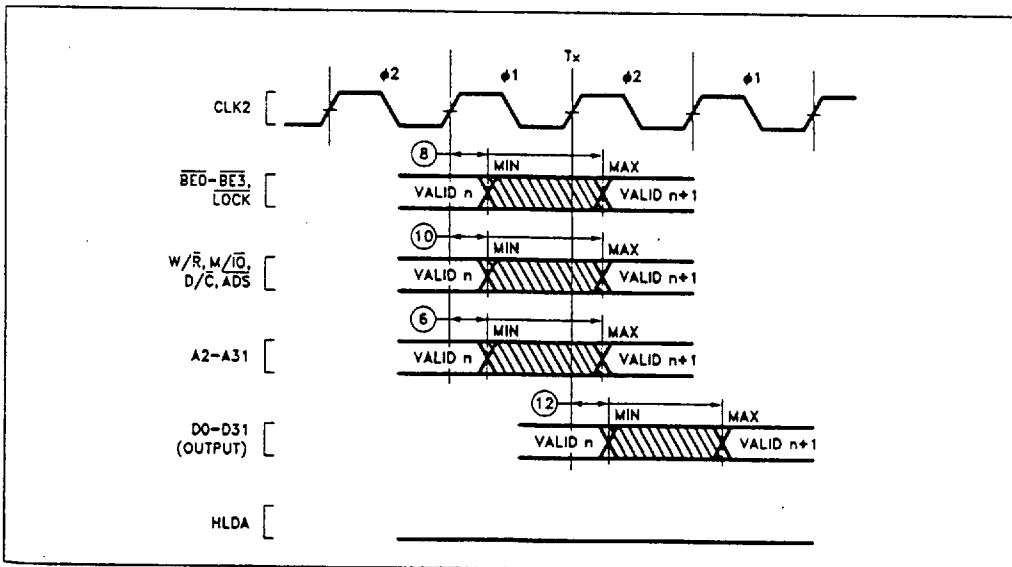


Input Setup and Hold Timing

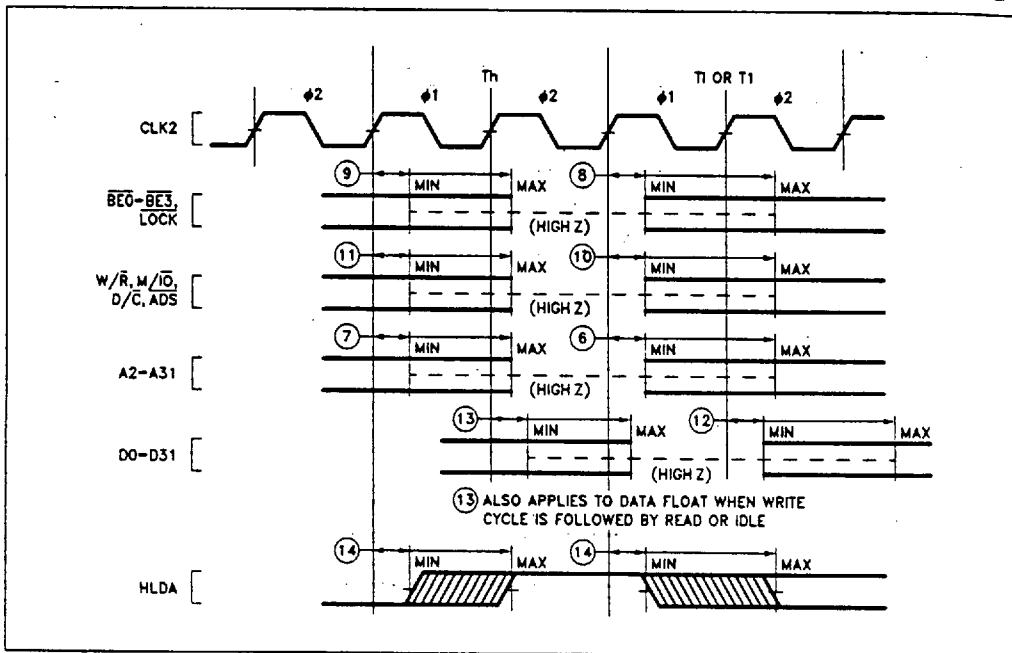


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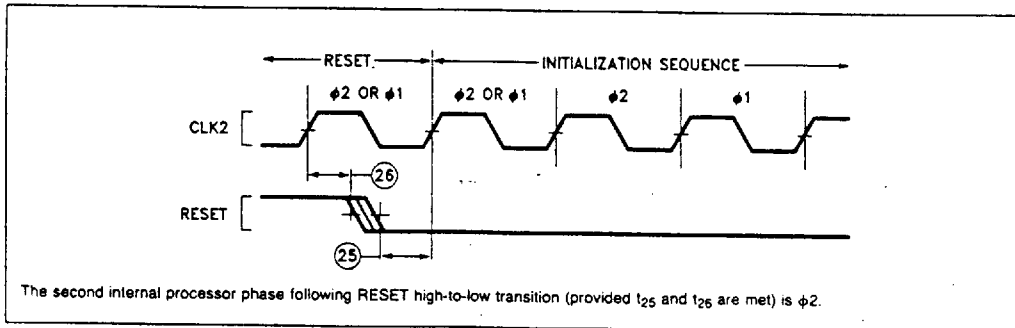
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Output Valid Delay Timing



Output Float Delay and HLDA Valid Delay Timing



The second internal processor phase following RESET high-to-low transition (provided  $t_{25}$  and  $t_{26}$  are met) is  $\phi 2$ .

RESET Setup and Hold Timing, and Internal Phase



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## 80386DXRP MICROPROCESSOR PINOUT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	A16	42	PEREQ	83	READY\	124	D19
2	A17	43	Vss	84	NC	125	NC
3	A15	44	Vcc	85	D1	126	NC
4	A14	45	ERROR\	86	NC	127	D24
5	A13	46	RESET	87	D2	128	D21
6	A12	47	NC	88	NC	129	NC
7	A11	48	NC	89	D4	130	NC
8	NC	49	BUSY\	90	D0	131	D25
9	A9	50	Vcc	91	Vcc	132	D23
10	A10	51	Vss	92	Vss	133	NC
11	Vss	52	Vcc	93	D6	134	NC
12	A7	53	Vss	94	D3	135	D27
13	A8	54	Vcc	95	Vss	136	D26
14	Vcc	55	Vss	96	Vcc	137	Vcc
15	Vss	56	Vcc	97	D8	138	Vss
16	A5	57	Vss	98	D5	139	D29
17	A6	58	Vcc	99	Vcc	140	D28
18	NC	59	LOCK\	100	Vss	141	Vcc
19	NC	60	W/R\	101	HLDA	142	Vss
20	A3	61	Vss	102	D7	143	D31
21	A4	62	Vcc	103	NC	144	D30
22	NC	63	M/IO\	104	D10	145	NC
23	NC	64	D/C\	105	D9	146	A31
24	A2	65	NC	106	NC	147	A30
25	NC	66	NC	107	NC	148	A29
26	Vcc	67	BE2\	108	D12	149	A28
27	Vss	68	NC	109	D11	150	Vcc
28	NC	69	Vcc	110	Vcc	151	Vss
29	NC	70	Vss	111	Vss	152	A27
30	NC	71	BE0\	112	D14	153	A26
31	Vcc	72	BE3\	113	D13	154	A25
32	Vss	73	NC	114	NC	155	NC
33	NC	74	BE1\	115	D15	156	A23
34	Vcc	75	NA\	116	D16	157	A24
35	Vss	76	NC	117	Vcc	158	A21
36	NC	77	NC	118	Vss	159	A22
37	INTR	78	BS16\	119	D18	160	NC
38	NC	79	HOLD	120	D17	161	A20
39	NC	80	CLK2	121	D20	162	A19
40	NC	81	ADS\	122	Vss	163	A18
41	NMI	82	NC	123	D22	164	NC



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