CMC7106 Low Power Operational Amplifier, RRIO, with Shutdown, SOT23-6

Features

- Tiny SOT23-6 package
- Guaranteed specs at 2.7V, 3V, and 5V
- Low supply current 0.3μA typ. operating. Less than 1μA idle.
- Rail-to-Rail Input and Output (RRIO)
- Simple shutdown mode (with logic level control) for power savings
- 1MHz gain-bandwidth
- Input common mode range includes V- and V+

Applications

- Test and Measurement Equipment
- Cellular Phones
- Portable Equipment
- Notebooks and PDAs
- Electronic Toys

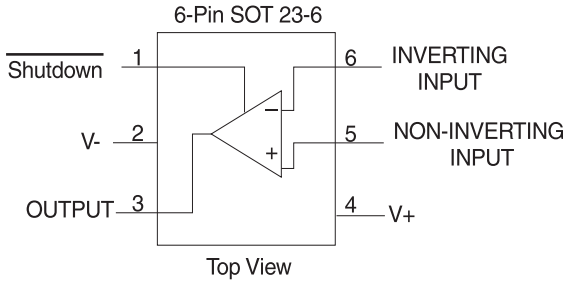
Product Description

The California Micro Devices CMC7106 is a high performance CMOS operational amplifier in a 6-pin SOT23-6 package. Operating with low supply current, it is ideal for battery operated applications where power, space, and weight are critical considerations.

Performance is similar to CAMD's CMC7101AY SOT Amp, with the addition of a shutdown pin to greatly reduce supply current when idle. The shutdown mode is controlled by an extra pin, and is compatible with most logic family signal levels.

Ideal for use in test and measurement equipment and personal electronics such as cellular handsets, pagers, cordless telephones, and other products with limited space and battery power.

CONNECTION DIAGRAM



STANDARD PART ORDERING INFORMATION

Package		Ordering Part Number	
Pins	Style	Tape & Reel	Part Marking
6	SOT23-6	CMC7106Y/R	7106

OPERATING CONDITIONS (unless specified otherwise)		
Parameter	**Rating**	**Units**
Supply Voltage	$2.7 \leq V+ \leq 7$	V
Junction Temperature Range	$-40 \leq T_J \leq +85$	°C
Thermal Resistance (θ_{JA})	325	°C / W

ABSOLUTE MAXIMUM RATINGS (Note 1)		
Parameter	**Rating**	**Units**
ESD Tolerance (see Note 2)	2,000	V
Differential Input Voltage	± Supply Voltage	V
Voltage at Input / Output Pin	(V+) + 0.3V, (V-) -0.3V	V
Supply Voltage (V+ to V-)	7.5	V
Current at Input Pin	5	mA
Current at Output Pin (see Note 3)	35	mA
Current at Power Supply Pin	35	mA
Lead Temperature (soldering, 10 sec.)	260	°C
Storage Temperature Range (T_J)	-65 to +150	°C
Junction Temperature (see Note 4)	150	°C

Note 1 Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate ratings for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Operating Characteristics.

Note 2 Human body model, 1.5KΩ in series with 100pF.

Note 3 Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperatures can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4 The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $PD = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly to a PC board.

2.7V ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, all limits guaranteed for T_J=25°C, V+ =2.7V, V- = 0V, R_L > 1MΩ

Symbol	Parameter	Conditions	TYP	LIMIT	UNIT
V_{OS}	Input Offset Voltage		0.11	6	mV
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.50		pA
R_{IN}	Input Resistance		1		TΩ
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$	70	55	dB
V_{CM}	Input Common Mode Range		0	0	V
			3.0	2.7	V
PSRR	Power Supply Rejection Ratio	V+ = 1.35V to 1.65V V- = -1.35V to -1.65V V_{CM} = 0	60	50	dB
C_{IN}	Common-Mode Input Capacitance		3		pf
V_O	Output Swing	R_L = 600Ω	2.60		V
			0.10		V
		R_L = 2KΩ	2.60	2.15	V
			0.10	0.50	V
		R_L = 10KΩ	2.68	2.64	V
			0.02	0.06	V
I_S	Supply Current	Amplfier "On", V_{SD} = 2.7V	300	810	µA
I_S	Supply Current	Amplfier "Off", V_{SD} = 0V		1	µA
V_{SDIH}	Amplfier On Logic Level	Amplfier "On"		2.0	V
V_{SDIL}	Amplfier Off Logic Level	Amplfier "Off"		1.0	V
I_{IN}	Logic Pin Current	V_{SD} = V+ or GND		1.0	µA
SR	Slew Rate		0.70		V/µs
GBW	Gain Bandwidth Product		0.60		MHz

3V ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, all limits guaranteed for T_J=25°C, V+ =3V, V- = 0V, R_L > 1MΩ

Symbol	Parameter	Conditions	TYP	LIMIT	UNIT
V_{OS}	Input Offset Voltage		0.11	4	mV
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/ºC
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.50		pA
R_{IN}	Input Resistance		1		TΩ
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 3V$		55	dB
V_{CM}	Input Common Mode Range		-0.30	0	V
		For CMRR > 50dB	3.30	3.0	V
PSRR	Power Supply Rejection Ratio	V+ = 1.5V to 1.8V V- = -1.5V to -1.8V V_{CM} = 0	80	68	dB
C_{IN}	Common-Mode Input Capacitance		3		pf
V_O	Output Swing	R_L = 600Ω	2.90	2.60	V
			0.10	0.40	V
		R_L = 2KΩ	2.90	2.60	V
			0.10	0.40	V
		R_L = 10KΩ	2.99	2.70	V
			0.01	0.30	V
I_S	Supply Current	Amplfier "On", V_{SD} = 3.0V	300	810	µA
I_S	Supply Current	Amplfier "Off", V_{SD} = 0V		1	µA
V_{SDIH}	Amplfier On Logic Level	Amplfier "On"		2.0	V
V_{SDIL}	Amplfier Off Logic Level	Amplfier "Off"		1.0	V
I_{IN}	Logic Pin Current	V_{SD} = V+ or GND		1.0	µA
SR	Slew Rate		0.70		V/µs
GBW	Gain Bandwidth Product		0.60		MHz

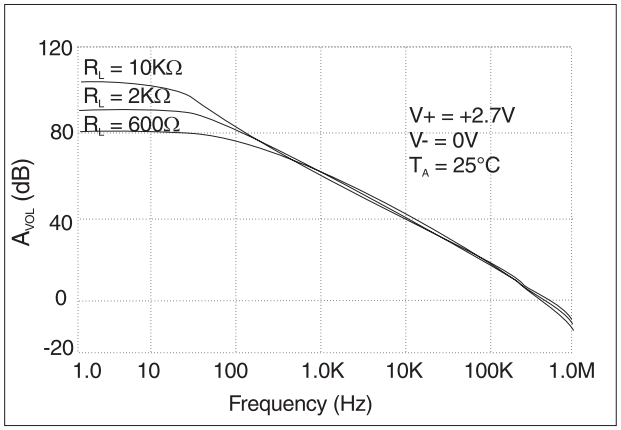
5V ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, all limits guaranteed for T_J=25°C, V+ =5V, V- = 0V, R_L > 1MΩ

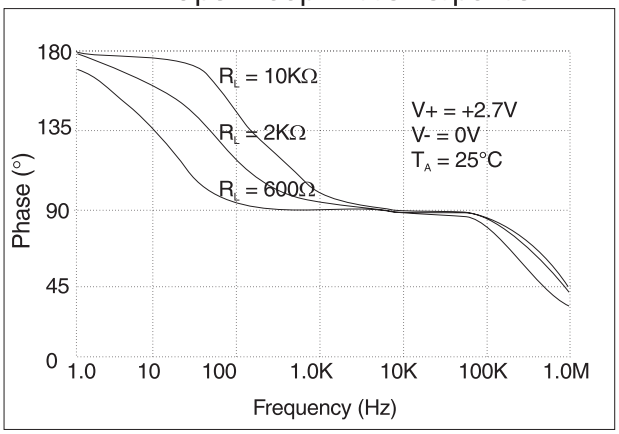
Symbol	Parameter	Conditions	TYP	LIMIT	UNIT
V_{OS}	Input Offset Voltage		0.11	3	mV
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.50		pA
R_{IN}	Input Resistance		1		TΩ
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	82	55	dB
V_{CM}	Input Common Mode Range		-0.30		V
		For CMRR > 50dB	5.30		V
PSRR	Power Supply Rejection Ratio	V+ = 2.5V to 2.8V V- = -2.5V to -2.8V V_{CM} = 0	82	70	dB
C_{IN}	Common-Mode Input Capacitance		3		pf
V_O	Output Swing	R_L = 600Ω	4.90	4.50	V
			0.10	0.50	V
		R_L = 2KΩ	4.90	4.70	V
			0.10	0.18	V
		R_L = 10KΩ	4.99	4.80	V
			0.01	0.15	V
I_{SC}	Output Short Circuit Current	Sourcing V_0 = 0V (see Note 3)	100	16	mA
		Sinking V_0 = 5V (see Note 3)	80	11	mA
I_S	Supply Current	Amplfier "On", V_{SD} = 5.0V	300	810	µA
I_S	Supply Current	Amplfier "Off", V_{SD} = 0V		1	µA
V_{SDIH}	Amplfier On Logic Level	Amplfier "On"		4.0	V
V_{SDIL}	Amplfier Off Logic Level	Amplfier "Off"		1.0	V
I_{IN}	Logic Pin Current	V_{SD} = V+ or GND		1.0	µA
T.H.D.	Total Harmonic Distortion	f = 10kHz, Av = -2 R_L = 10kΩ, Vo = 4.0pp	0.01		%
SR	Slew Rate		1		V/µs
GBW	Gain Bandwidth Product		1		MHz
t_{ON}	Turn On Time	Av = +1, RL = 10KΩ	5		µs
t_{OFF}	Turn Off Time	Av = +1, RL = 10KΩ	2		µs

TYPICAL PERFORMANCE CHARACTERISTICS

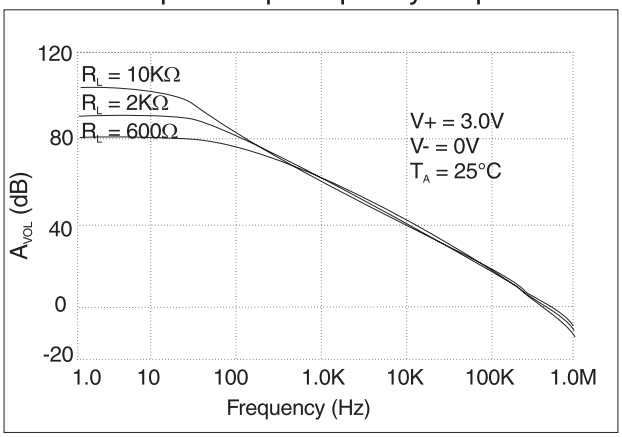
2.7V Open Loop Frequency Response



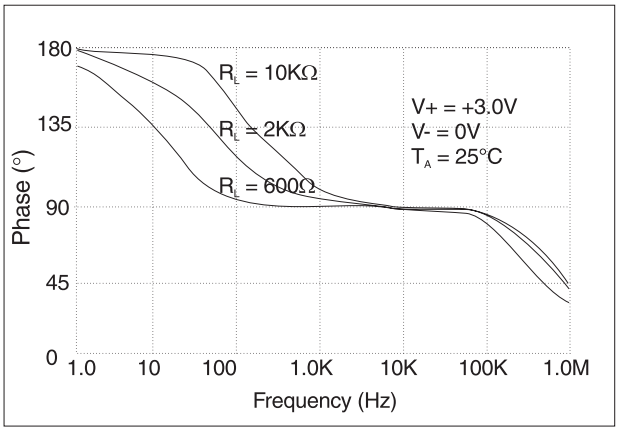
2.7V Open Loop Phase Response



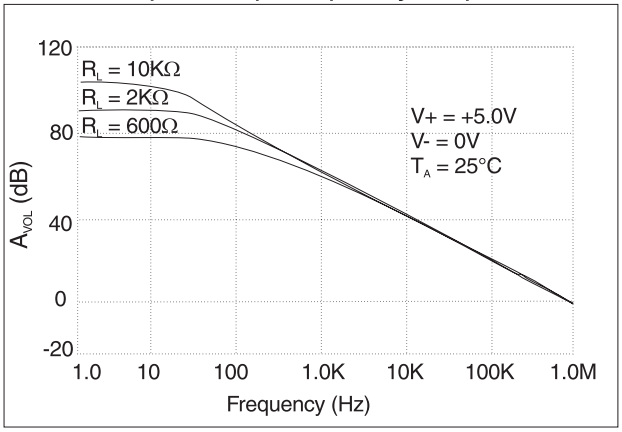
3V Open Loop Frequency Response



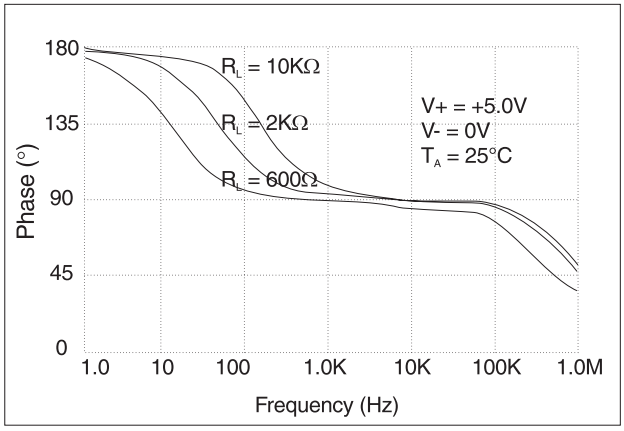
3V Open Loop Phase Response



5V Open Loop Frequency Response

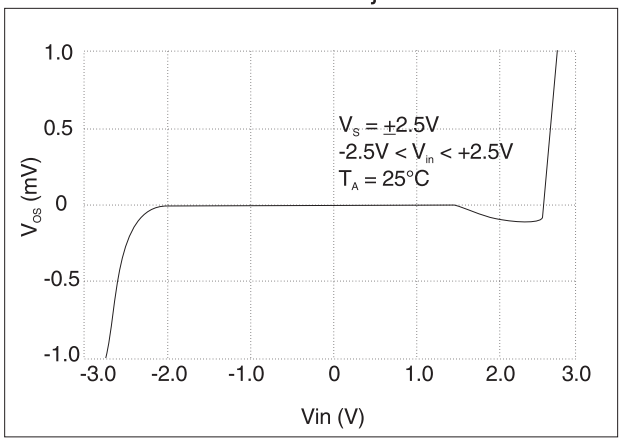


5V Open Loop Phase Response

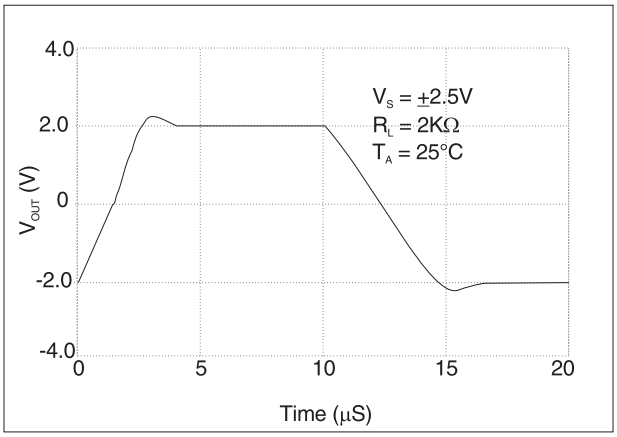


TYPICAL PERFORMANCE CHARACTERISTICS

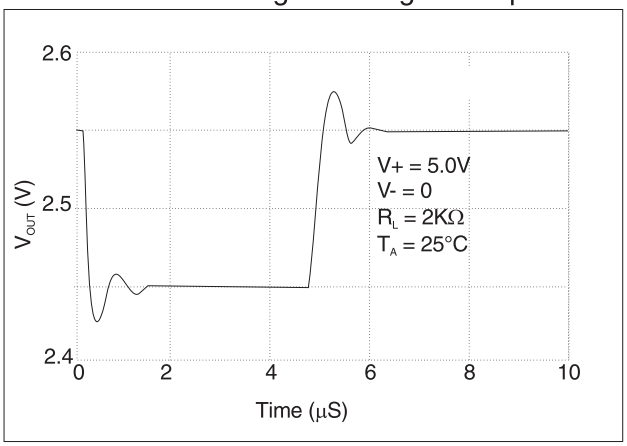
5V Common Mode Rejection Ratio



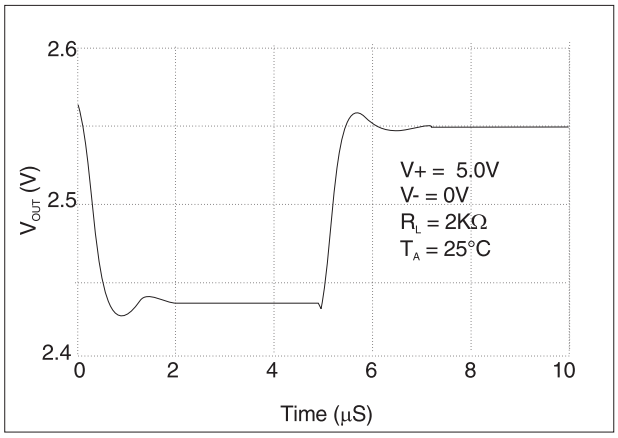
5V Large Signal Pulse Response



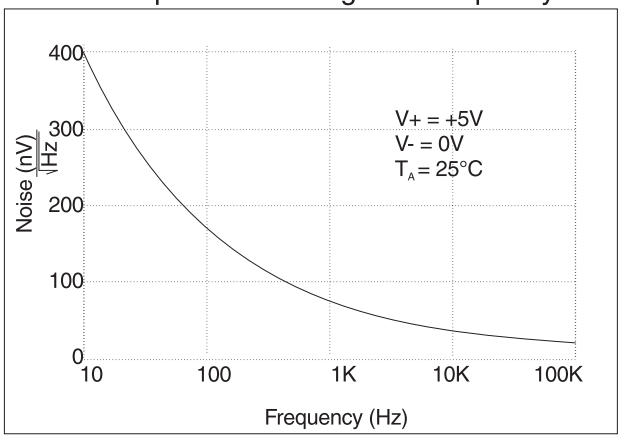
5V Non Inverting Small Signal Response



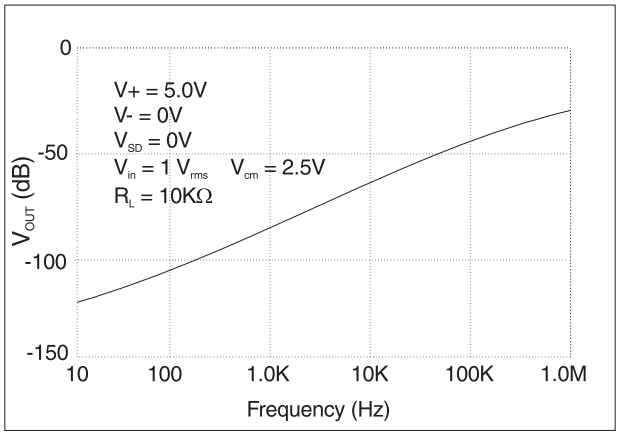
5V Inverting Small Signal Response



5V Input Noise Voltage Vs. Frequency

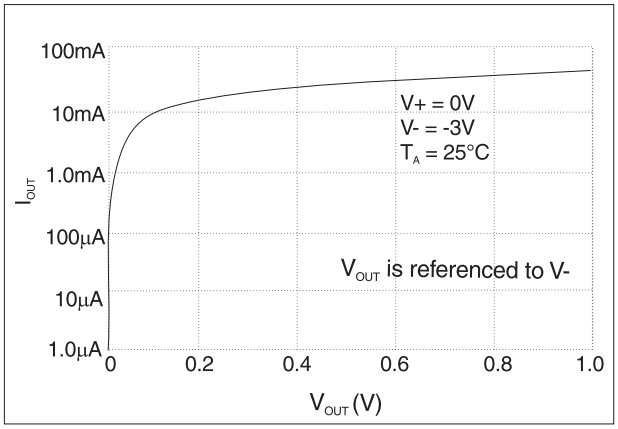


5V Disabled Input to Output Isolation

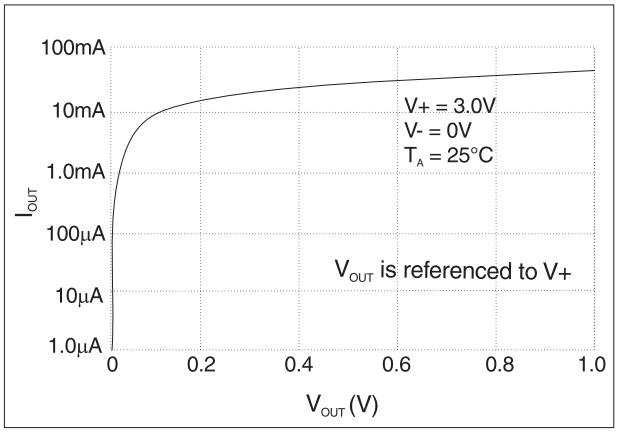


TYPICAL PERFORMANCE CHARACTERISTICS

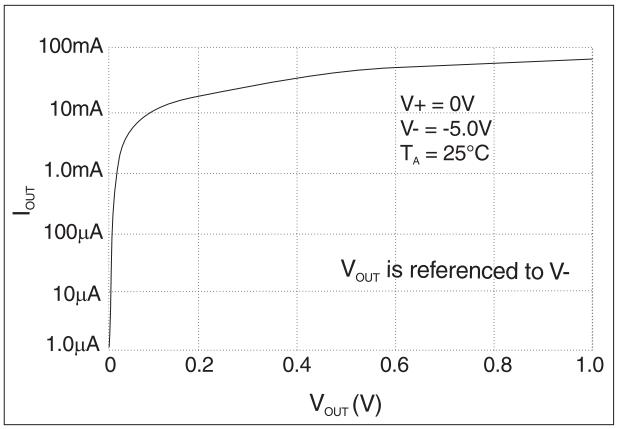
3V Current Sinking Versus V_{OUT}



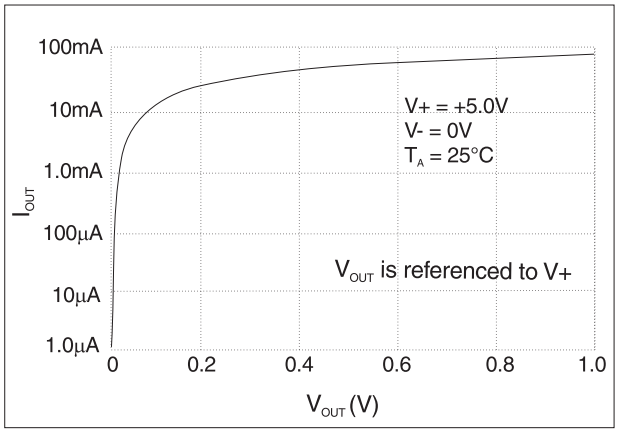
3V Current Sourcing Versus V_{OUT}



5V Current Sinking Versus V_{OUT}

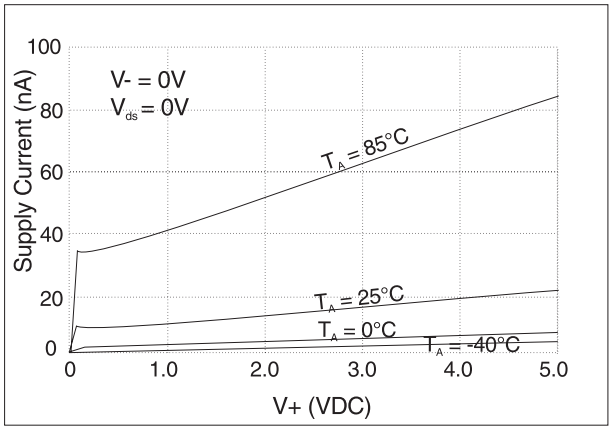


5V Current Sourcing Versus V_{OUT}

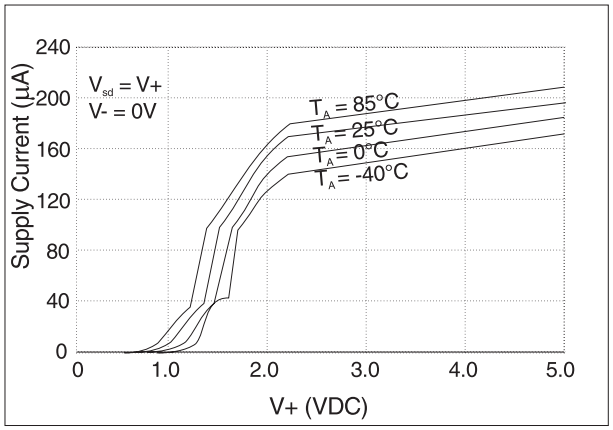


TYPICAL PERFORMANCE CHARACTERISTICS

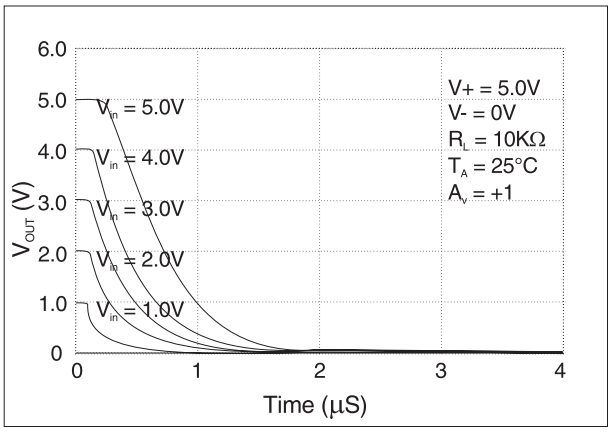
Disabled Supply Current



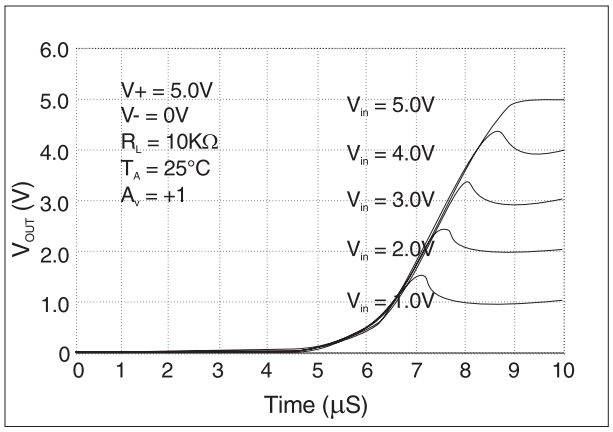
Enabled Supply Current



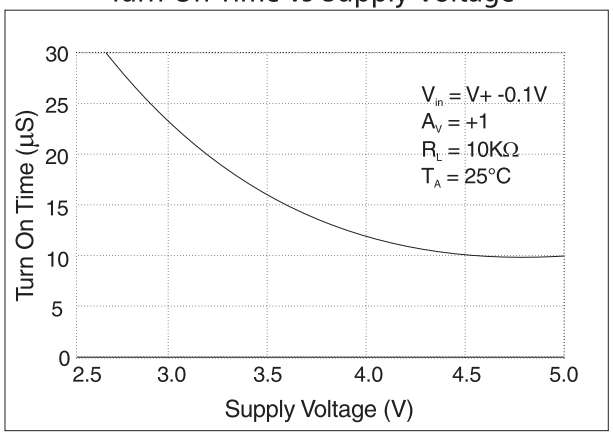
5V Disable Response for a Family of DC Inputs



5V Enable Response for a Family of DC Inputs



Turn On Time vs Supply Voltage



Application Benefits

The CMC7106 is very similar to the CAMD CMC7101AY, an improved version of the industry standard '7101' op amp. The CMC7106 has the additional benefit of reducing power consumption to almost nothing (<5microWatts @ 5V) when the amplifier is not being used.

Packaging
Most of the benefits of the CMC7106 are due to the use of a SOT package. The industry has readily adopted the SOT23-5 footprint, and this similar version has six pins. This leads to smaller finished products.

PC CARDS (PCMCIA type III cards) require low profile components. At 0.056 inches (1.43 mm), the CMC7106 is ideal.

Signal Integrity
As products become smaller, the natural space used to isolate circuits is lost. Signals can interact or pick up noise in these designs. By using a physically smaller amplifier package, the CMC7106 can be placed closer to the signal source, reducing noise pickup and it's small size makes it a simple buffer.

Rail-to-Rail Input and Output allow the amplifier to operate from lower supplies and also maintain signal level swings under large signal amplitude conditions.

Simplified Board Layout
Board layout is helped in a couple of ways due to the small size. Op Amps can be placed where amps are needed, shortening signal paths and PCB traces subject to noise pick up. Compared to a dual or quad device, two or four strategically placed SOT Amps reduce cross-talk and avoid long traces.

Lower Power Supply Current Drain
The CAMD CMC7106 is similar to the CAMD CMC7101AY, which has lower power supply drain than other SOT Amps. The CMC7106 lower supply current means longer operation in battery operated products, and even further savings in a 'shutdown' to idle mode.

Higher Output Drive
The CAMD CMC7106 has higher output current than other SOT Amps. It can be used as a driver in addition to use as a signal level amplifier.

Rail-To-Rail Input Swing
When the amplifier is used as a buffer, the input of the amplifier follows the input signal and if this is large compared to the available supply voltage, it is important that the Op Amp has a wide CMVR (Common Mode Voltage Range). RRIO Op Amps have a CMVR equal to (or greater than) the supplies and this allows large signal swings without clipping or distortion.

Shutdown Operation
Compared to a typical SOT Amp, an additional pin, Shutdown, is used to control the 'idle' mode of the amplifier. It allows the amplifier to be placed in a very low power consumption mode, effectively reducing the current to less than 5 μW (at 5V supply).

To use the shutdown pin, a logic level signal is connected to the shutdown pin, which is configured as a digital input (Logic "1" turns the amplifier on). This makes the input directly compatible with common logic family parts. If the shutdown feature is not desired, the pin should be shorted to V+ (pin 4).

Turn On and Turn Off (Shutdown) Characteristics
The turn off delay, t_{OFF}, is defined as the time between the Shutdown signal crossing and the disable threshold (typically V+ - 1 volt) and the time for the amplifier's output to come within 10% of its final value. It is largely governed by a propagation delay within the CMC7106 of a few hundred nanoseconds followed by an exponential decay determined by the load resistance in parallel with the load capacitance.

The turn on delay, t_{ON}, is defined as the time between the Shutdown signal crossing the threshold and the time the output reaches to within 10% of its final value. It exhibits a larger propagation delay through the amplifier which increases as V+ decreases (see the typical Performance Characteristics). The delay is followed by output slewing to the final value.

The delay time for V+ equal to 5 volts is about 4 μS, and since the slew rate is 1V/μS, a five volt signal requires about 10 μS to reach its final value. With V+ equal to 3 volts, however, the propagation delay increases to 20 μS yielding a total turn-on time of 24 μS for a 3 volt signal.

Applications of the CMC7106

High Side Current Sense

To monitor a load current, it is necessary to insert a current sense resistor into the power supply feed, as shown in Figure 1. The resulting voltage drop is proportional to the load current, but as both ends of this resistor are at (or very near to) the supply voltage, it is difficult to use a conventional Op Amp.

The CMC7106 is ideal for this application as the inputs can operate at either supply rail (or at ground when used with a single supply). The output voltage is directly proportional to current in the load, scaled by the gain of the amplifier. To reduce the power loss in the sense resistor and also keep the supply voltage to the load immune to load current variations, a small value R_{sense} is used.

An excellent application for this circuit is in a battery charger, where the charging current is monitored to detect end of charge (battery current will rise as the cells 'top off'), and charging must be reduced to prevent damage (out gassing or over heating).

The sense resistor can be placed in the negative side (known as Low Side Sensing), however this is less desirable due to disruption of the ground path.

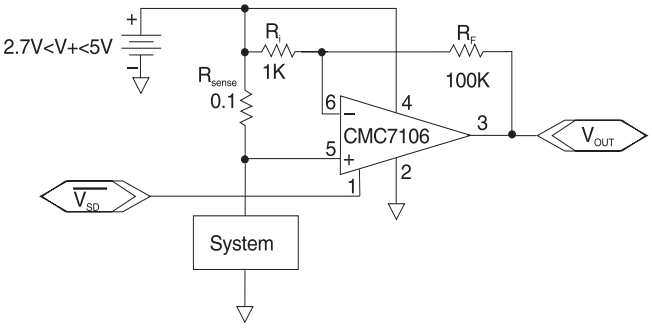


Figure 1. High Side Current Sense

Low Current 3.3V Regulator with Disable

Over the past few years, power supply voltages in systems, particularly in PC's, have migrated from 5 volts to 3.3 volts while at the same time, saving power – particularly in portable systems has become a major issue. On the other hand, there are "legacy" devices which still mandate the use of a 5 volt V_{cc}. Frequently in systems, a finite amount of current is needed for the 3.3 volt IC's. The circuit shown below provides a stable 3.3 voltage supply derived from the 5 volts at currents up to 100 mA while drawing only 300 µA's when enabled. It takes advantage of the CMC7106 op amp which provides a power down disable (shutdown) compatible with all 5 volt logic families and an ultra low current reference, the LT1389. When disabled, the circuit draws essentially zero current but when enabled exhibits load regulation of 0.05% from 0 to 100 mA, and line regulation of 0.01% from 4.5 V < Vdd < 5.5 V.

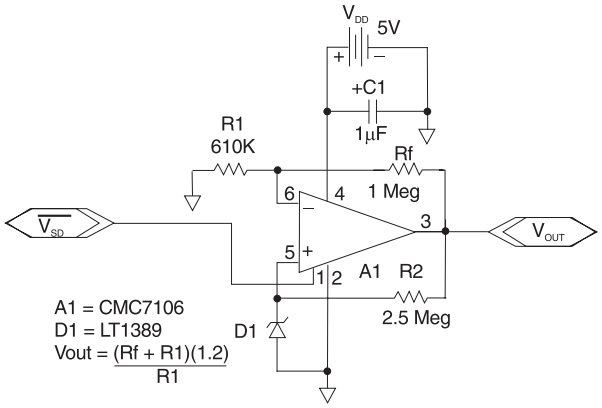


Figure 2. 5V to 3.3V Regulator with Disable

Input Common Mode Range Considerations

The CMC7106 is capable of accommodating input common mode and output voltages equal to both power supply rails. Nor will voltages that exceed the supply voltages cause phase inversion of the output. However, ESD diode clamps are provided at the inputs that can be damaged if static currents in excess of ± 5 mA are allowed to flow through them. This can occur when the magnitude of input voltage exceeds the rail by more than 0.3 volt. To preclude damage, a current limiting resistor, R_s, in series with the input is recommended as illustrated in Figure 1, whose value for R_s is given by:

$$R_s > \frac{V_{in} - (V+ 0.3\ V)}{5\ mA} \quad \textbf{(1)}$$

For V+ (or V-) equal to 2.7 volts and V_{in} equal to 10 volts, Rs should be chosen for a value of 1.5 KΩ or greater.

Shut-down Pin Current Limiting Considerations

The Shut-down pin also provides ESD clamp diodes that will be damaged if the signal exceeds the rail by 0.3 volt either from a logic gate or other signal source. If possible, the current should be limited to less than ± 5 mA by inserting a resistor between the gate or source and the Shut-down Pin whose value is determined by Equation (1) above.