

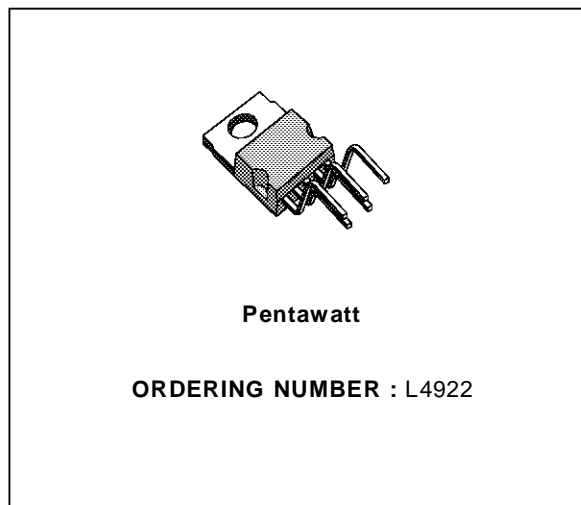
VERY LOW DROP REGULATOR WITH RESET

- VERY LOW DROP (max. 0.9 V at 1 A) OVER FULL OPERATING TEMPERATURE RANGE (- 40 / + 125°C)
- LOW QUIESCENT CURRENT (max 70 mA at 1 A) OVER FULL T RANGE
- PRECISE OUTPUT VOLTAGE (5 V ± 4 %) OVER FULL T RANGE
- POWER ON-OFF INFORMATION WITH SET-TABLE DELAY
- REVERSE BATTERY PROTECTION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN

DESCRIPTION

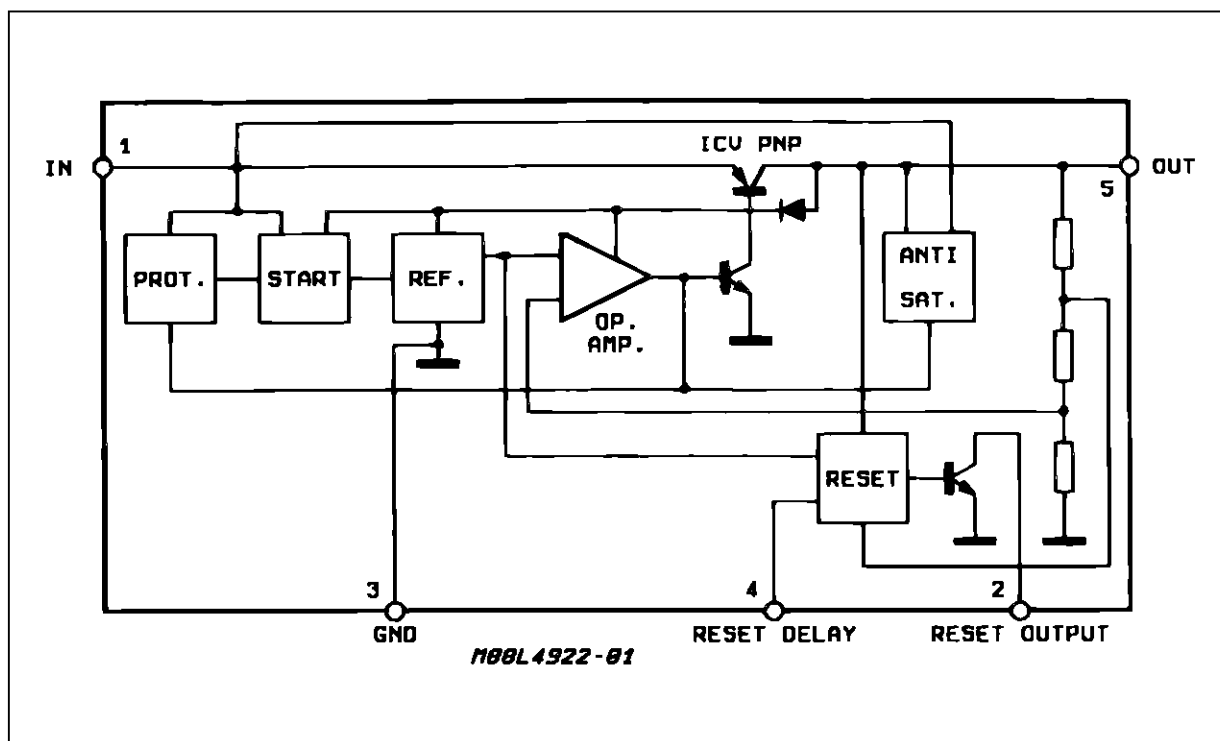
The L4922 is a high current monolithic voltage regulator with very low voltage drop (0.70 V max at 1 A, $T_J = 25\text{ }^\circ\text{C}$).

The device is internally protected against load dumps transient of + 60V, reverse polarity, over-



heating and output short circuit : thanks toted for the automotive and industrial applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

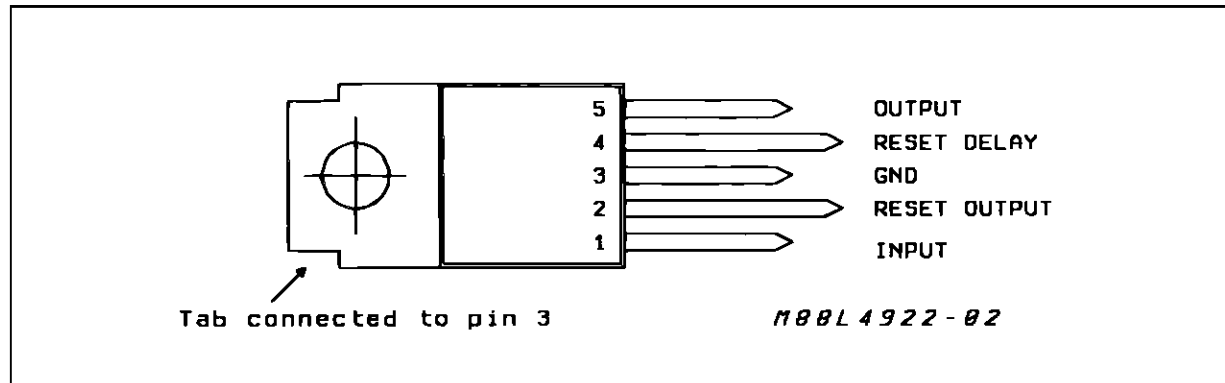
Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	V
V_r	DC Reverse Voltage	-18	V
V_D	Positive Load Dump Protection (t = 300ms)	60	V
T_J	Junction Temperature Range	-40 to 150	°C
T_{op}	Operating Temperature Range	-40 to 125	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal Resistance Junction-case	Max. 3.5	°C/W

PIN CONNECTION (Top view)



FUNCTIONAL DESCRIPTION

The operating principle of the voltage regulator is based on the reference, the error amplifier, the driver and the power PNP. This stage uses an Isolated Collector Vertical PNP transistor which allows to obtain very low dropout voltage (typ. 450mV) and low quiescent current ($I_Q = 20mA$ typically at $I_o = 1A$).

Thanks to these features the device is particularly suited when the power dissipation must be limited as, for example, in automotive or industrial applications supplied by battery.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor ($C_{o\min} = 22\mu F$) to guarantee the global stability of the system.

The antisaturation circuit allows to reduce drastically the current peak which takes place during the start up.

The reset function is LOW active when the output voltage level is lower than the reset threshold voltage V_{RthOFF} (typ. value : $V_o - 150mV$). When the output voltage is higher than V_{RthON} the reset becomes HIGH after a delay time settable with the external capacitor C_d . Typically $t_d = 20ms$, $C_d = 0.1\mu F$. The reset and delay threshold hysteresis improve the noise immunity allowing to avoid false switchings. The typical reset output waveform is shown in fig. 1.

ELECTRICAL CHARACTERISTICS ($V_i = 14.4\text{V}$, $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	(*) Note 1	6		26	V
V_o	Output Voltage	$I_o = 0\text{mA}$ to 1A $T_J = 25^\circ\text{C}$	4.8 4.9		5.2 5.1	V V
ΔV_{Line}	Line Regulation	$V_i = 6$ to 26V ; $I_o = 10\text{mA}$		5	25	mV
SVR	Supply Voltage Rejection	$I_o = 700\text{mA}$ $f = 120\text{Hz}$; $C_o = 47\mu\text{F}$ $V_i = 12V_{\text{dc}} + 5V_{\text{pp}}$		55		dB
ΔV_{LOAD}	Load Regulation	$I_o = 10\text{mA}$ to 1A		15	50	mV
$V_i - V_o$	Dropout Voltage	$T_J = 25^\circ\text{C}$, $I_o = 1\text{A}$ Over Full T, $I_o = 1\text{A}$		0.45	0.70 0.90	V V
I_q	Quiescent Current	$I_o = 10\text{mA}$ $I_o = 1\text{A}$		7 25	12 70	mA mA
I_{SC}	Short Circuit Current			1.8		A
V_R	Rset Output Saturation Voltage	$1.5\text{V} < V_o < V_{\text{RT (off)}}$, $I_R = 1.6\text{mA}$ $3\text{V} < V_o < V_{\text{RT (off)}}$, $I_R = 8\text{mA}$			0.40 0.40	V V
$V_{\text{RT peak}}$	Power On-Off Reset out Peak Voltage	$1\text{K}\Omega$ Reset Pull-up to V_o		0.65	1.0	V
I_R	Reset Output Leakage Current (high level)	V_o in Regul. $V_R = 5\text{V}$			50	μA
t_D	Reset Pulse Delay Time	$C_D = 100\text{nF}$		20		ms
V_{RthOFF}	Power OFF V_o Threshold	V_o @ Reset out H to L Transition; $T_J = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	4.75 4.70	$V_o - 0.15$		V V
I_{C6}	Delay Capacitor Charging Current (current generator)	$V_4 = 3\text{V}$		20		μA
V_{RthON}	Power ON V_o Threshold	V_o @ Reset out L to H Transition		$V_{\text{rthOFF}} + 0.03\text{V}$	$V_o - 0.04\text{V}$	V
V_4	Delay Comparator Threshold	Reset out = "1" H to L Transition Reset out = "0" L to H Transition	3.2 3.7	4	3.8 4.4	V V
V_{6H}	Delay Comparator Hysteresis			500		mV

(*) **Note 1** : The device is not operating within the range : $26\text{V} < V_i < 37\text{V}$.

EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parasitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is $47\mu\text{F}$.

Figure 1 : Typical Reset Output Waveform.

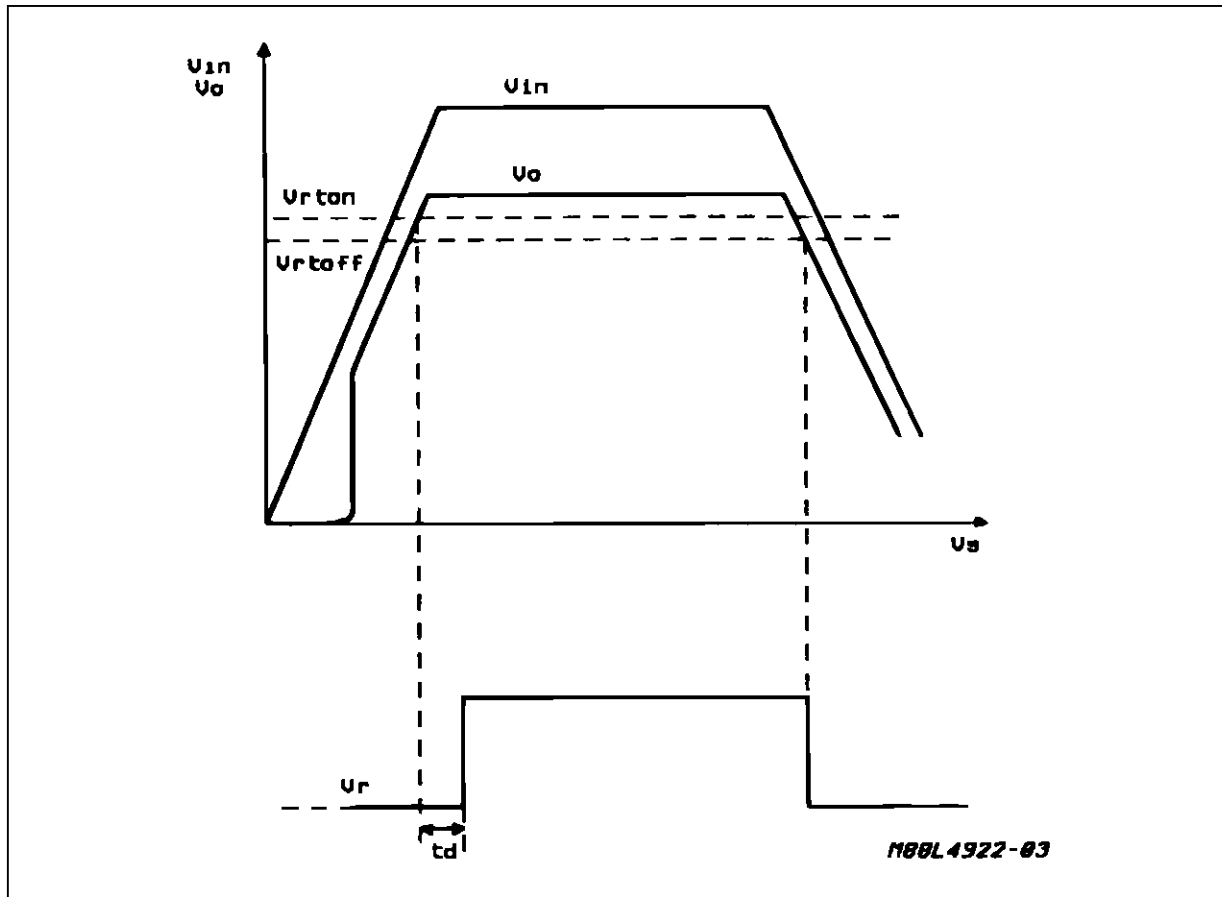
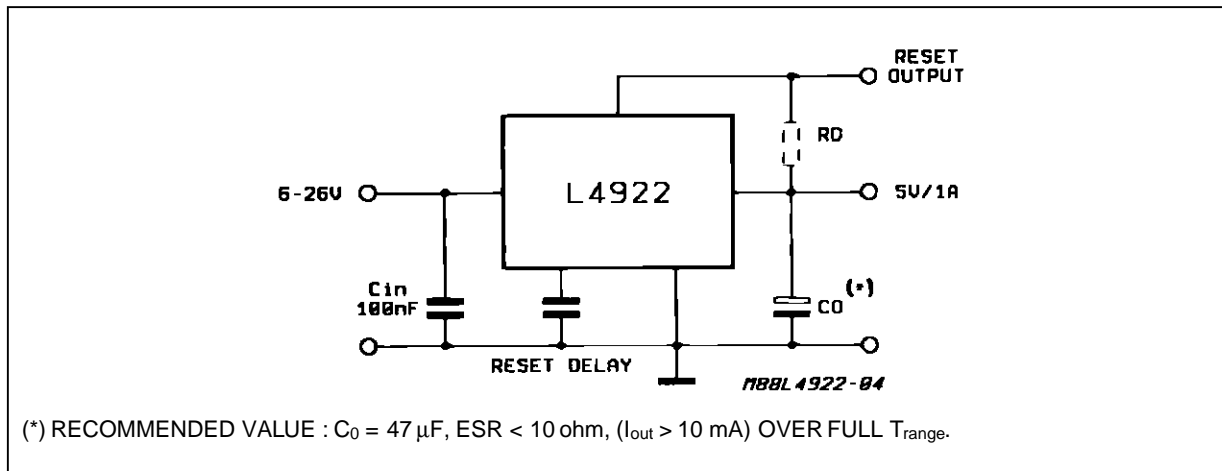
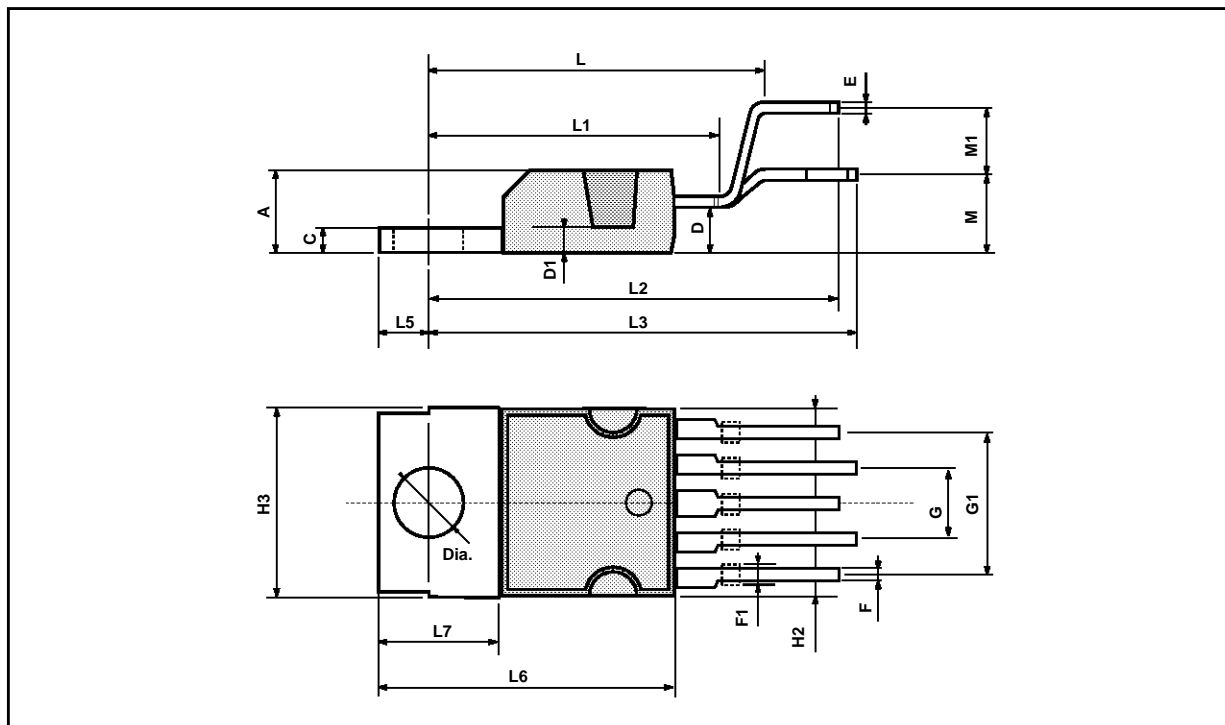


Figure 2 : Typical Application Circuit.



PENTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4		0.126	0.134	0.142
G1		6.8		0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152



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