19-0370; Rev 0; 2/95

MAXIM

Quadrature Digitizer Circuits

General Description

The MAX2100 family of quadrature digitizers offers complete solutions to digital demodulation problems. The flagship of the MAX2100 family is the MAX2101 6-bit Quadrature Digitizer. The subcircuits derived from the MAX2101 provide excellent starting points for the RF IC designer to develop components that bridge the gap between existing RF downconverters and CMOS digital signal processors.

Each MAX2100 subcircuit comes with a detailed schematic, TEKSPICE or PSPICE netlist, models, and GDSII layout for incorporation in your own custom ASIC design. These subcircuits can be used separately or in combination to produce complete demodulation and digitization components for intermediate frequencies (IF) ranging from 70MHz to 700MHz, and for base bandwidths to 80MHz*. All are powered by a +5V supply, and are implemented in Maxim's proprietary GST-1 wafer fabrication process with NPN f_T = 13GHz.

Maxim does not guarantee specifications or fitness for use of these subcircuits in your custom ASIC. The subcircuits are intended to demonstrate Maxim's process and design capability, and to provide circuit designers with a "head start" in developing their own ASIC. Operation of these subcircuits in a customer-designed ASIC is the responsibility of the customer.

Applications

Recovery of PSK and QAM Modulated RF Carriers
Direct-Broadcast Satellite (DBS) Systems
Television Receive-Only (TVRO) Systems
Cable Television (CATV) Systems

Features

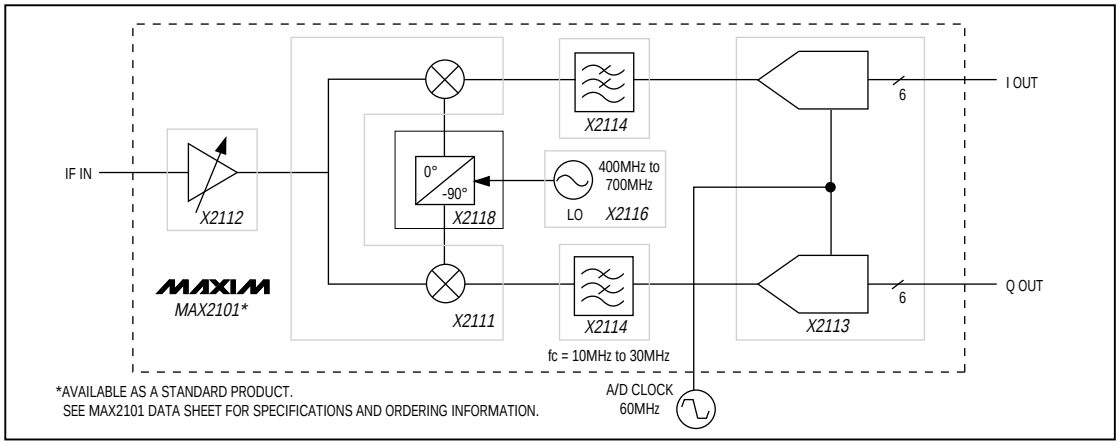
- **Operation at IFs from 70MHz to 700MHz***
- **Precision Quadrature Demodulation (1°, 0.2dB typ Mismatch, f = 650MHz)**
- **Matched Active Filters with Electronically Variable Cutoff from 10MHz to 30MHz**
- **40dB of AGC Range**
- **High-Speed 6-Bit ADCs with 5.8 (typ) Effective Bits (f_{IN} = 30MHz, f_C = 120Msps) and 200MHz Input Bandwidth**

Ordering Information

PART	SIMULATOR	MEDIUM	FORMAT
X21nnPFD	PSPICE	3.5" Floppy	DOS
X21nnPFT	PSPICE	3.5" Floppy	TAR
X21nnPTT	PSPICE	Tape	TAR
X21nnPHT	PSPICE	9-track 6250 bpi	TAR
X21nnPLT	PSPICE	9-track 1600 bpi	TAR
X21nnPET	PSPICE	Electronic mail	TAR
X21nnTFT	TEKSPICE	3.5" Floppy	TAR
X21nnTTT	TEKSPICE	Tape	TAR
X21nnTHT	TEKSPICE	9-track 6250 bpi	TAR
X21nnTLT	TEKSPICE	9-track 1600 bpi	TAR
X21nnTET	TEKSPICE	Electronic mail	TAR

The MAX2100 cells are available in the above formats to customers who have purchased a GST-1 ASIC Start-Up Package and signed Maxim's Non-Disclosure Agreement.

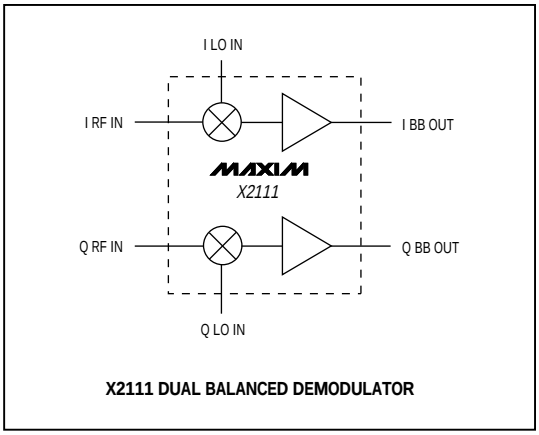
Block Diagram



**VCO and Quadrature Generator limited to 400MHz to 700MHz*

Dual Balanced Demodulator

Block Diagram



X2111 DUAL BALANCED DEMODULATOR

Features

- **Wide Output Bandwidth (>80MHz)**
- **Matched Demodulation to 700MHz**
- **10dB Conversion Gain**

Description

The X2111 Dual Balanced Demodulator cell comprises two Gilbert-cell, double-balanced mixers. In combination with the X2118 precision quadrature generator, the X2111 provides precise quadrature demodulation of QPSK and QAM modulated carriers to 700MHz.

Cell Dimensions: 2 x [300µm x 230µm]

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

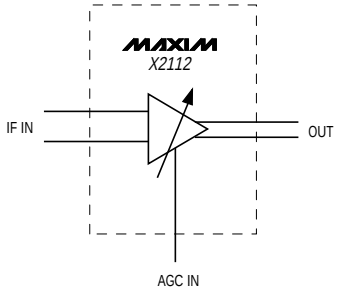
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5V						
LO Input Frequency	f_{LO}		400		700	MHz
Output Baseband Gain Flatness		5Hz to 20MHz			0.4	dB
I/Q Amplitude Imbalance	ΔM(I/Q)	f_{LO} = 650MHz			0.4	dB
I/Q Phase Imbalance	Δϕ(I/Q)	f_{LO} = 650MHz			1.5	°
Noise Figure	NF	f_{LO} = 650MHz			15	dB
Conversion Gain	A	f_{LO} = 650MHz	10			dB
Input Third-Order Intercept	IIP3	f_{LO} = 650MHz	+10			dBm
Supply Current	I_{CC}			18		mA
Output Bandwidth	f_{-3dB}		80			MHz

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V_{CC} (I/Q)	+5V supply to I/Q mixer	SUB	Substrate connection (GND)
BIAS (I/Q)	500µA PTAT reference current input (from X2112 or equivalent)	OSC (I/Q)	+ LO input
V_{EE} (I/Q)	GND for I/Q mixer	OSCB (I/Q)	- LO input
IP (I/Q)	+ RF input	OPA (I/Q)	+ Baseband output
IPB (I/Q)	- RF input	OPAB (I/Q)	- Baseband output

IF Amplifier with Variable Gain

Block Diagram



X2112 IF AMPLIFIER WITH VARIABLE GAIN

Features

- **24dB Gain**
- **800MHz Bandwidth**
- **Over 40dB of Gain Range**

Description

The X2112 IF Amplifier with Variable Gain cell comprises a differential input amplifier with 10dB insertion gain, an AGC amp with 40dB of control range, and a second IF amp with 12dB gain. The differential input can be driven single-ended by proper AC grounding or by terminating the inverting input. There is sufficient linearity to provide IIP3 of +10dBm at minimum AGC setting.

Cell Dimensions: 780µm x 725µm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

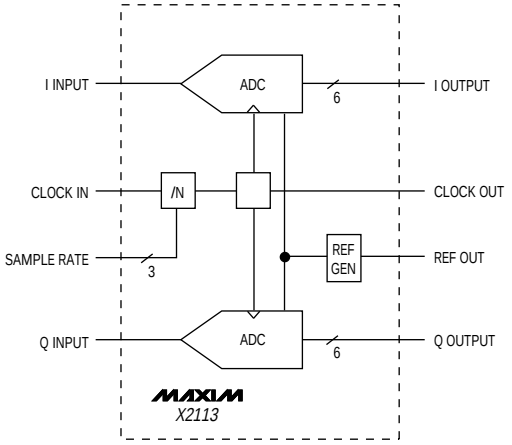
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%, R_L = 1kΩ, C_L = 2pF						
Bandwidth (-3dB)	BW-3dB	Max gain, Pin = -48dBm		800		MHz
Maximum Gain	AVmax	f = 650MHz, V_{AGC} = max	22			dB
Minimum Gain	AVmin	f = 650MHz, V_{AGC} = min			-18	dB
Gain-Control Range	ΔAV	f = 650MHz	40			dB
Noise Figure	NF	f = 650MHz, V_{AGC} = max		15	18	dB
Noise-Figure Variation	ΔNF	Max gain to min gain			1	dB/dB
Input Third-Order Intercept	IIP3	f = 650MHz, max gain	-35			dBm
		f = 650MHz, min gain	+10			
Input VSWR		Z0 = 50Ω/side			2:1	
Output VSWR		Z0 = 50Ω/side			2:1	
Supply Current	I_{CC}			20		mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V_{CC}	+5V supply	AGCIP	AGC control voltage input
V_{EE}	Ground	2R5	Bandgap-derived 2.5V output
SUB	Substrate connection (ground)	OP	+ IF output
IP	+ IF input	OPB	- IF output
IPB	- IF input	BGR	Bandgap reference (1.2V) output
K250	250µA constant reference current for X2118	VPTAT	Voltage proportional to absolute T output
P250	250µA PTAT reference current for X2118	(I/Q)BIAS	250µA PTAT reference current for X2114
MIX(I/Q)	500µA PTAT reference current for X2111		

Dual 6-Bit ADCs (Megacell)

Block Diagram



X2113 DUAL 6-BIT ADCs (MEGACELL)

Features

- **Dual, 6-Bit, 120Msps Flash Architecture**
- **Programmable Sample Rate**
- **Excellent Dynamic Performance (5.8 effective bits at f_{IN} = 30MHz)**
- **Low Incidence of Metastable States**
- **All Reference Generation Circuitry Included**

Description

The X2113 “Megacell” contains two 6-bit flash ADCs and associated reference and clock generation circuitry. The comparator array in each ADC contains 63 identical differential comparator and latch cells. The proprietary differential architecture minimizes integral linearity error and the occurrence of metastable states. The thermometer code output of the comparator array is translated into gray code using a fully differential wired-AND/wired-OR scheme. This maximizes noise immunity. The gray code is then converted to binary with a modified XOR array.

The reference generator applies a precision bandgap signal to the differential ladder in the comparator array. Additional circuitry is provided to adjust the half-scale ladder voltage to the common-mode voltage of the differential input signal.

A programmable divider allows the user to change sample rate from a fixed external-clock oscillator.

Cell Dimensions: 2800µm x 1500µm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%						
Maximum Sample Rate, Each Channel	SRmax		120			Msps
0.1dB Bandwidth	BW0.1dB		20			MHz
Effective Number of Bits	ENOB	f_{IN} = 30MHz, f_S = 60Msps, 95% FS		5.8		Bits
Input Third-Order Intermod	IM3	f1 = 10MHz, FS–7dB; f2 = 12MHz, FS–7dB		-38		dBc
Settling Time	t_{TRAN}	Full-scale to <1%			10	ns
Full-Scale Input Range	ΔVIN_{FS}			±0.75		V
Common-Mode Input Range	VIN_{cm}		2.25		2.75	V
Input Resistance	RIN		5			kΩ
Input Capacitance	CIN				2	pF
Amplitude Response Mismatch	ΔA	Channel-to-channel			0.3	dB
Aperture Uncertainty		f_S = 60Msps			80	ps
Aperture Delay Match, Channel-to-Channel					20	ps

KEY ELECTRICAL CHARACTERISTICS (continued)

(T_A = 0°C to +70°C, unless otherwise noted.)

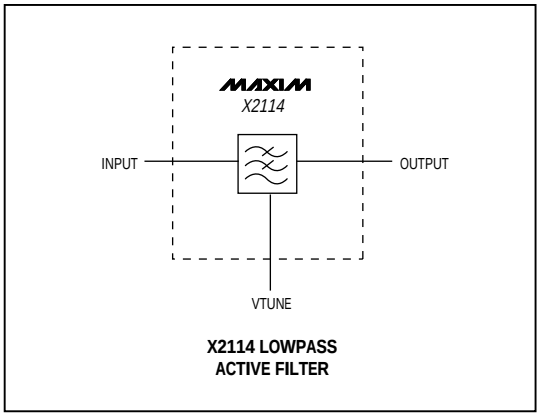
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset	V_{OS}	LSB = 24mV, either channel			0.5	LSB
Differential Nonlinearity	DNL				0.5	LSB
Integral Nonlinearity	INL				0.5	LSB
Data Output High	V_{OH}	R_L = 1MΩ, C_L = 15pF	2.4			V
Data Output Low	V_{OL}	R_L = 1MΩ, C_L = 15pF			0.5	V
Supply Current	I_{CC}			80	100	mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V_{CC}AD	+5V supply, quantizer	AIN (I/Q)	+ Analog input
V_{CC}D	+5V supply, digital	AINB (I/Q)	- Analog input
V_{CC}O	+5V supply, outputs	BGR	Bandgap reference output
V_{CC}C	+5V supply, clock	D0 (I/Q)	Digital output, LSB
SUBA	Substrate (ground), analog	D1 (I/Q)	Digital output
SUBD	Substrate (ground), digital	D2 (I/Q)	Digital output
VGNDAD	Ground connection, quantizer	D3 (I/Q)	Digital output
VGNDDD	Ground connection, encoder	D4 (I/Q)	Digital output
VGNDDO	Ground connection, output	D5 (I/Q)	Digital output, MSB
VGNDC	Ground connection, clock	BINEN	Binary enable/Two's complement
MCLK	Master clock input	S2	Programmable sample-rate control, MSB
RCLK	Reference clock (div 6) output	S1	Programmable sample-rate control
DCLK	Data clock output	S0	Programmable sample-rate control, LSB
DCLKB	Data clock complement output	P250 (I/Q)	250µA PTAT reference current input (from cell X2114 or equivalent)

Active Lowpass Filter

Block Diagram



X2114 LOWPASS ACTIVE FILTER

Features

- **5-Pole Butterworth Response**
- **Adjustable Cutoff Frequency**
- **No External Components Required**

Description

The X2114 cell is an Active Lowpass Filter for anti-aliasing. The 5th-order Butterworth response is realized using a Gyrator topology. Cutoff frequency can be adjusted from 10MHz to 30MHz. Other pole-only filter characteristics, as well as different cutoff frequency ranges, can be designed by changing capacitor values.

Filter cutoff-frequency control requires a linear PTAT voltage between 1V and 4V (at +27°C). An on-chip reference generator provides the necessary voltage variation with temperature.

Cell Dimensions: 620 x 780 + 260 x 520µm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

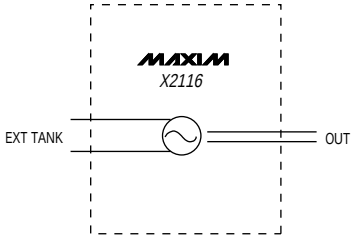
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%						
Cutoff Frequency	f_C	VTUNE = 2.1V, 3dB, T_A = +25°C	16		24	MHz
Minimum Cutoff	f_{CMIN}	VTUNE = 1V, 3dB, T_A = +25°C			10	MHz
Maximum Cutoff	f_{CMAX}	VTUNE = 4V, 3dB, T_A = +25°C	30			MHz
Passband Attenuation	APB	f = 5MHz		0	2	dB
Stop-Band Attenuation	ASB	f = 2 x f_C (with respect to signal level at f = 0.5 x f_C)	27			dB
Maximum Input Signal, p-p	V_{IN} (max)		30			mV
Supply Current	I_{CC}			2.5		mA
Equivalent Input Noise	e_n	f = 5MHz, R_S = 50Ω		58		nV/√Hz

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V_{CC}	+5V supply	OP	Output
V_{EE}	Ground	REF1	Output reference
BIAS	250µA PTAT reference current input (from X2112 or equivalent)	REF	Bandgap voltage in (from X2112 or equivalent)
IP	+ Input	ADC	250µA PTAT reference current output for X2113
IPB	- Input	VTUNE	Tuning voltage input (PTAT)
SUB	Substrate connection (GND)		

Differential Oscillator

Block Diagram



X2116 DIFFERENTIAL OSCILLATOR

Features

- **Oscillates from <400MHz to >700MHz**
- **Low Phase Noise (-88dBc/Hz @ 10kHz Offset, Qr >20)**
- **Differential Resonator Port for Immunity to Interference and Crosstalk**

Description

The X2116 cell is a Differential Oscillator suitable for use as the LO in a receiver system. The differential inputs present a negative resistance for use with an external resonator. A differential topology is used to provide maximum interference rejection.

Cell Dimensions: 520µm x 260µm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

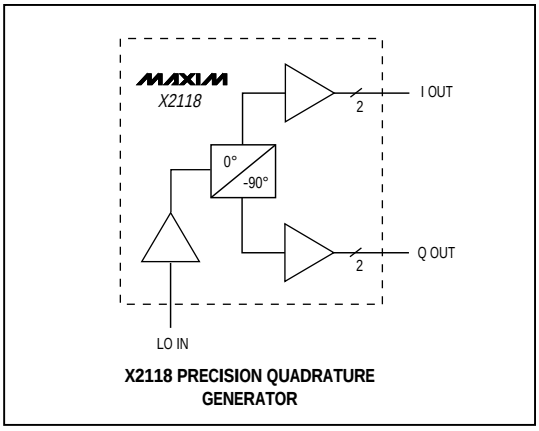
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%						
Oscillation Frequency	f_C	External resonator	400		700	MHz
Phase Noise Floor	ΦN	20MHz off f_C, 1Hz BW, Qr = 20		-140		dBc
Phase Noise	ΦN	10MHz off f_C, 1Hz BW, Qr = 20		-88		dBc
Output Level, Differential, p-p	Vo	C_L = 1pF/side, R_L = 10k/side		600		mV
Supply Current	I_{CC}				10	mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V_{CC}	+5V supply	OP	+ Output
TNKA	Differential tank connection A	OPB	- Output
TNKB	Differential tank connection B	SUB	Substrate connection (GND)
K125	125µA constant reference current input (from X2118 or equivalent)	P250	250µA PTAT reference current input (from X2118 or equivalent)
V_{EE}	Ground		

Precision Quadrature Generator

Block Diagram



X2118 PRECISION QUADRATURE GENERATOR

Features

- **Precision Quadrature Generation (<1.5° at 650MHz)**
- **Wide Input Frequency Range (400MHz to 700MHz)**

Description

The X2118 Precision Quadrature Generator cell uses a delay-locked loop to provide tight amplitude and phase matching. The input from an external VCO drives a buffer and a delay line consisting of three electronically variable delay cells. The output of the delay line drives a second buffer identical to the first. The buffer outputs are compared by a phase detector whose error signal drives the variable delay cells to adjust the phase difference to 90°. This method provides precise quadrature generation over the wide input frequency range of 400MHz to 700MHz.

Cell Dimensions: 570µm x 1800µm

KEY ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5.0V ±5%						
LO Frequency	f_{LO}		400		700	MHz
Output Phase Mismatch	$\Delta\Phi$	f_{LO} = 650MHz			1.5	°
Output Level	Vo (pk-pk)			400		mV
Output Amplitude Mismatch	ΔVo	f_{LO} = 650MHz			12	mV
LO Input Level	V_{LO}		-10		0	dBm
LO Input VSWR		ZC = 50Ω			2:1	
Supply Current	I_{CC}			20		mA

PORT LIST

PORT NAME	DESCRIPTION	PORT NAME	DESCRIPTION
V_{CC}	+5V supply	Q	+ Quadrature output
IP	+ Input	QB	- Quadrature output
IPB	- Input	I	+ Inphase output
V_{EE}	GND	IB	- Inphase output
K250	250µA constant reference current input (from X2112 or equivalent)	P250	250µA PTAT reference current input (from X2112 or equivalent)
SUB	Substrate connection (GND)		