

## MEMORY

## CMOS

## 1 M × 4 BITS

## HYPER PAGE MODE DYNAMIC RAM

## MB814405D-60/60L/-70/70L

## CMOS 1,048,576 × 4 BITS Hyper Page Mode Dynamic RAM

## ■ DESCRIPTION

The Fujitsu MB814405D is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 4-bit increments. The MB814405D features the "hyper page" mode of operation which provides extended valid time for data output and higher speed random access of up to 1,024 × 4 bits of data within the same row than the fast page mode. The MB814405D DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814405D is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB814405D is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814405D are not critical and all inputs are TTL compatible.

## ■ PRODUCT LINE &amp; FEATURES

Parameter		MB814405D				
		-60	-60L	-70	-70L	
RAS Access Time		60 ns max.		70 ns max.		
CAS Access Time		15 ns max.		20 ns max.		
Address Access Time		30 ns max.		35 ns max.		
Random Cycle Time		105 ns min.		125 ns min.		
Hyper Page Mode Cycle Time		25 ns min.		30 ns min.		
Low Power Dissipation	Operating Current	Normal Mode	495 mW max.		413 mW max.	
		Hyper Page Mode	385 mW max.		358 mW max.	
	Standby Current	TTL Level	11 mW max.	8.25 mW max.	11 mW max.	8.25 mW max.
		CMOS Level	5.5 mW max.	1.1 mW max.	5.5 mW max.	1.1 mW max.

- 1,048,576 words × 4 bits organization
- Silicon gate, CMOS, Advanced-Stacked Capacitor Cell
- All input and output are TTL compatible
- 1,024 refresh cycles every 16.4 ms
- Self refresh function

- Standard power and Low power versions
- Early write or  $\overline{OE}$  controlled write capability
- RAS-only, CAS-before-RAS, or Hidden Refresh
- Hyper Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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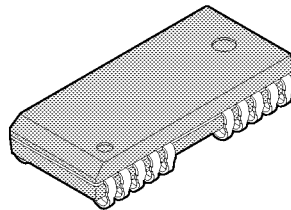
## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1.0 to +7.0	V
Voltage of $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-1.0 to +7.0	V
Power Dissipation	$P_D$	1.0	W
Short Circuit Output Current	$I_{OUT}$	-50 to +50	mA
Storage Temperature	$T_{STG}$	-55 to +125	°C

**WARNING:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## ■ PACKAGE

Plastic SOF Package



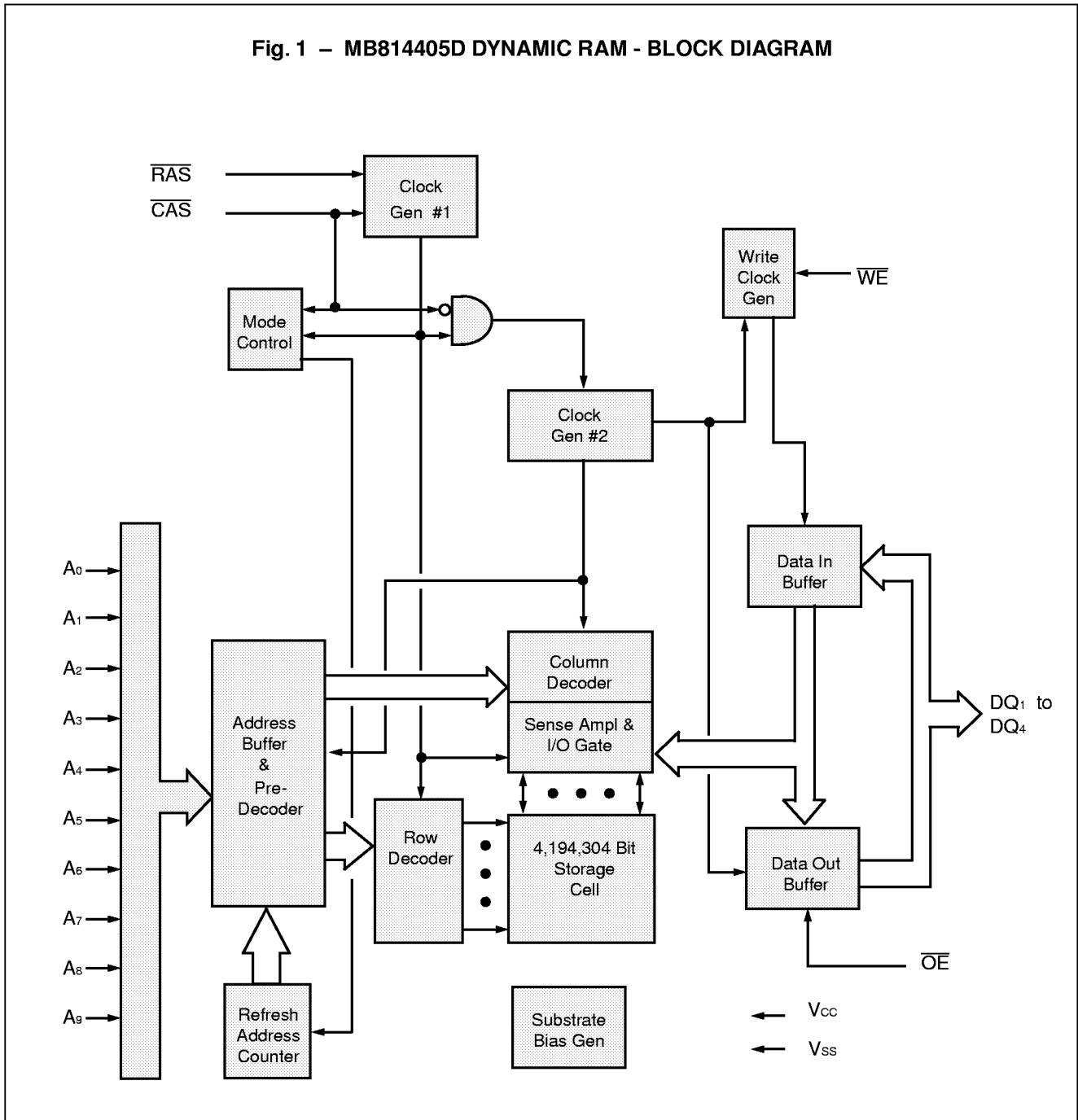
(LCC-26P-M04)

### Package and Ordering Information

- 26-pin plastic (300 mil) SOJ, order as MB814405D-xxPJN
- 26-pin plastic (300 mil) SOJ, order as MB814405D-xxLPJN (Low Power)

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Fig. 1 – MB814405D DYNAMIC RAM - BLOCK DIAGRAM



## ■ CAPACITANCE

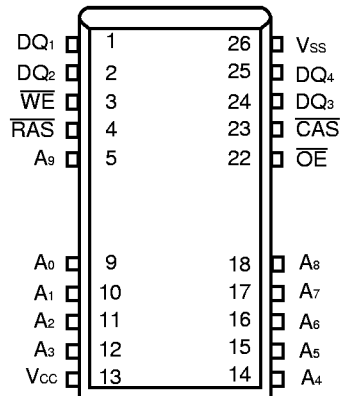
(T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A <sub>0</sub> to A <sub>9</sub>	C <sub>IN1</sub>	–	5	pF
Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	C <sub>IN2</sub>	–	7	pF
Input/Output Capacitance, DQ <sub>1</sub> to DQ <sub>4</sub>	C <sub>DO</sub>	–	7	pF

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## ■ PIN ASSIGNMENT AND DESCRIPTION

26-Pin SOJ  
(TOP VIEW)  
<LCC-26P-M04>



Designator	Function
DQ <sub>1</sub> to DQ <sub>4</sub>	Data Input/Output
$\overline{WE}$	Write enable
$\overline{RAS}$	Row address strobe
A <sub>0</sub> to A <sub>9</sub>	Address inputs
V <sub>cc</sub>	+5.0 volt power supply
$\overline{OE}$	Output enable
$\overline{CAS}$	Column address strobe
V <sub>ss</sub>	Circuit ground

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## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	*1	$V_{CC}$	4.5	5.0	5.5	V	0°C to +70°C
		$V_{SS}$	0	0	0		
Input High Voltage, all inputs	*1	$V_{IH}$	2.4	—	6.5	V	
Input Low Voltage, all inputs*	*1	$V_{IL}$	-2.0	—	0.8	V	
Input Low Voltage, DQ*	*1	$V_{ILD}$	-1.0	—	0.8	V	

\* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

## ■ FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any four of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by  $\overline{CAS}$  and  $\overline{RAS}$  as shown in Figure 5. First, ten row address bits are input on pins  $A_0$ -through- $A_9$  and latched with the row address strobe ( $\overline{RAS}$ ) then, ten column address bits are input and latched with the column address strobe ( $\overline{CAS}$ ). Both row and column addresses must be stable on or before the falling edge of  $\overline{CAS}$  and  $\overline{RAS}$ , respectively. The address latches are of the flow-through type; thus, address information appearing after  $t_{RAH}$  (min) +  $t_T$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{WE}$ . When  $\overline{WE}$  is active Low, a write cycle is initiated; when  $\overline{WE}$  is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an  $\overline{OE}$  (delayed) write cycle, and a read-modify-write cycle. The falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data ( $DQ_1$  to  $DQ_4$ ) is strobed by  $\overline{CAS}$  and the setup/hold times are referenced to  $\overline{CAS}$  because  $\overline{WE}$  goes Low before  $\overline{CAS}$ . In a delayed write or a read-modify-write cycle,  $\overline{WE}$  goes Low after  $\overline{CAS}$ ; thus, input data is strobed by  $\overline{WE}$  and all setup/hold times are referenced to the write-enable signal.

### DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs and High-Z state are obtained under the following conditions:

- $t_{RAC}$  : from the falling edge of  $\overline{RAS}$  when  $t_{RCD}$  (max) is satisfied.
- $t_{CAC}$  : from the falling edge of  $\overline{CAS}$  when  $t_{RCD}$  is greater than  $t_{RCD}$  (max).
- $t_{AA}$  : from column address input when  $t_{RAD}$  is greater than  $t_{RAD}$  (max), and  $t_{RCD}$  (max) is satisfied.
- $t_{OEA}$  : from the falling edge of  $\overline{OE}$  when  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$ .
- $t_{OEZ}$  : from  $\overline{OE}$  inactive.
- $t_{OFF}$  : from  $\overline{CAS}$  inactive while  $\overline{RAS}$  inactive.
- $t_{OFR}$  : from  $\overline{RAS}$  inactive while  $\overline{CAS}$  inactive.
- $t_{WEZ}$  : from  $\overline{WE}$  active while  $\overline{CAS}$  inactive.

The data remains valid after either  $\overline{OE}$  is inactive, or both  $\overline{RAS}$  and  $\overline{CAS}$  are inactive, or  $\overline{CAS}$  is reactivated. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

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## HYPER PAGE MODE OPERATION

The hyper page mode operation provides faster memory access and lower power dissipation. The hyper page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions,  $\overline{RAS}$  is held Low for all contiguous memory cycles in which row addresses are common. For each page of memory (within column address locations), any of  $1,024 \times 4$ -bits can be accessed and, when multiple MB814405Ds are used,  $\overline{CAS}$  is decoded to select the desired memory page. Hyper page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted. Hyper page mode features that output remains valid when  $\overline{CAS}$  is inactive until  $\overline{CAS}$  is reactivated.

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## ■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note 3

Parameter	Notes	Symbol	Conditions	Value				Unit
				Min.	Typ.	Max.		
						Std power	Low power	
Output High Voltage	*1	$V_{OH}$	$I_{OH} = -5.0 \text{ mA}$	2.4	—	—		V
Output Low Voltage	*1	$V_{OL}$	$I_{OL} = 4.2 \text{ mA}$	—	—	0.4		
Input Leakage Current (Any Input)		$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V};$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V};$ $V_{SS} = 0 \text{ V};$ All other pins not under test = 0 V	-10	—	10		$\mu\text{A}$
Output Leakage Current		$I_{O(L)}$	$0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V};$ Data out disabled	-10	—	10		
Operating Current (Average Power Supply Current)	MB814405D-60	$I_{CC1}$	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ cycling; $t_{RC} = \text{min}$	—	—	90		mA
	MB814405D-70					75		
Standby Current (Power Supply Current)	TTL level	$I_{CC2}$	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$	—	—	2.0	1.5	mA
	CMOS level		$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$			1.0	0.2	
Refresh Current #1 (Average Power Supply Current)	MB814405D-60	$I_{CC3}$	$\overline{\text{CAS}} = V_{IH}, \overline{\text{RAS}}$ cycling; $t_{RC} = \text{min}$	—	—	90		mA
	MB814405D-70					75		
Hyper Page Mode Current	MB814405D-60	$I_{CC4}$	$\overline{\text{RAS}} = V_{IL}, \overline{\text{CAS}}$ cycling; $t_{HPC} = \text{min}$	—	—	70		mA
	MB814405D-70					65		
Refresh Current #2 (Average Power Supply Current)	MB814405D-60	$I_{CC5}$	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ; $t_{RC} = \text{min}$	—	—	90		mA
	MB814405D-70					75		
Battery Back Up Current (Average Power Supply Current)	MB814405D-60L	$I_{CC6}$	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ; $t_{RC} = 125 \mu\text{s}$ $t_{RAS} = \text{min to } 1 \mu\text{s}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V},$ $V_{IL} \leq 0.2 \text{ V}$	—	—	300		$\mu\text{A}$
	MB814405D-70L					300		
Refresh Current #3 (Average Power Supply Current)	MB814405D-60	$I_{CC9}$	$\overline{\text{RAS}} = \overline{\text{CAS}} \leq 0.2 \text{ V}$ Self refresh	—	—	1000	300	$\mu\text{A}$
	MB814405D-70					1000	300	

# MB814405D-60/60L/-70/70L

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814405D-60		MB814405D-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh	Std power	$t_{REF}$	—	16.4	—	16.4	ms
		Low power		—	128	—	128	
2	Random Read/Write Cycle Time		$t_{RC}$	105	—	125	—	ns
3	Read-Modify-Write Cycle Time		$t_{RWC}$	142	—	167	—	ns
4	Access Time from $\overline{RAS}$	*6,9	$t_{RAC}$	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	*7,9	$t_{CAC}$	—	15	—	20	ns
6	Column Address Access Time	*8,9	$t_{AA}$	—	30	—	35	ns
7	Output Hold Time		$t_{OH}$	0	—	0	—	ns
8	Output Hold Time from $\overline{CAS}$		$t_{OHC}$	5	—	5	—	ns
9	Output Buffer Turn On Delay Time		$t_{ON}$	0	—	0	—	ns
10	Output Buffer Turn Off Delay Time	*10	$t_{OFF}$	—	15	—	15	ns
11	Output Buffer Turn Off Delay Time from $\overline{RAS}$	*10	$t_{OFFR}$	—	15	—	15	ns
12	Output Buffer Turn Off Delay Time from $\overline{WE}$	*10	$t_{WEZ}$	—	15	—	15	ns
13	Transition Time		$t_T$	2	50	2	50	ns
14	$\overline{RAS}$ Precharge Time		$t_{RP}$	40	—	45	—	ns
15	$\overline{RAS}$ Pulse Width		$t_{RAS}$	60	100000	70	100000	ns
16	$\overline{RAS}$ Hold Time		$t_{RSH}$	15	—	20	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	*21	$t_{CRP}$	5	—	5	—	ns
18	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*11,12,22	$t_{RCD}$	20	45	20	50	ns
19	$\overline{CAS}$ Pulse Width		$t_{CAS}$	10	10000	15	10000	ns
20	$\overline{CAS}$ Hold Time		$t_{CSH}$	40	—	50	—	ns
21	$\overline{CAS}$ Precharge Time (Normal)	*19	$t_{CPN}$	10	—	10	—	ns
22	Row Address Set Up Time		$t_{ASR}$	0	—	0	—	ns
23	Row Address Hold Time		$t_{RAH}$	10	—	10	—	ns
24	Column Address Set Up Time		$t_{ASC}$	0	—	0	—	ns
25	Column Address Hold Time		$t_{CAH}$	10	—	15	—	ns
26	$\overline{RAS}$ to Column Address Delay Time	*13	$t_{RAD}$	15	30	15	35	ns
27	Column Address to $\overline{RAS}$ Lead Time		$t_{RAL}$	30	—	35	—	ns
28	Column Address to $\overline{CAS}$ Lead Time		$t_{CAL}$	30	—	35	—	ns
29	Read Command Set Up Time		$t_{RCS}$	0	—	0	—	ns
30	Read Command Hold Time Referenced to $\overline{RAS}$	*14	$t_{RRH}$	2	—	2	—	ns
31	Read Command Hold Time Referenced to $\overline{CAS}$	*14	$t_{RCH}$	0	—	0	—	ns
32	Write Command Set Up Time	*15	$t_{WCS}$	0	—	0	—	ns
33	Write Command Hold Time		$t_{WCH}$	10	—	10	—	ns
34	$\overline{WE}$ Pulse Width		$t_{WP}$	10	—	10	—	ns
35	Write Command to $\overline{RAS}$ Lead Time		$t_{RWL}$	15	—	15	—	ns
36	Write Command to $\overline{CAS}$ Lead Time		$t_{CWL}$	10	—	15	—	ns

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# MB814405D-60/60L/-70/70L

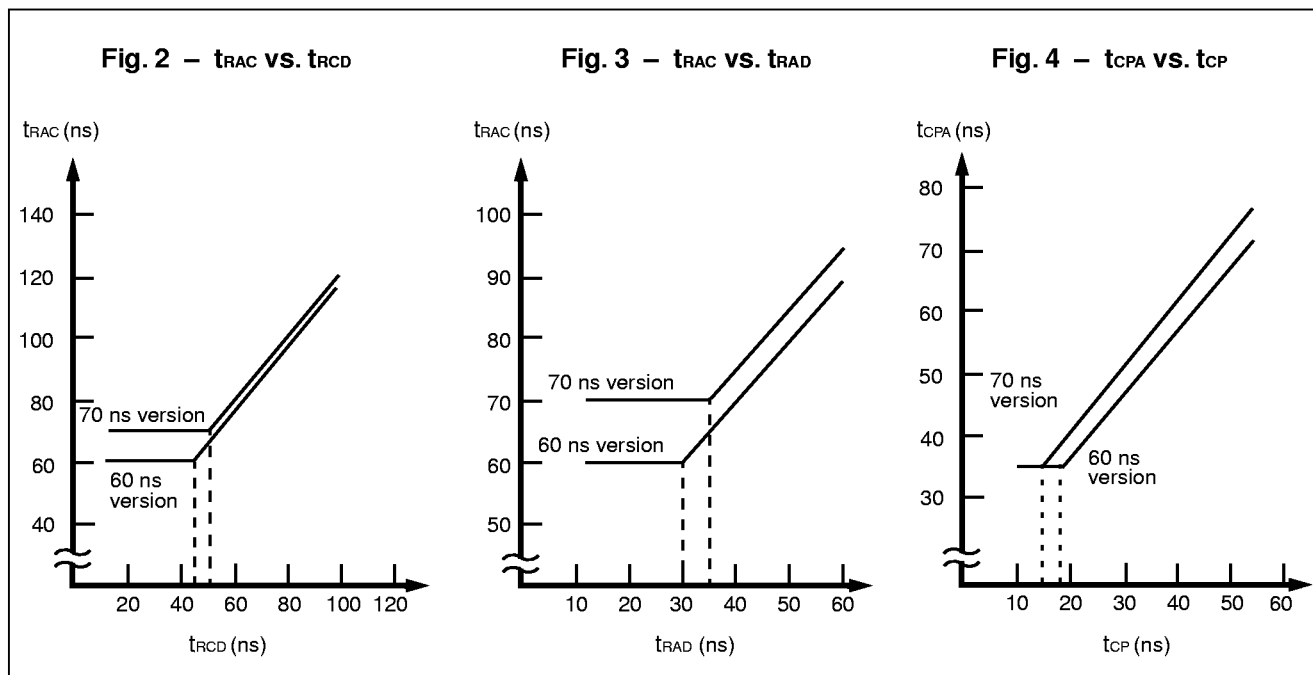
(Continued)

No.	Parameter	Notes	Symbol	MB814405D-60		MB814405D-70		Unit
				Min.	Max.	Min.	Max.	
37	DIN Set Up Time		t <sub>DS</sub>	0	—	0	—	ns
38	DIN Hold Time		t <sub>DH</sub>	10	—	10	—	ns
39	RAS to WE Delay Time		t <sub>RWD</sub>	80	—	95	—	ns
40	CAS to WE Delay Time		t <sub>CWD</sub>	40	—	45	—	ns
41	Column Address to WE Delay Time		t <sub>AWD</sub>	50	—	60	—	ns
42	RAS Precharge Time to CAS Active Time (Refresh Cycles)		t <sub>RPC</sub>	5	—	5	—	ns
43	CAS Set Up Time for CAS-before-RAS Refresh		t <sub>CSR</sub>	0	—	0	—	ns
44	CAS Hold Time for CAS-before-RAS Refresh		t <sub>CHR</sub>	10	—	10	—	ns
45	WE Set Up Time from RAS	*20	t <sub>WSR</sub>	10	—	10	—	ns
46	WE Hold Time from RAS	*20	t <sub>WHR</sub>	10	—	10	—	ns
47	Access Time from OE	*9	t <sub>OEA</sub>	—	15	—	20	ns
48	Output Buffer Turn Off Delay from OE	*10	t <sub>OEZ</sub>	—	15	—	15	ns
49	OE to RAS Lead Time for Valid Data		t <sub>OEL</sub>	10	—	10	—	ns
50	OE to CAS Lead Time		t <sub>COL</sub>	0	—	0	—	ns
51	OE Hold Time Referenced to WE	*16	t <sub>OEH</sub>	15	—	20	—	ns
52	OE to Data In Delay Time		t <sub>OED</sub>	15	—	20	—	ns
53	DIN to CAS Delay Time	*17	t <sub>DZC</sub>	0	—	0	—	ns
54	DIN to OE Delay Time	*17	t <sub>DZO</sub>	0	—	0	—	ns
55	OE Precharge Time		t <sub>OEP</sub>	10	—	10	—	ns
56	OE Hold Time Referenced to CAS		t <sub>OECH</sub>	5	—	7	—	ns
57	WE Precharge Time		t <sub>WPZ</sub>	10	—	10	—	ns
58	WE to Data In Delay Time		t <sub>WED</sub>	15	—	15	—	ns
59	RAS to Data In Delay Time		t <sub>RDD</sub>	15	—	15	—	ns
60	CAS to Data In Delay Time		t <sub>CDD</sub>	15	—	15	—	ns
61	RAS to Column Address Hold Time		t <sub>AR</sub>	45	—	50	—	ns
62	Write Command Hold Time Referenced to RAS		t <sub>WCR</sub>	45	—	50	—	ns
63	Data Input Hold Time Referenced to RAS		t <sub>DHR</sub>	45	—	50	—	ns
64	Hyper Page Mode Read/Write Cycle Time		t <sub>HPC</sub>	25	—	30	—	ns
65	Hyper Page Mode Read-Modify-Write Cycle Time		t <sub>HPRWC</sub>	73	—	85	—	ns
66	Access Time from CAS Precharge	*9,18	t <sub>CPA</sub>	—	35	—	35	ns
67	Hyper Page Mode CAS Precharge Time		t <sub>CP</sub>	10	—	10	—	ns
68	Hyper Page Mode RAS Pulse Width		t <sub>RASP</sub>	—	200000	—	200000	ns
69	Hyper Page Mode RAS Hold Time from CAS Precharge		t <sub>RHCP</sub>	35	—	40	—	ns
70	Hyper Page Mode CAS Precharge to WE Delay Time		t <sub>CPWD</sub>	55	—	65	—	ns

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- Notes:**
- \*1. Referenced to  $V_{SS}$ .
  - \*2.  $I_{CC}$  depends on the output load conditions and cycle rates; The specified values are obtained with the output open.  
 $I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$   
 $I_{CC1}$ ,  $I_{CC3}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  
 $I_{CC4}$  is specified at one time of address change during one Page cycle.
  - \*3. An Initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200  $\mu s$  is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
  - \*4. AC characteristics assume  $t_T = 2$  ns.
  - \*5.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
  - \*6. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$ ,  $t_{RAD} \leq t_{RAD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig. 2 and 3.
  - \*7. If  $t_{RCD} \geq t_{RCD}(\max)$ ,  $t_{RAD} \geq t_{RAD}(\max)$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{CAC}$ .
  - \*8. If  $t_{RAD} \geq t_{RAD}(\max)$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{AA}$ .
  - \*9. Measured with a load equivalent to two TTL loads and 100 pF.
  - \*10.  $t_{OFF}$ ,  $t_{OFFR}$ ,  $t_{WEZ}$  and  $t_{OEZ}$  is specified that output buffer change to high impedance state.
  - \*11. Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*12.  $t_{RCD}(\min) = t_{RAH}(\min) + 2t_T + t_{ASC}(\min)$ .
  - \*13. Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
  - \*15.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS}(\min)$  the data output pin will remain High-Z state through entire cycle.
  - \*16. Assumes that  $t_{WCS} < t_{WCS}(\min)$ .
  - \*17. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
  - \*18.  $t_{CPA}$  is access time from the selection of a new column address (that is caused by changing  $\overline{CAS}$  from "L" to "H"). Therefore, if  $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA}(\max)$  as shown in Fig. 4.
  - \*19. Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh.
  - \*20. Assumes that Test mode function.
  - \*21. The last  $\overline{CAS}$  rising edge.
  - \*22. The first  $\overline{CAS}$  falling edge.

# MB814405D-60/60L/-70/70L



## FUNCTIONAL TRUTH TABLE

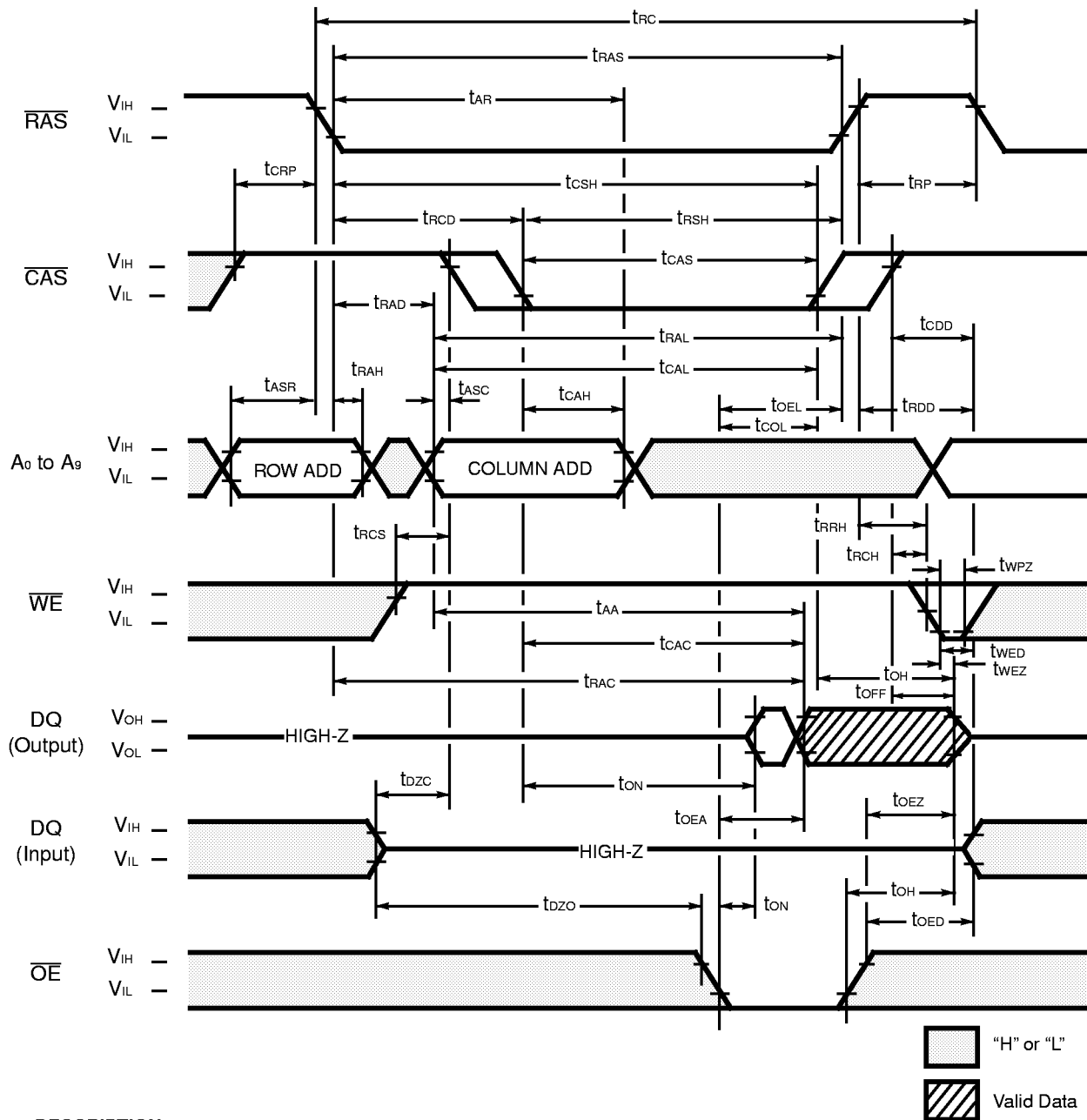
Operation Mode	Clock Input				Address Input		Input Data		Refresh	Note
	RAS	CAS	WE	OE	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes*	t <sub>RCS</sub> ≥ t <sub>RCS</sub> (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes*	t <sub>WCS</sub> ≥ t <sub>WCS</sub> (min)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes*	t <sub>CWD</sub> ≥ t <sub>CWD</sub> (min)
RAS-only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
CAS-before-RAS Refresh Cycle	L	L	H	X	—	—	—	High-Z	Yes	t <sub>CSR</sub> ≥ t <sub>CSR</sub> (min)
Hidden Refresh Cycle	H→L	L	H	L	—	—	—	Valid	Yes	Previous data is kept
Test Mode Set Cycle (CBR)	L	L	L	X	—	—	—	High-Z	Yes	t <sub>CSR</sub> ≥ t <sub>CSR</sub> (min) t <sub>WSR</sub> ≥ t <sub>WSR</sub> (min)
Test Mode Set Cycle (Hidden)	H→L	L	L	X	—	—	—	Valid	Yes	t <sub>CSR</sub> ≥ t <sub>CSR</sub> (min) t <sub>WSR</sub> ≥ t <sub>WSR</sub> (min)

X: "H" or "L"

\* : It is impossible in Hyper Page Mode.

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Fig. 5 – READ CYCLE



## DESCRIPTION

To implement a read operation, a valid address is latched by the  $\overline{RAS}$  and  $\overline{CAS}$  address strobes and with  $\overline{WE}$  set to a High level and  $\overline{OE}$  set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by  $\overline{RAS}(t_{TRAC})$ ,  $\overline{CAS}(t_{CAC})$ ,  $\overline{OE}$  ( $t_{OEA}$ ) or column addresses ( $t_{AA}$ ) under the following conditions:

If  $t_{RCD} > t_{RCD}(\text{max})$ , access time =  $t_{CAC}$ .

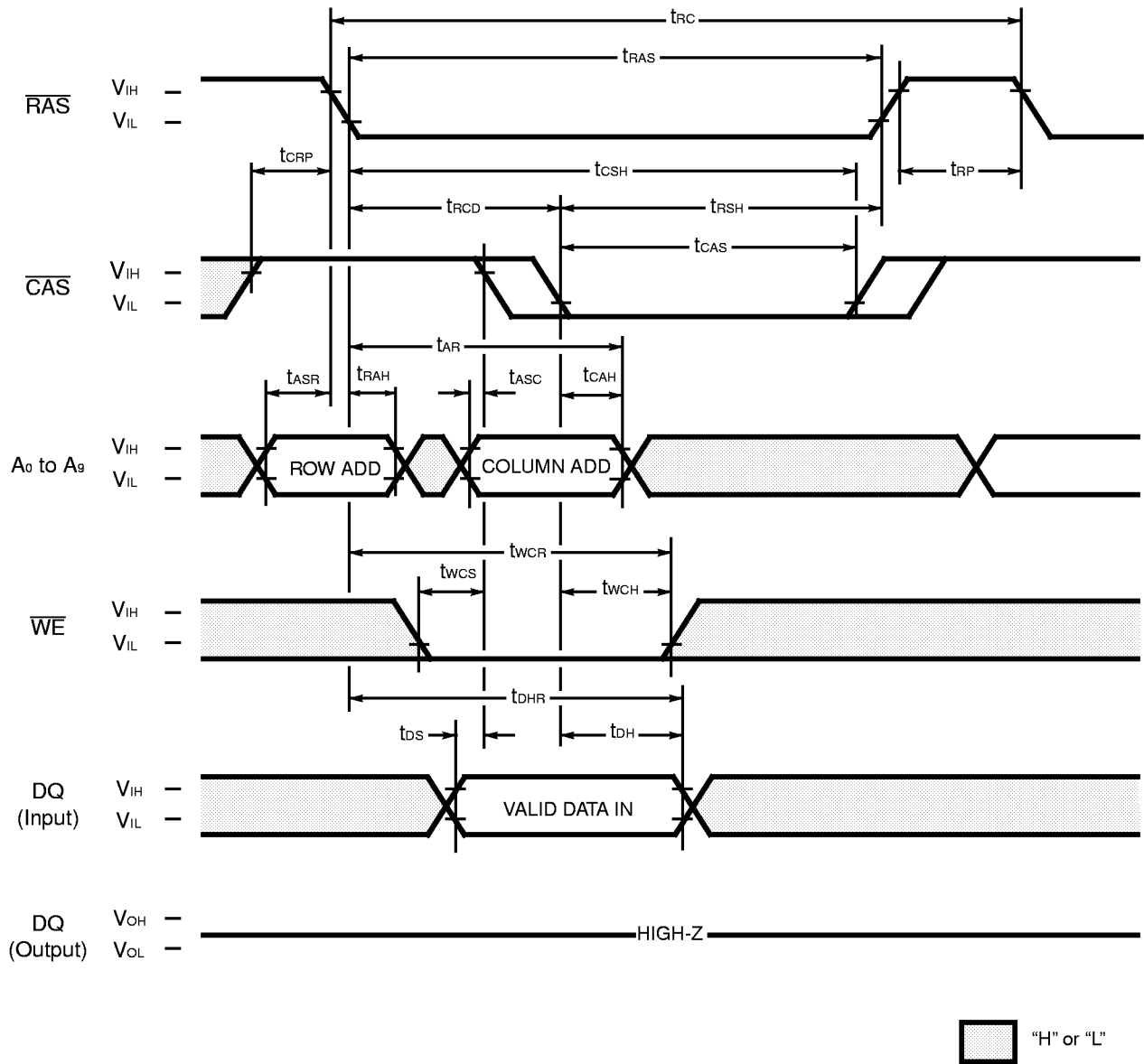
If  $t_{RAD} > t_{RAD}(\text{max})$ , access time =  $t_{AA}$ .

If  $\overline{OE}$  is brought Low after  $t_{TRAC}$ ,  $t_{CAC}$ , or  $t_{AA}$  (whichever occurs later), access time =  $t_{OEA}$ .

However, if either  $\overline{OE}$  or both  $\overline{RAS}$  and  $\overline{CAS}$  or  $\overline{OE}$  goes High, the output returns to a high-impedance state after  $t_{OH}$  is satisfied.

# MB814405D-60/60L/-70/70L

Fig. 6 – EARLY WRITE CYCLE

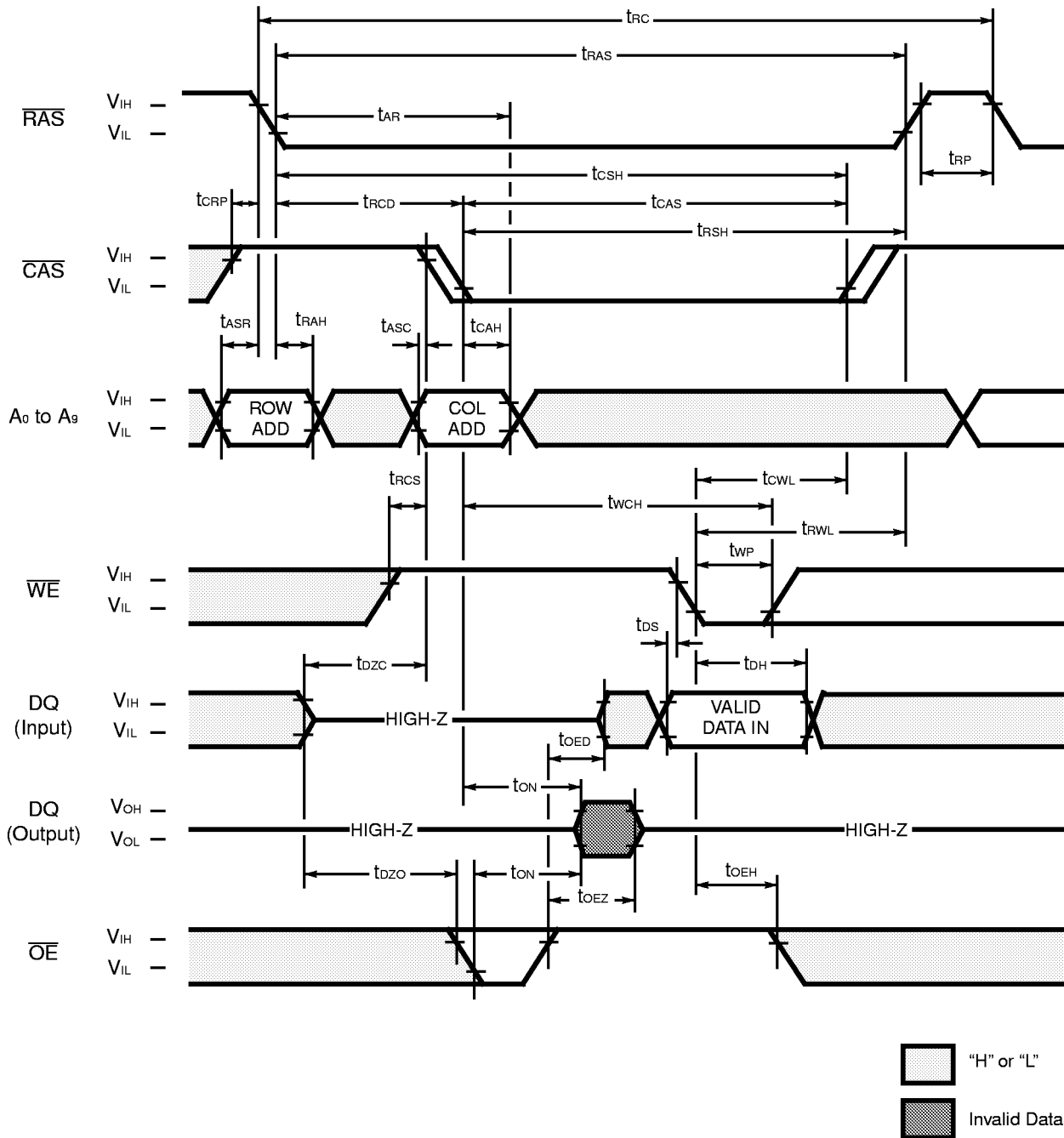


**DESCRIPTION**

A write cycle is similar to a read cycle except  $\overline{WE}$  is set to a Low state and  $\overline{OE}$  is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters  $t_{RWL}$ ,  $t_{CWL}$ ,  $t_{RAL}$  and  $t_{CAL}$  must be satisfied. In the early write cycle shown above  $t_{WCS}$  satisfied, data on the DQ pins are latched with the falling edge of  $\overline{CAS}$  and written into memory.

# MB814405D-60/60L/-70/70L

Fig. 7 – DELAYED WRITE CYCLE ( $\overline{OE}$  CONTROLLED)

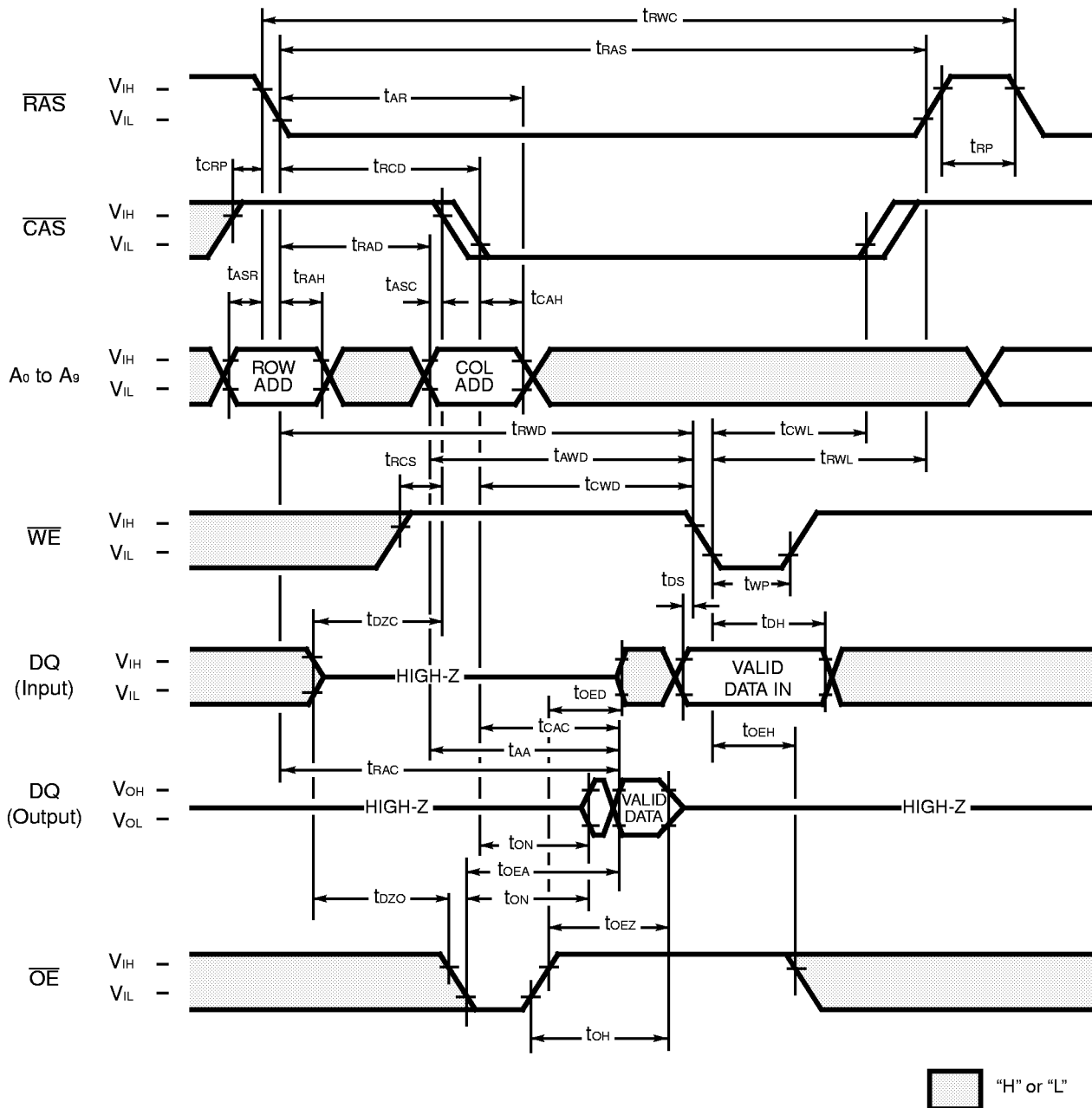


## DESCRIPTION

In the delayed write cycle,  $t_{wCS}$  is not satisfied; thus, the data on the DQ pins is latched with the falling edge of  $\overline{WE}$  and written into memory. The Output Enable ( $\overline{OE}$ ) signal must be changed from Low to High before  $\overline{WE}$  goes Low ( $t_{OED} + t_T + t_{DS}$ ).

# MB814405D-60/60L/-70/70L

Fig. 8 – READ-MODIFY-WRITE CYCLE

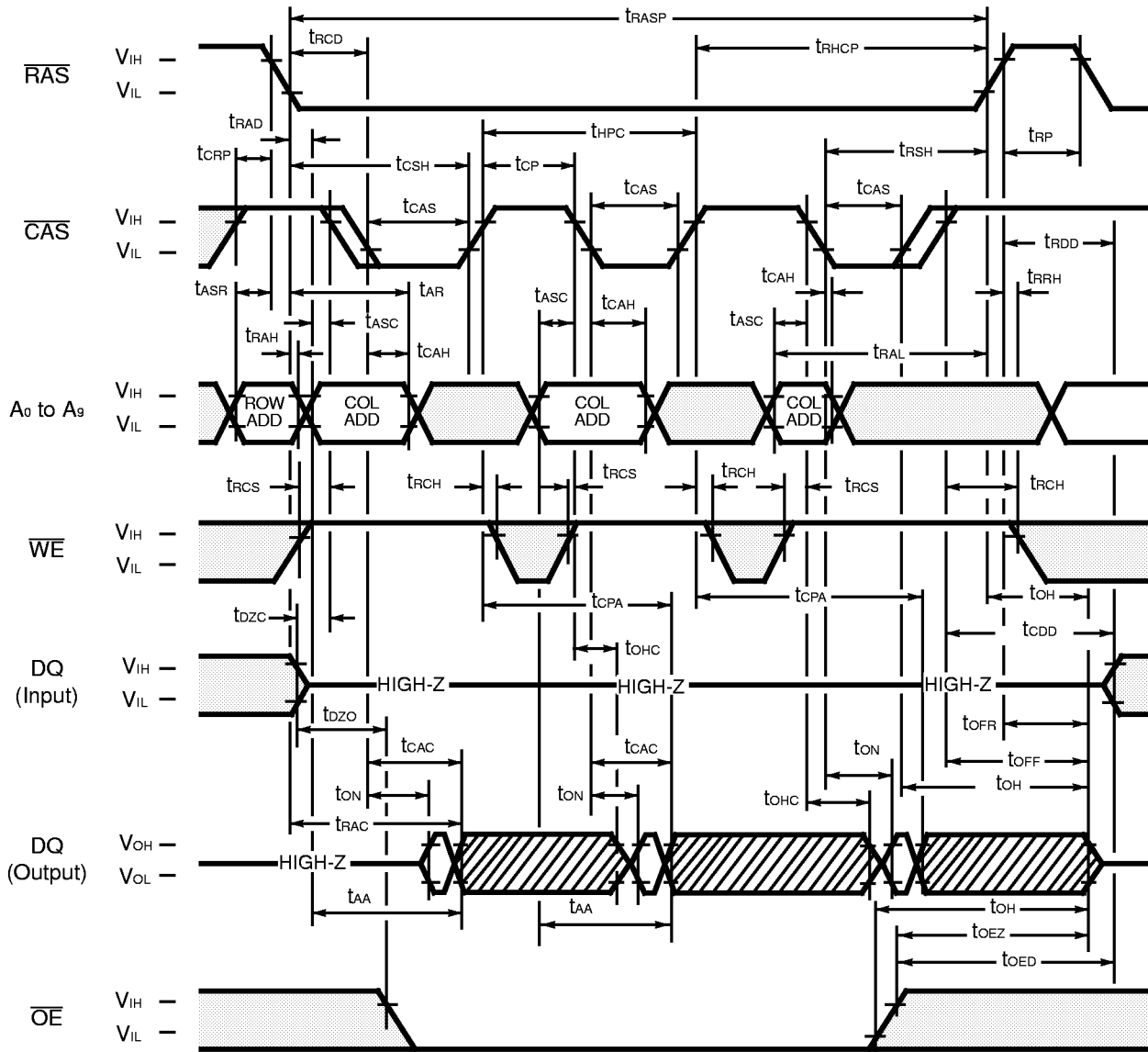


**DESCRIPTION**

The read-modify-write cycle is executed by changing  $\overline{WE}$  from High to Low after the data appears on the DQ pins. In the read-modify-write cycle,  $\overline{OE}$  must be changed from Low to High after the memory access time.

# MB814405D-60/60L/-70/70L

Fig. 9 – HYPER PAGE MODE READ CYCLE



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.



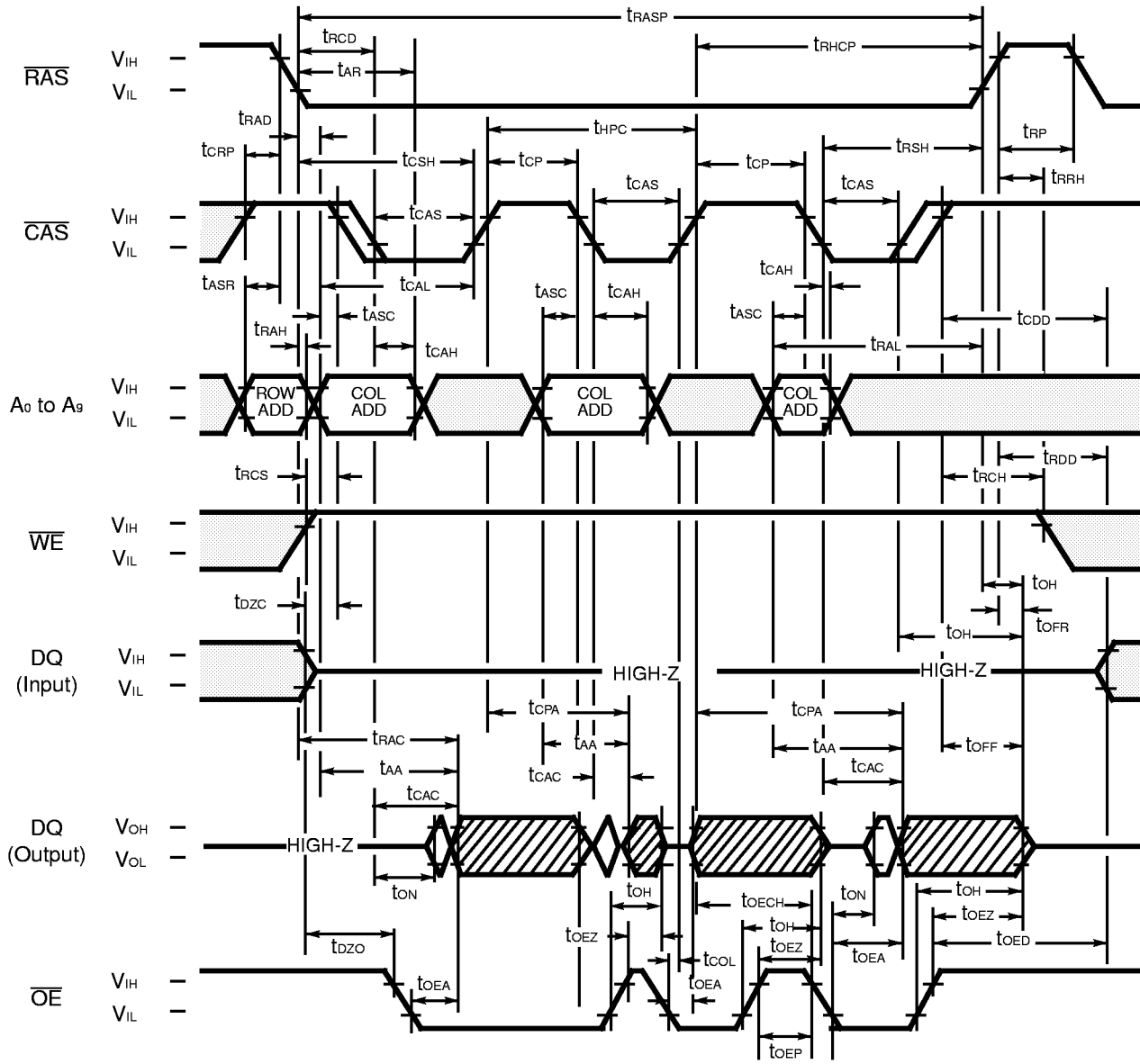
## DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining  $\overline{\text{RAS}}$  at a Low level during all successive memory cycles in which the row address is latched. The access time is determined by  $t_{\text{CAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CPA}}$ , or  $t_{\text{DEA}}$ , whichever one is the latest in occurring.



# MB814405D-60/60L/-70/70L

Fig. 10 – HYPER PAGE MODE READ CYCLE ( $\overline{OE}$  CONTROLLED)



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.



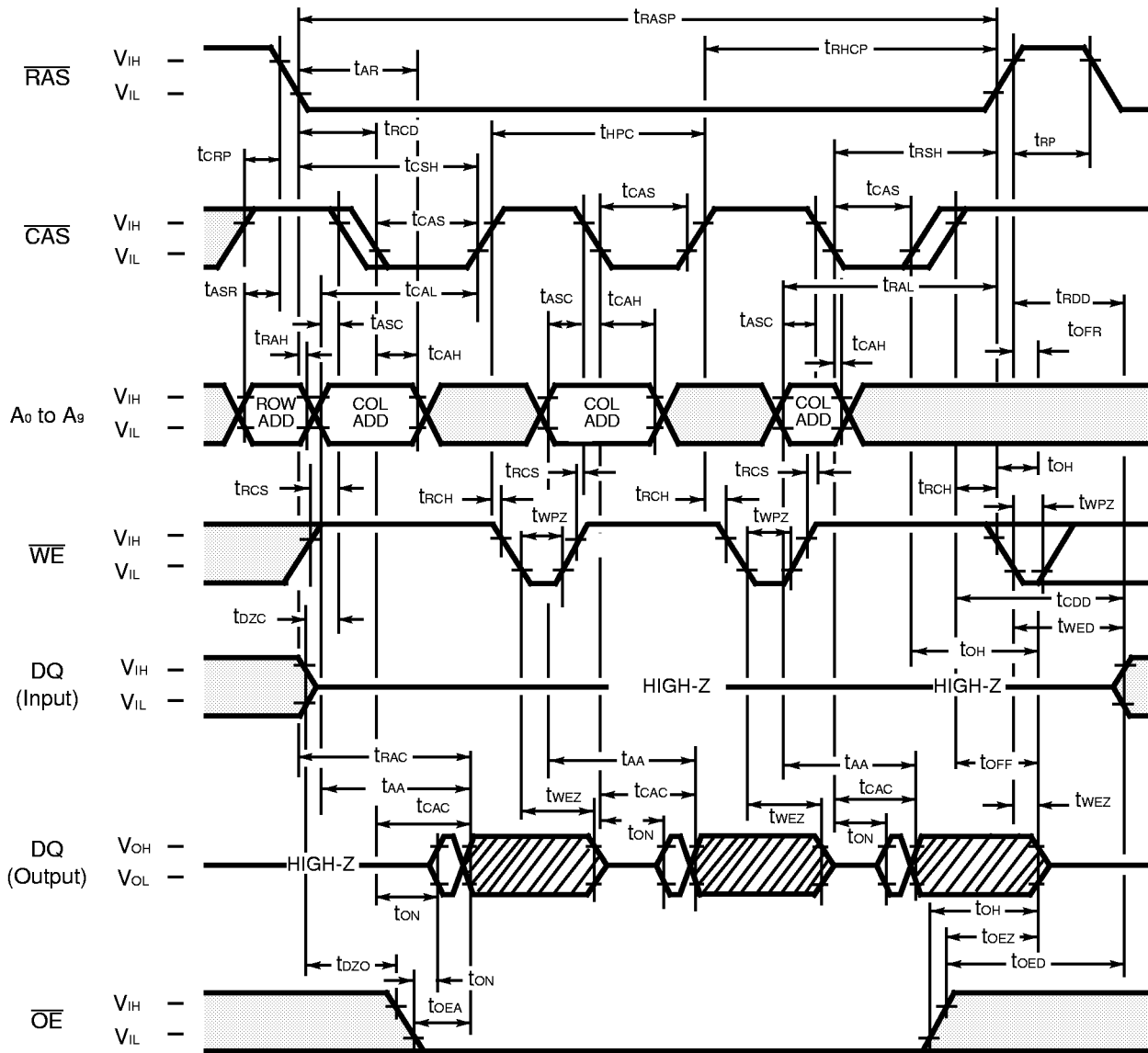
## DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining  $\overline{RAS}$  at a Low level and  $\overline{WE}$  at a High level during all successive memory cycles in which the row address is latched. The access time is determined by  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ , or  $t_{OEA}$ , whichever one is the latest in occurring.

To obtain a high-impedance state, set  $\overline{OE}$  or both  $\overline{RAS}$  and  $\overline{CAS}$  going high level.

# MB814405D-60/60L/-70/70L

Fig. 11 – HYPER PAGE MODE READ CYCLE ( $\overline{WE}$  CONTROLLED)



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

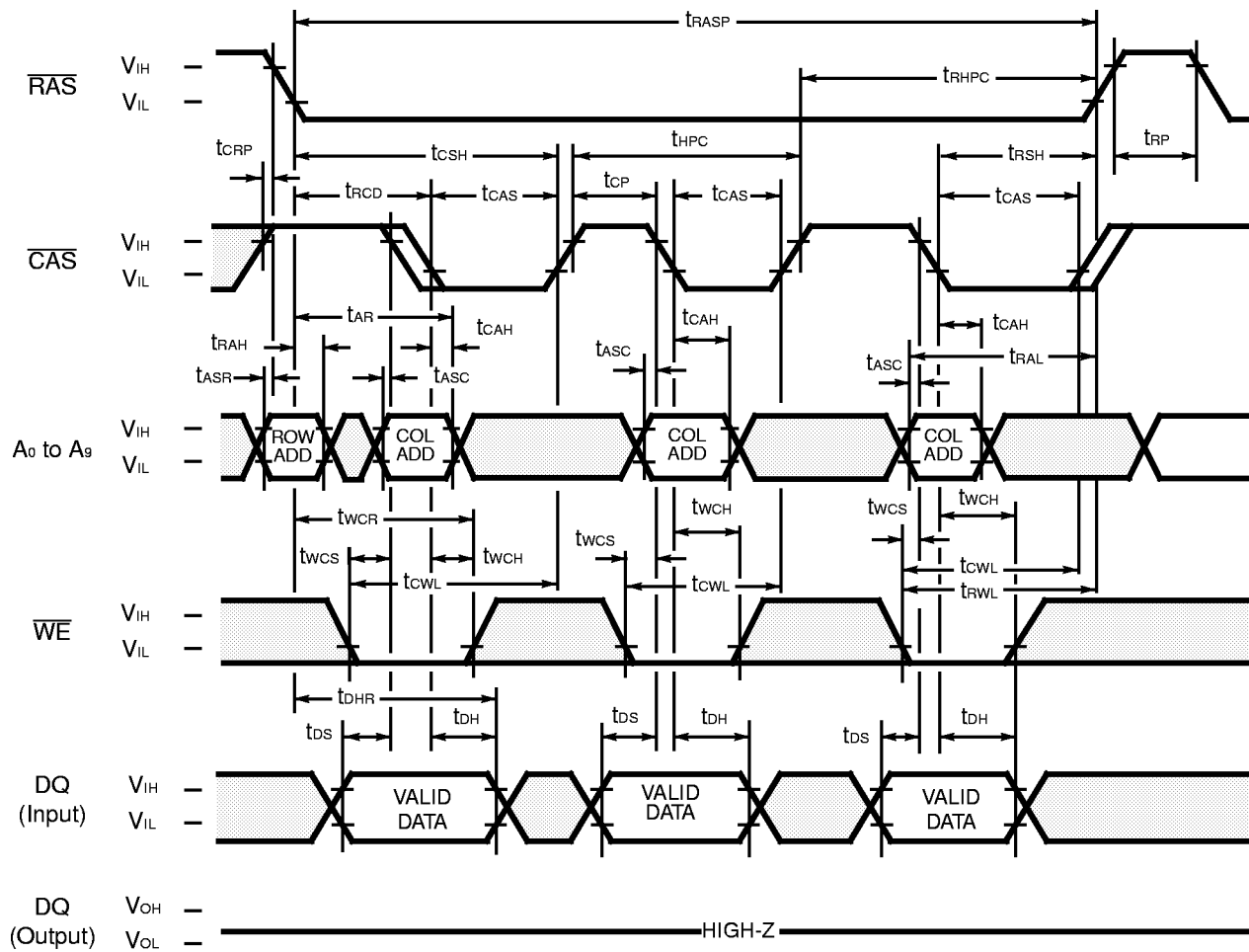


### DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining  $\overline{RAS}$  at a Low level and  $\overline{WE}$  at a High level during all successive memory cycles in which the row address is latched. The address time is determined by  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ , or  $t_{OEA}$ , whichever one is the latest in occurring.

To obtain a high-impedance state, confirm either of the following conditions,  $\overline{OE}$  set to a high level or  $\overline{WE}$  set to a low level after  $\overline{CAS}$  set to a high level or  $\overline{RAS}$  and  $\overline{CAS}$  set to a high level.

**Fig. 12 – HYPER PAGE MODE EARLY WRITE CYCLE**



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

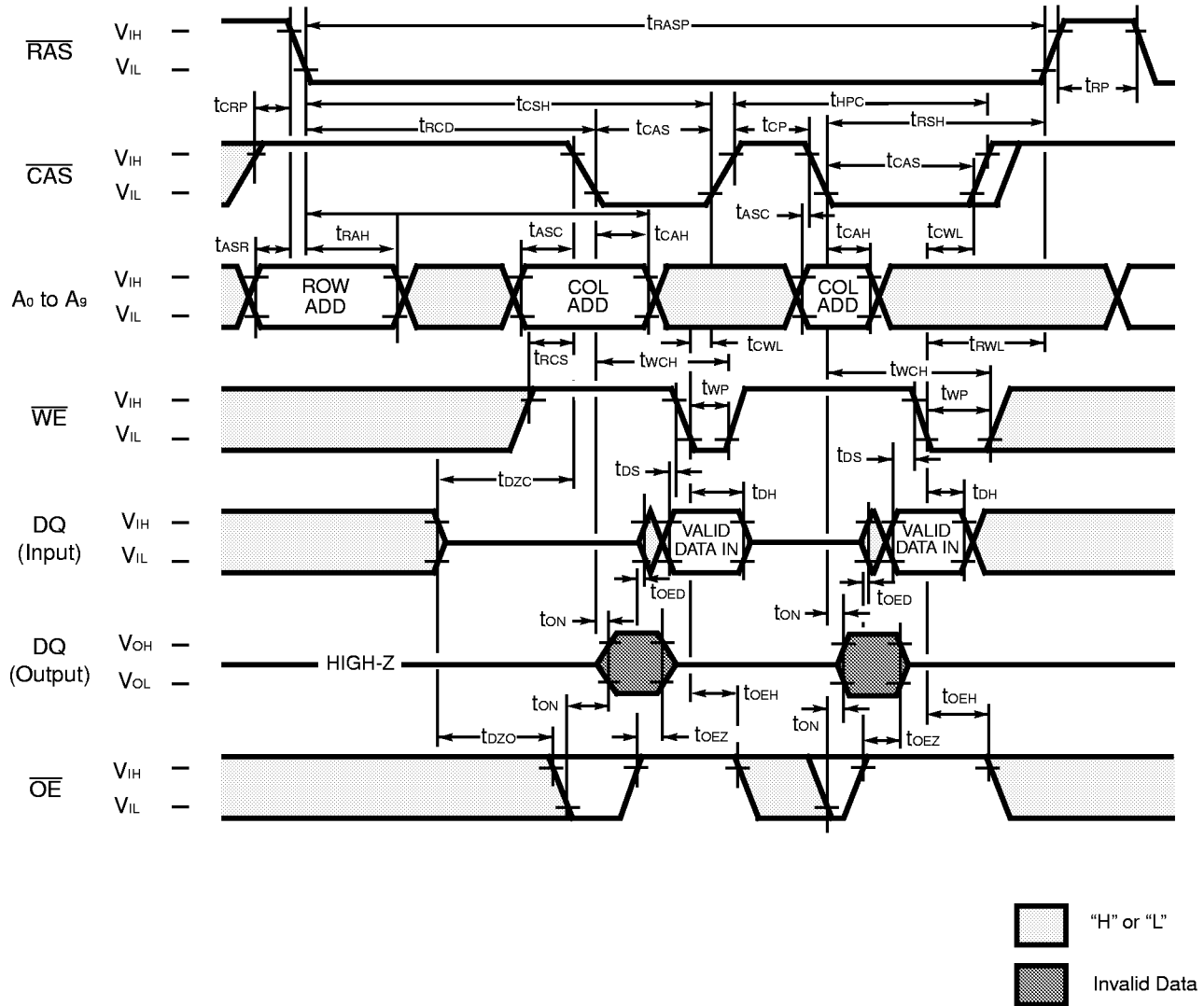


**DESCRIPTION**

The hyper page mode early write cycle is executed in the same manner as the hyper page mode read cycle except  $\overline{WE}$  is set to a low state and  $\overline{OE}$  is a "H" or "L" signal. Data appearing on the DQ pins is latched on the falling edge of  $\overline{CAS}$  and the data is written into the memory. During the hyper page mode write cycle, including the delayed ( $\overline{OE}$ ) write and read-modify-write cycles,  $t_{cwl}$  must be satisfied.

# MB814405D-60/60L/-70/70L

Fig. 13 – HYPER PAGE MODE DELAYED WRITE CYCLE ( $\overline{OE}$  CONTROLLED)

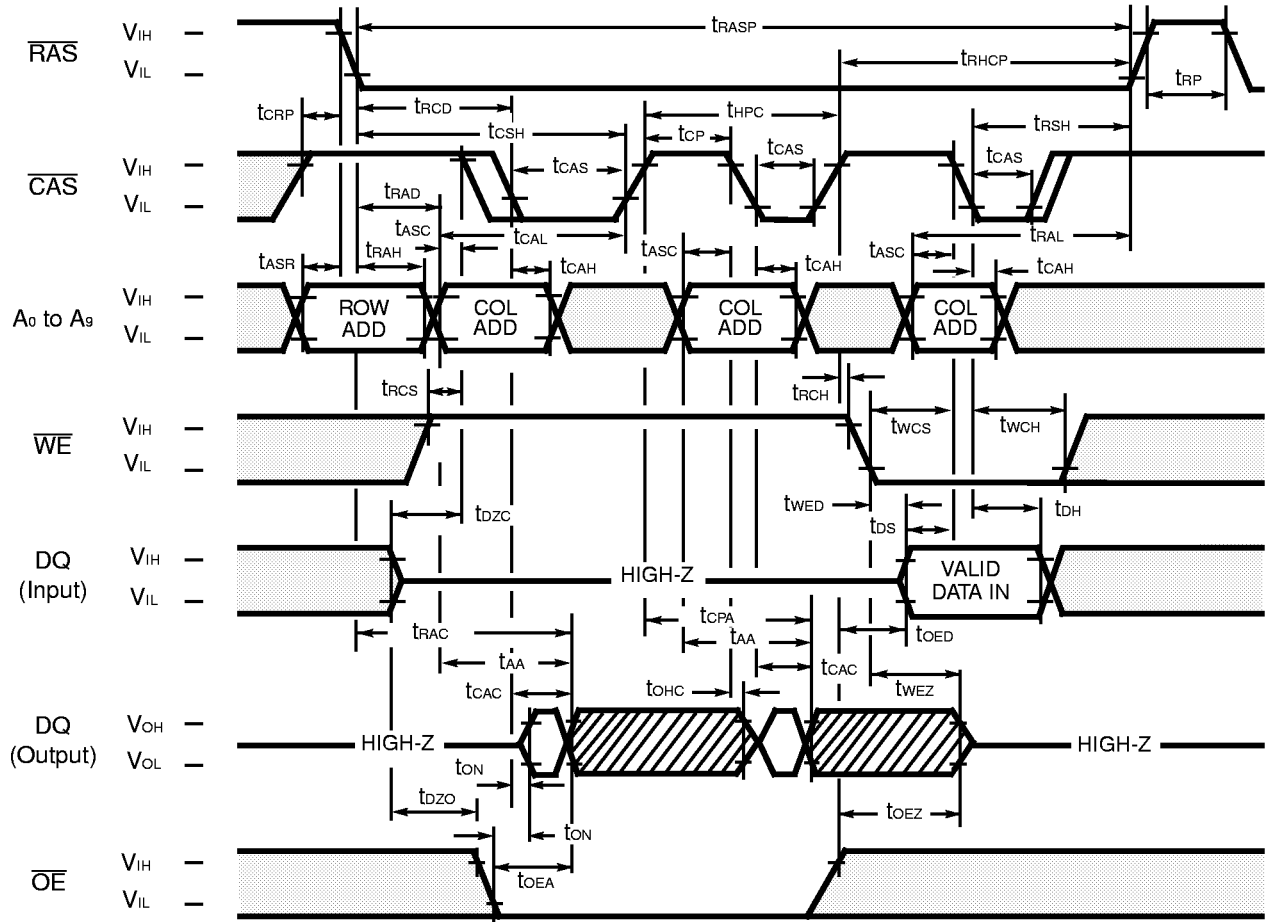


## DESCRIPTION

The hyper page mode delayed write cycle is executed in the same manner as the hyper page mode early write cycle except for the states of  $\overline{WE}$  and  $\overline{OE}$ . Input data on the DQ pins are latched on the falling edge of  $\overline{WE}$  and written into memory. In the hyper page mode delayed write cycle,  $\overline{OE}$  must be changed from Low to High before  $\overline{WE}$  goes Low ( $t_{OED} + t_r + t_{DS}$ ).

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Fig. 14 – HYPER PAGE MODE READ/WRITE MIXED CYCLE

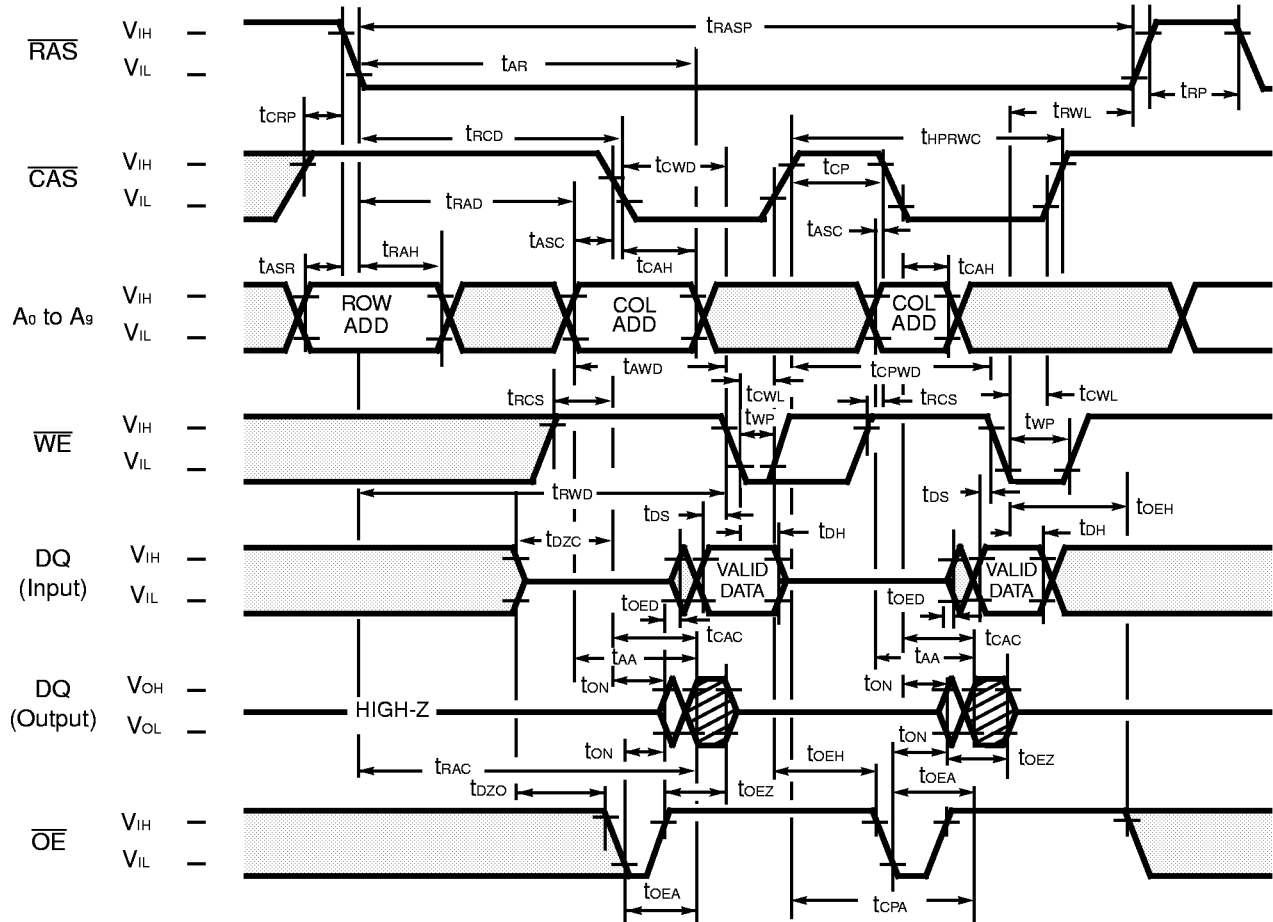


**DESCRIPTION**

The hyper page mode performs read/write operations repetitively during one  $\overline{RAS}$  cycle. At this time,  $t_{HPC}$  (min) is invalid.

# MB814405D-60/60L/-70/70L

Fig. 15 – HYPER PAGE MODE READ-MODIFY-WRITE CYCLE

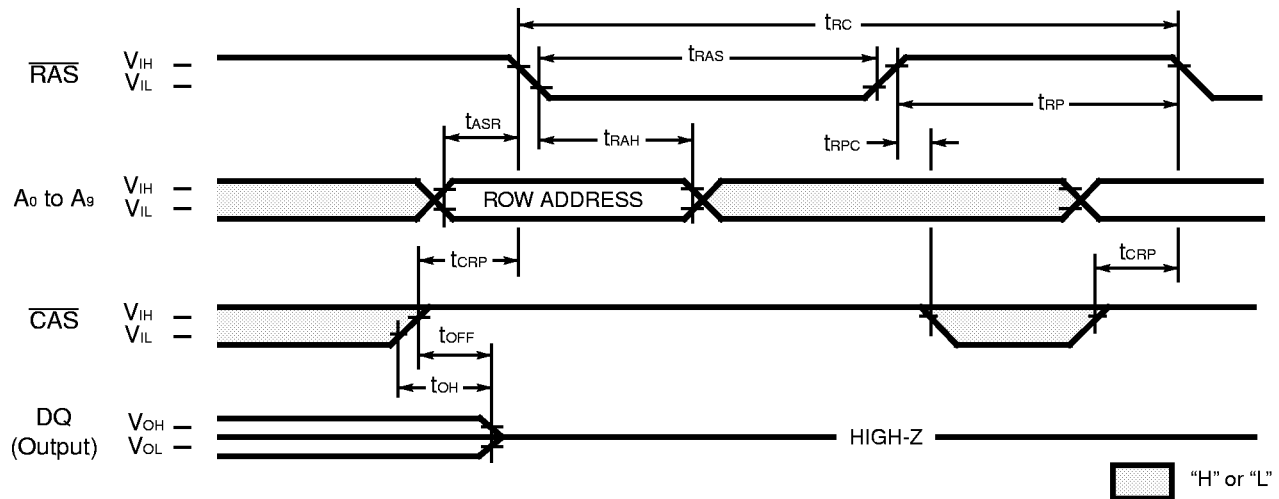


**DESCRIPTION**

During the hyper page mode of operation, the read-modify-write cycle can be executed by switching  $\overline{WE}$  from High to Low after input data appears at the DQ pins during a normal cycle.

# MB814405D-60/60L/-70/70L

Fig. 16 –  $\overline{\text{RAS}}$ -ONLY REFRESH ( $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"} \text{ or } \text{"L"} \text{"}$ )

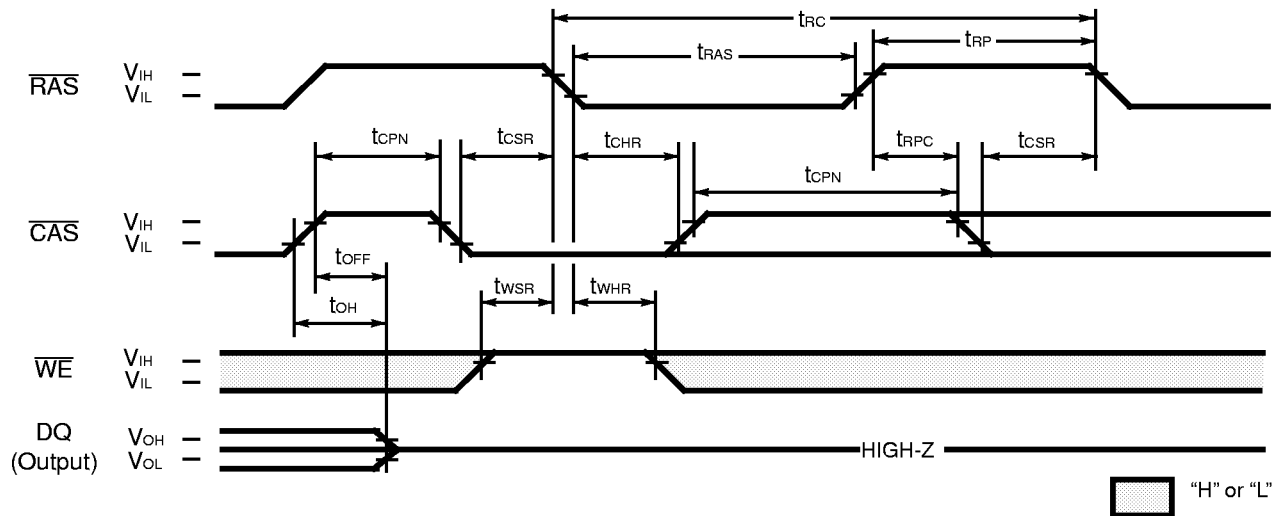


## DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1,024 row addresses every 16.4-milliseconds. Three refresh modes are available:  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping  $\overline{\text{RAS}}$  Low and  $\overline{\text{CAS}}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{\text{RAS}}$ . During  $\overline{\text{RAS}}$ -only refresh, DQ pins are kept in a high-impedance state.

Fig. 17 –  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH (ADDRESSES =  $\overline{\text{OE}} = \text{"H"} \text{ or } \text{"L"} \text{"}$ )



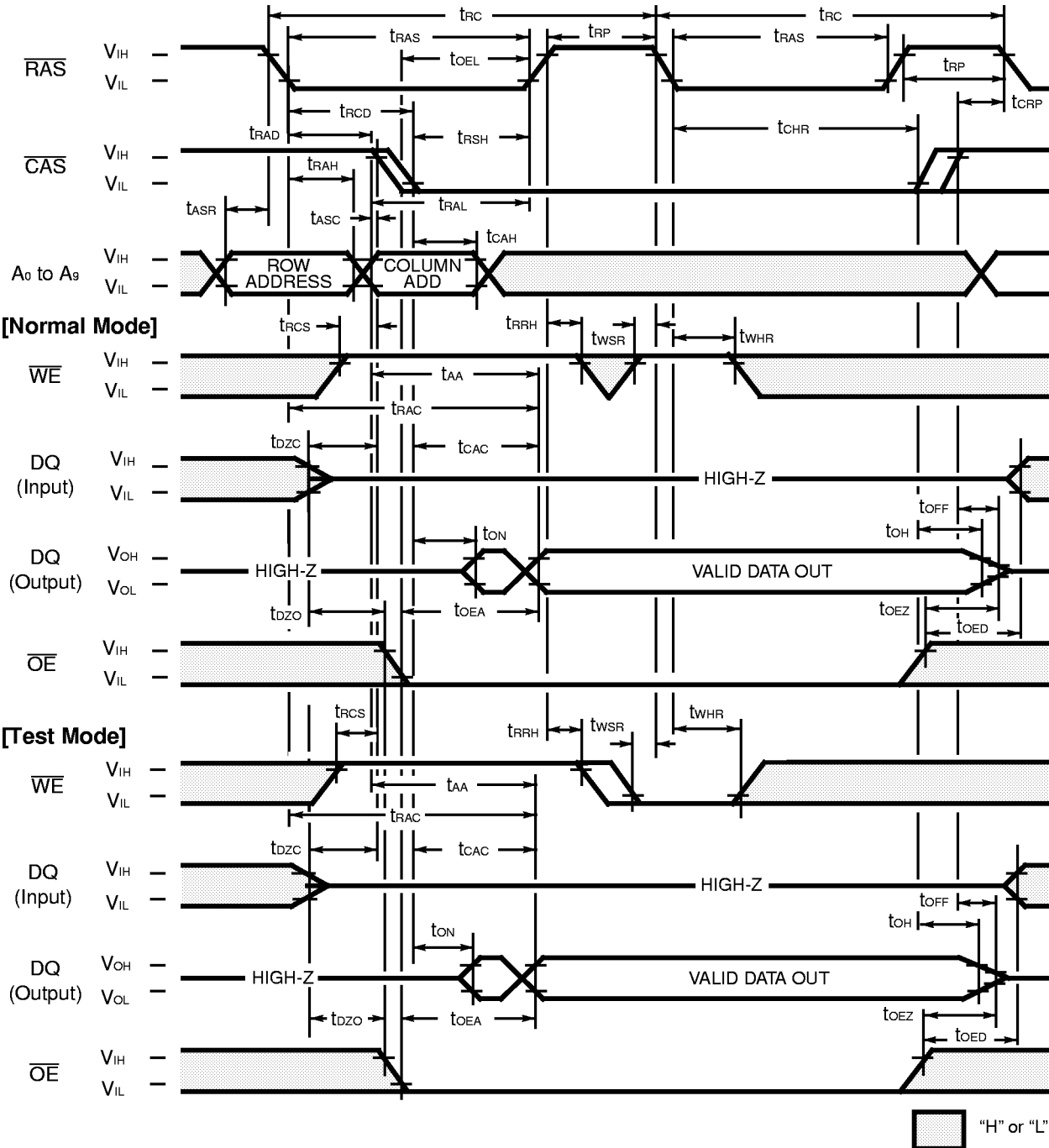
## DESCRIPTION

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{CAS}}$  is held Low for the specified setup time ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes Low, the on-chip refresh control generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh operation.

$\overline{\text{WE}}$  must be held High for the specified set up time ( $t_{\text{WSR}}$ ) before  $\overline{\text{RAS}}$  goes Low in order not to enter "Test Mode".

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Fig. 18 – HIDDEN REFRESH CYCLE



**DESCRIPTION**

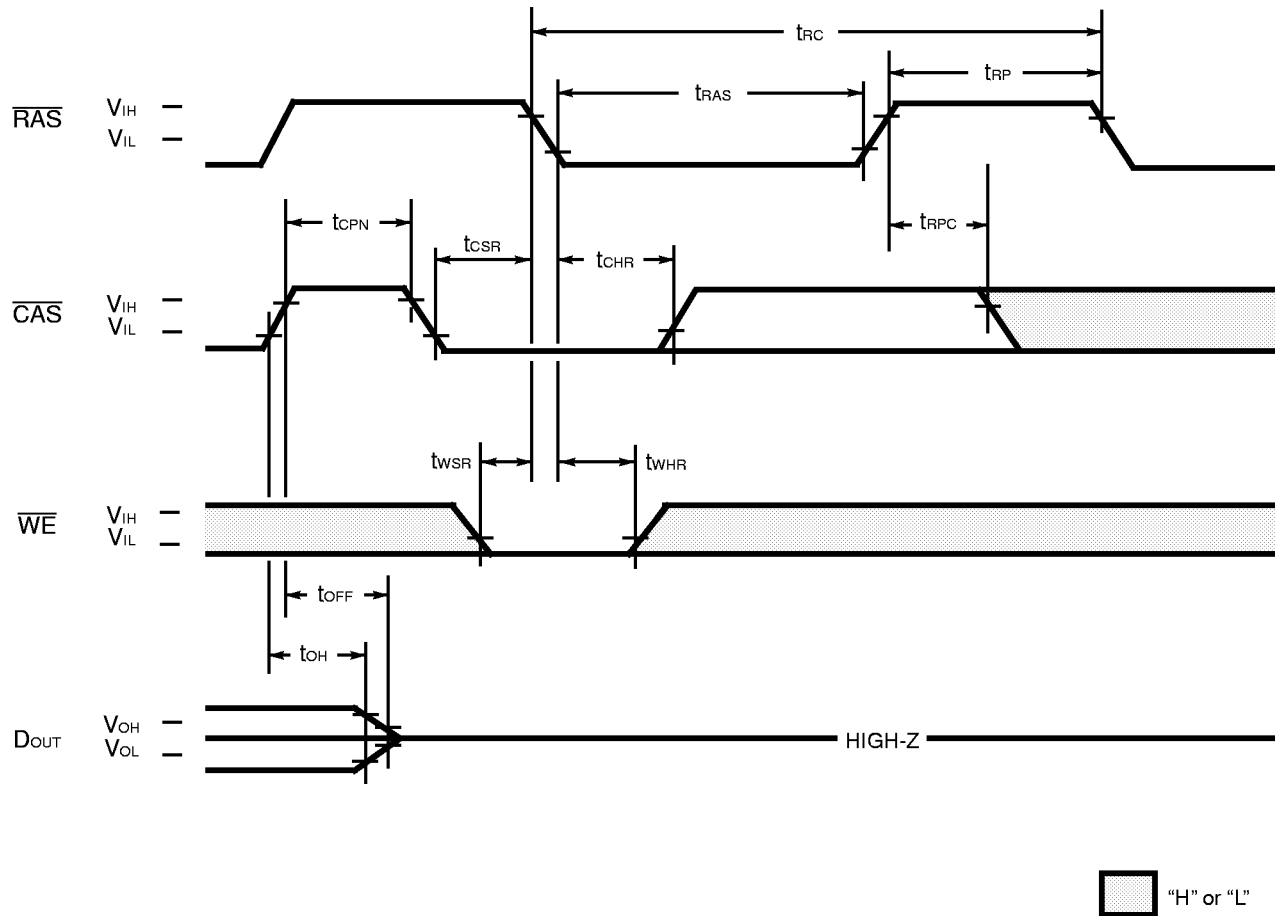
A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{\text{CAS}}$  and cycling  $\overline{\text{RAS}}$ . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability.

$\overline{\text{WE}}$  must be held High for the specified set up time ( $t_{WSR}$ ) before  $\overline{\text{RAS}}$  goes Low in order not to enter "Test Mode".



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Fig. 19 – TEST MODE SET CYCLE ( $A_0$  to  $A_9$ ,  $\overline{OE} = \text{“H” or “L”}$ )



## DESCRIPTION

Test Mode;

The purpose of this test mode is to reduce device test time to half of that required to test the device conventionally.

The test mode function is entered by performing a  $\overline{WE}$  and  $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) refresh for the entry cycle.

In the test mode, read and write operations are executed in units of eight bits which are selected by the address combination of  $CA_0$ .

In the write mode, data is written into eight cells simultaneously. But the data must be input from all DQ pins. In the read mode, the data of eight cells at the selected addresses are read out from DQ and checked in the following manner.

When the eight bits are all "L" or all "H", a "H" level is output.

When the eight bits show a combination of "L" and "H", a "L" level is output.

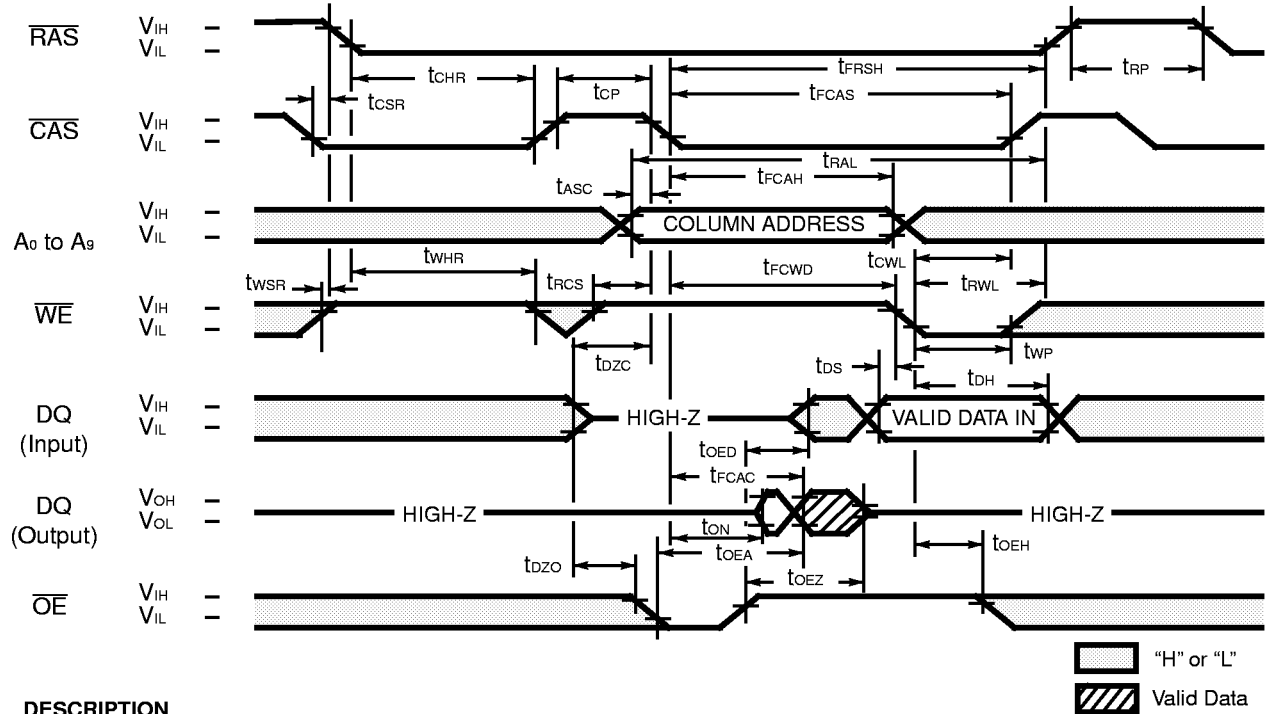
The test mode function is exited by performing a  $\overline{RAS}$ -only refresh or a  $\overline{CAS}$ -before- $\overline{RAS}$  refresh for the exit cycle.

In test mode operation, the following parameters are delayed approximately 5 ns from the specified value in the data sheet.

$t_{RC}$ ,  $t_{RWC}$ ,  $t_{RAS}$ ,  $t_{AA}$ ,  $t_{TRAS}$ ,  $t_{CSH}$ ,  $t_{RAL}$ ,  $t_{RWD}$ ,  $t_{AWD}$ ,  $t_{HPC}$ ,  $t_{HPRWC}$ ,  $t_{CPA}$ ,  $t_{RHP}$ ,  $t_{CPWD}$

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**Fig. 20 –  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH COUNTER TEST CYCLE**



**DESCRIPTION**

A special timing sequence using the  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle provides a convenient method to verify the functionality of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh circuitry. If, after a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle,  $\overline{\text{CAS}}$  makes a transition from High to Low while  $\overline{\text{RAS}}$  is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

- Row Address: Bits  $A_0$  through  $A_9$  are defined by the on-chip refresh counter.
- Column Address: Bits  $A_0$  through  $A_9$  are defined by latching levels on  $A_0$  to  $A_9$  at the second falling edge of  $\overline{\text{CAS}}$ .

The  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Counter Test procedure is as follows ;

- 1) Normalize the internal refresh address counter by using 8  $\overline{\text{RAS}}$ -only refresh cycles.
- 2) Use the same column address throughout the test.
- 3) Write "0" to all 1,024 row addresses at the same column address by using normal write cycles.
- 4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test (read-modify-write cycles). Repeat this procedure 1,024 times with addresses generated by the internal refresh address counter.
- 5) Read and check data written in procedure 4) by using normal read cycle for all 1,024 memory locations.
- 6) Reverse test data and repeat procedures 3), 4), and 5).

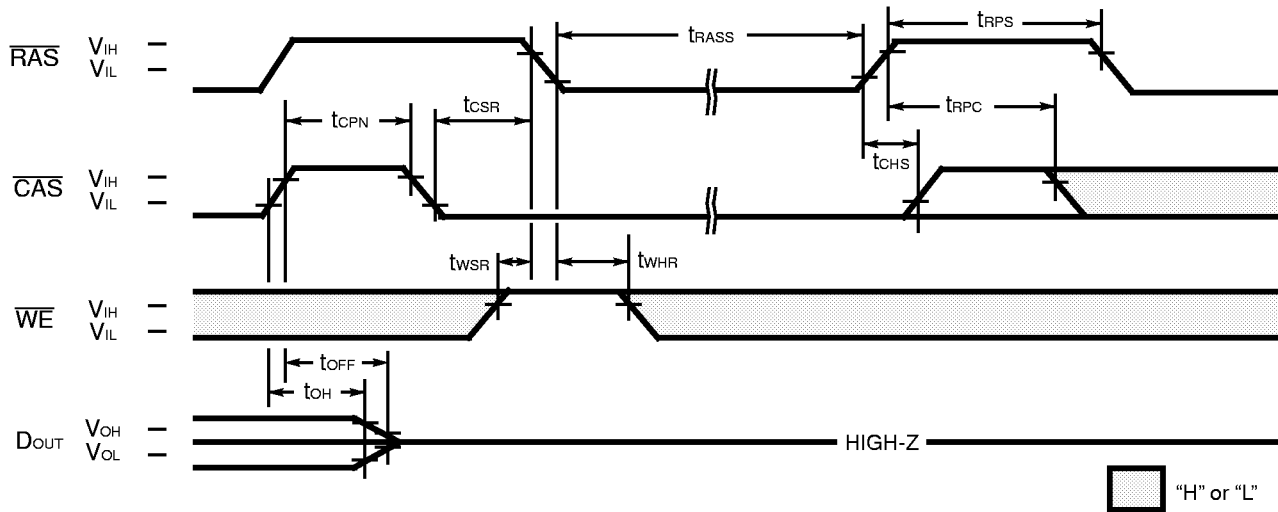
(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB814405D-60		MB814405D-70		Unit
			Min.	Max.	Min.	Max.	
90	Access Time from $\overline{\text{CAS}}$	$t_{\text{FCAC}}$	—	15	—	20	ns
91	Column Address Hold Time	$t_{\text{FCAH}}$	10	—	10	—	ns
92	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{FCWD}}$	40	—	45	—	ns
93	$\overline{\text{CAS}}$ Pulse Width	$t_{\text{FCAS}}$	10	—	15	—	ns
94	$\overline{\text{RAS}}$ Hold Time	$t_{\text{FRSH}}$	15	—	20	—	ns
95	$\overline{\text{CAS}}$ Precharge Time	$t_{\text{CPT}}$	10	—	10	—	ns

**Note:** Assumes that  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle only.

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Fig. 21 – SELF REFRESH CYCLE ( $A_0$  to  $A_9 = \overline{OE} = \text{“H” or “L”}$ )



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB814405D-60		MB814405D-70		Unit
			Min.	Max.	Min.	Max.	
100	$\overline{RAS}$ Pulse Width	$t_{RASS}$	100	—	100	—	$\mu\text{s}$
101	$\overline{RAS}$ Precharge Time	$t_{RPS}$	105	—	125	—	ns
102	$\overline{CAS}$ Hold Time	$t_{CHS}$	-50	—	-50	—	ns

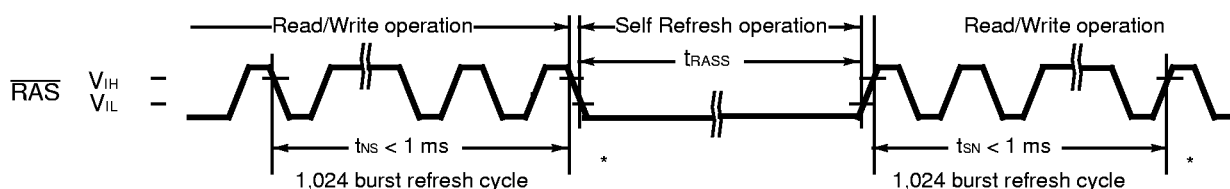
**Note:** Assumes Self Refresh cycle only.

## DESCRIPTION

The Self Refresh cycle provides a refresh operation without external clock and external Address. Self Refresh control circuit on chip is operated in the Self Refresh cycle and refresh operation can be automatically executed using internal refresh address counter. If  $\overline{CAS}$  goes to “L” before  $\overline{RAS}$  goes to “L” (CBR) and the condition of  $\overline{CAS}$  “L” and  $\overline{RAS}$  “L” is kept for term of  $t_{RASS}$  (more than 100  $\mu\text{s}$ ), the device can be entered the Self Refresh cycle. And after that, refresh operation is automatically executed per fixed interval using internal refresh address counter during “ $\overline{RAS}=\text{L}$ ” and “ $\overline{CAS}=\text{L}$ ”. And exit from Self Refresh cycle is performed by toggling of  $\overline{RAS}$  and  $\overline{CAS}$  to “H” with specifying  $t_{CHS}$  min.

Restriction for Self Refresh operation ;  
For Self Refresh operation, the notice below must be considered.

- 1) In the case that distribute CBR refresh are operated in read/write cycles  
Self Refresh cycles can be executed without special rule if 1,024 cycles of distribute CBR refresh are executed within  $t_{REF}$  max.
- 2) In the case that burst CBR refresh or  $\overline{RAS}$ -only refresh are operated in read/write cycles  
1,024 times of burst CBR refresh or 1,024 times of burst  $\overline{RAS}$ -only refresh must be executed before and after Self Refresh cycles.



\* Read/Write operation can be performed non refresh time within  $t_{NS}$  or  $t_{SN}$

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## ■ PACKAGE DIMENSIONS

