MIC5009CN T-51-19

Counter Time-Base Circuit

General Description

The MIC5009 is a highly versatile MOS oscillator and divider chain manufactured by Micrel using a depletion-load ion-implantation process and P-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36 x 10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination, the internal oscillator with an external crystal, or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

The MIC5009 consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36 x 10^8 counter stages, which are fully synchronous with each other.

With an input frequency of 1MHz, the MIC5009 provides the basic time periods necessary for most frequency measuring instruments, i.e., 1µS through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1MHz input. Using a 1/1.2 MHz input, the MIC5009 can also provide a 50/60Hz output for accurate generation of line frequencies in portable instruments or clocks.

Features

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- Operates DC to above 1MHz
- Binary-encoded for frequency selection
- Resettable to highest or lowest state
- Twenty different modes of division

Ordering Information

Part Number	Temperature Range	Package
MIC5009CN	0°C to 70°C	16-pin Plastic DIP

Functional Diagram

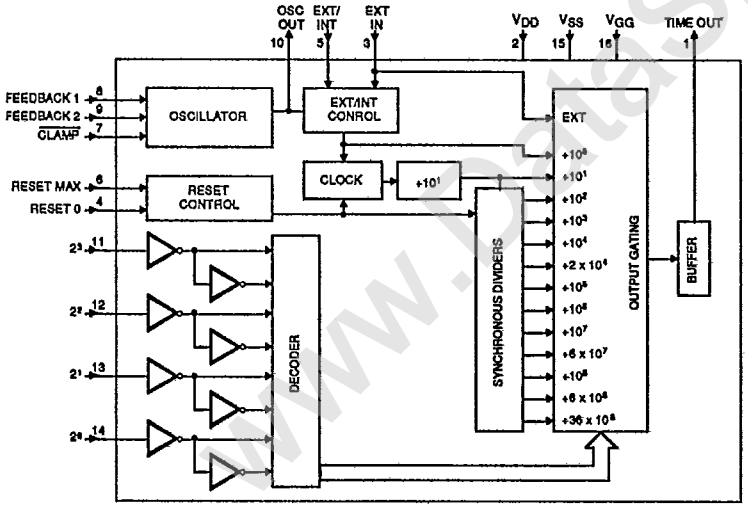
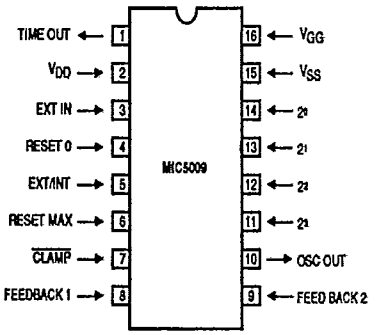


Figure 1

Pin Configuration



T-51-19

The time-base output (TIME OUT) is a square wave; its frequency is determined by the selected counter division, and by the oscillator or external input frequency. The falling edge of the output square wave should be used to control external circuitry.

Division Modes vs. Control Inputs

Table 1

DIVISION SELECTORS 2^3	2^2	2^1	2^0	NORMAL Mode 0 $R_{MAX} = 0$ $R_0 = 0$	BYPASS MODES Mode 1 $R_{MAX} = V_{GG}$ $R_0 = 0$	Mode 2 $R_{MAX} = 0$ $R0 = V_{GG}$	Mode 3 $R_{MAX} = V_{GG}$ $R0 = V_{GG}$
0	0	0	1	$+10^1$	$+10^1$	$+10^1$	$+10^1$
0	0	1	0	$+10^2$	$+10^2$	$+10^2$	$+10^2$
0	0	1	1	$+10^3$	$+10^3$	$+10^3$	$+10^3$
0	1	0	0	$+10^4$	$+10^4$	$+10^4$	$+10^4$
0	1	0	1	$+10^5$	$+10^2$	$+10^5$	$+10^2$
0	1	1	0	$+10^6$	$+10^3$	$+10^6$	$+10^3$
0	1	1	1	$+10^7$	$+10^4$	$+10^7$	$+10^4$
1	0	0	0	$+10^8$	$+10^5$	$+10^5$	$+10^5$
1	0	0	1	$+6 \times 10^7$	$+6 \times 10^4$	$+6 \times 10^4$	$+6 \times 10^1$
1	0	1	0	$+36 \times 10^8$	$+36 \times 10^5$	$+36 \times 10^5$	$+36 \times 10^2$
1	0	1	1	$+6 \times 10^8$	$+6 \times 10^5$	$+6 \times 10^5$	$+6 \times 10^2$
1	1	1	0	$+2 \times 10^4$	$+2 \times 10^1$	$+2 \times 10^1$	$+2 \times 10^1$

* SPECIAL ADDRESSES:

0000 - Oscillator signal selected by EXT/INT appears at TIME OUT
1100 or 1101 - Forces TIME OUT to logic 0 level
1111 - Signal at EXT IN appears at TIME OUT
Logic 1 = High = V_{SS}
Logic 0 = Low = V_{DD}

6

RC Operation

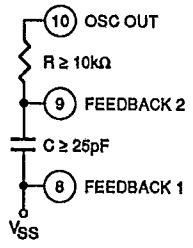


Figure 3

Crystal Operation

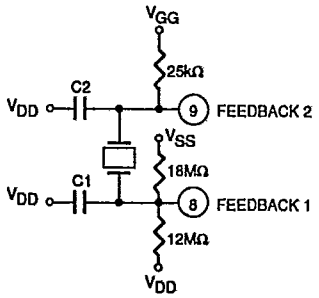


Figure 4

Functional Description

TIME OUT, Pin 1

TIME OUT is the output of the divider chain. It is a square wave whose period depends upon the division mode. For this reason, external circuitry should be triggered on the falling edge of this signal.

V_{DD}, Pin 2

V_{DD} is normally ground for the chip and the other supply voltages are measured with respect to V_{DD}.

EXT IN, Pin 3

When using an external frequency source to operate the MIC5009, the signal should be applied at EXT IN and EXT/INT should be brought to a logic 1 level. The counters are incremented on the falling edge of EXT IN and the signal applied to this pin must be TTL-compatible. When unused, this pin can be tied either high or low.

RESET 0, Pin 4

A positive going pulse of 10µS or longer applied to RESET 0 will reset the counters to their lowest state. Taking RESET 0 to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes according to Table 1.

EXT/INT, Pin 5

A logic 1 level on EXT/INT will gate the signal present at EXT IN through to the counters. A logic 0 level applied to EXT/INT will gate the internal oscillator (RC/crystal) through to the counters.

RESET MAX, Pin 6

A positive going pulse of 10µS or longer on RESET MAX will reset counters to their highest state. RESET MAX enables the user to set up the counters to provide a falling TIME OUT edge at the next oscillator cycle or negative going EXT IN, regardless of which divider chain is selected.

Taking RESET MAX to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes given in Table 1.

$\overline{\text{CLAMP}}$, Pin 7

$\overline{\text{CLAMP}}$ is used in conjunction with the RC mode of operation. Its purpose is to provide accurate start-up operations.

When $\overline{\text{CLAMP}}$ is taken to a logic 0 level, the internal circuitry is held at a fixed reference voltage. Then, when $\overline{\text{CLAMP}}$ is taken to a logic 1 level, the oscillator's first cycle will be a full cycle.

FEEDBACK 1 and FEEDBACK 2, Pins 8 and 9

FEEDBACK 1 and FEEDBACK 2 are oscillator ports. Operation in the RC mode is achieved as shown in Figure 3. Frequency is approximately 0.8/RC. R must be greater than or equal to 10kΩ and C must be greater than or equal to 25 pF for proper operation. Operation in the crystal oscillator mode is shown in Figure 4. The crystal operates in the parallel resonant mode, should operate properly with a 5mW drive, and should have a loading capacitance (C_L) of ≤32 pF. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. The series combination of C1 and C2 should not exceed the value of C_L.

OSC OUT, Pin 10

The oscillator output, provided at Pin 10, is not a true logic output but may be used to drive a high impedance device such as other MOS circuitry. OSC OUT reflects the state of the internal oscillator.

2^3, 2^2, 2^1, and 2^0, Pins 11 through 14

The division selector inputs are used to select the ratio of the TIME OUT frequency to the oscillator input frequency. The effect of specific combinations of logic levels on these pins is shown in Table 1. Note that when all division selector inputs are high, the signal applied to EXT IN appears at the TIME OUT output. Also when RESET 0 and RESET MAX are used in conjunction with the division selector inputs, several more modes can be accessed. (See Table 1.)

V_{SS}, Pin 15

V_{SS} is the positive supply voltage and should be maintained at 5 V_{DC} ± 10% with respect to V_{DD}.

VGG, Pin 16

V_{GG} is the negative supply voltage and should be maintained at −12Vdc with respect to V_{DD}.

Figure 5 shows a very simple test circuit which demonstrates the MIC5009 in the crystal oscillator mode. The division selector switches control the divide mode. The output frequency will be related to the 1MHz oscillator frequency according to Table 1.

Simple Test Configuration

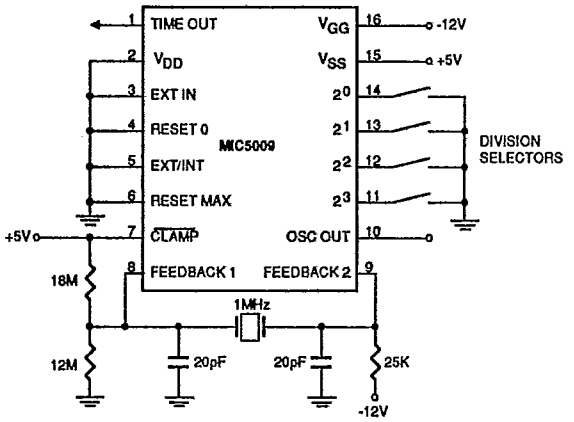
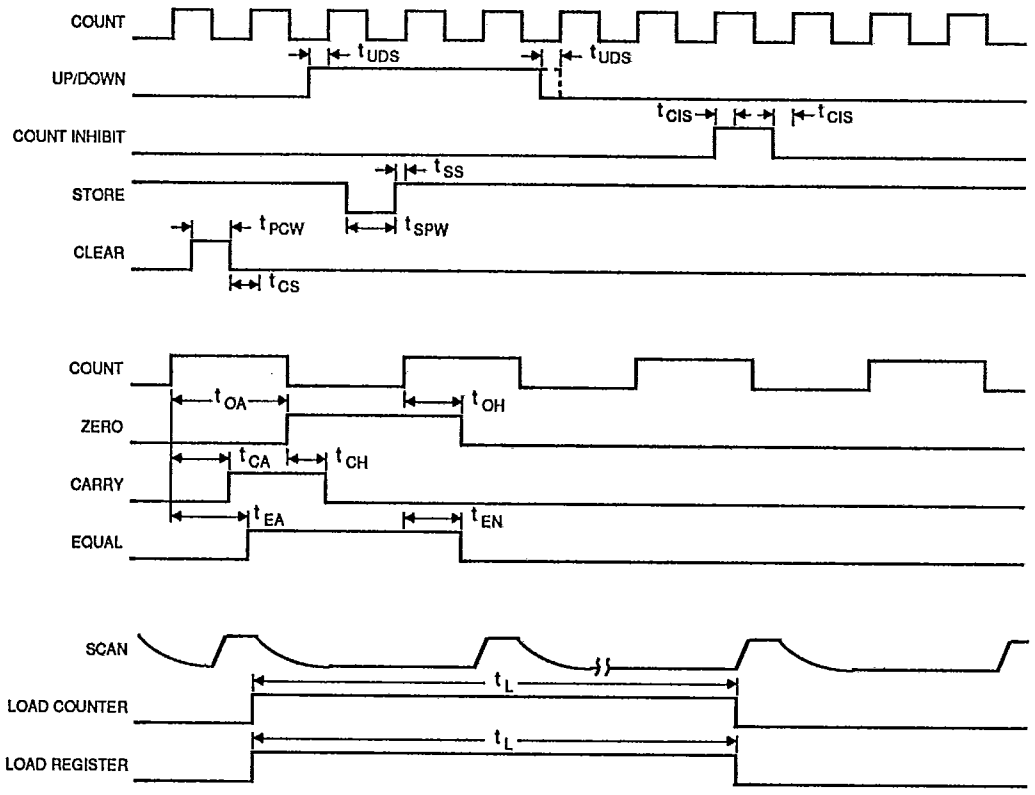


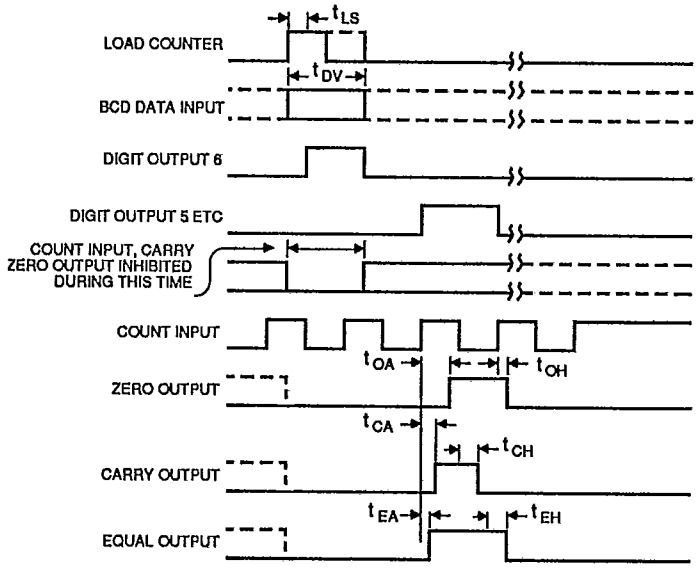
Figure 5

T-51-19

Timing



Loading Counter, Register (1 Digit)



t_{LS} 2.0µSmin — NOTE: REF. TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0µS min — NOTE: REF. TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:
The inhibit function of the zero or equal outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0µS prior to a positive transition of a digit output. This same timing restriction holds for Equal and Load Register.

T-51-19

Absolute Maximum Ratings*

Voltage on Any Terminal Relative to V_{SS}	+0.3V to –20V
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature Range (Ambient)	–65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics - DC

(V_{SS} = +5V ±10%; V_{DD} = 0V; V_{GG} = –12.0V ±20%; 0°C ≤ T_A ≤ 70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{SS}	Supply Voltage	+4.5		+5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	–9.6		–14.4	V	
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
R	Feedback Resistance	0.1		2.5	MΩ	Figure 3
V_{IL}	Input Voltage, Logic 0, Reset Inputs Reset (Bypass Mode) All Other Logic Inputs	0.0 V_{GG}		0.8 V_{GG} + 1.0 0.8	V V V	Note 2
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS} - 1.0	V_{SS}	V_{SS} + 0.3	V	Note 2
I_{IL}	Input Current, Logic 0			–1.6	mA	Note 2; V_I = 0.4V
V_{OL}	Output Voltage, Logic 0			0.4	V	I_{OL} = 1.6mA*
V_{OH}	Output Voltage, Logic 1	2.4			V	I_{OH} = –40µA*

Electrical Characteristics - AC

(V_{SS} = +5V ±10%; V_{DD} = –12.0V ± 20%; 0°C ≤ T_A ≤ 70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.†	Max.	Units	Notes
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	dc		200	kHz	
f_{EXT}	External Frequency	dc		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{CLAMP}$	1/2f_{OSC}				Note 5
	EXT IN	200			nS	
t_{PH}	Logic 1 Pulse Width, EXT IN	200			nS	
	RESET MAX	10.0			µS	
	RESET 0	10.0			µS	
fs_{TA}	Frequency Stability w/Volt. Change, RC Mode w /Temp. Change, RC Mode Crystal Mode		 ±3.0 –0.2		 %/V %/°C	 Note 3 Note 4
t_{EE}	Jitter, Edge-to-Edge Variation			15	nS	Temp. & Supply Voltage Constant

NOTES:
† Typical values at V_{SS} = +5V, V_{DD} = 0V, V_{GG} = –12V, and T_A = 25°C.
1. Logic inputs at V_{SS}, output open-circuited. Each logic input (see Note 2) contributes an additional 1.6mA (max) to I_{SS} when at logic 0 level.
2. Logic inputs are RESET MAX, RESET 0. Address inputs: EXT IN, EXT/INT, and $\overline{CLAMP}$.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at $\overline{CLAMP}$ input is 50% of oscillator period (f_{OSC} = oscillator frequency)
* V_{OH}, V_{OL} apply only to TIME OUT.