

T-46-23-12  
**MS6264A**

# MOSEL

SEPTEMBER 1988

## 8K x 8 HIGH SPEED CMOS STATIC RAM PRELIMINARY

### FEATURES

- High speed — 45/50/70 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  - 550 mW (Max.) Operating
  - 85 mW (Max.) Standby
  - 550  $\mu$ W (Max.) Power-down
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enables ( $\bar{E}_1$  and  $E_2$ ) for simple memory expansion
- Data retention as low as 2V

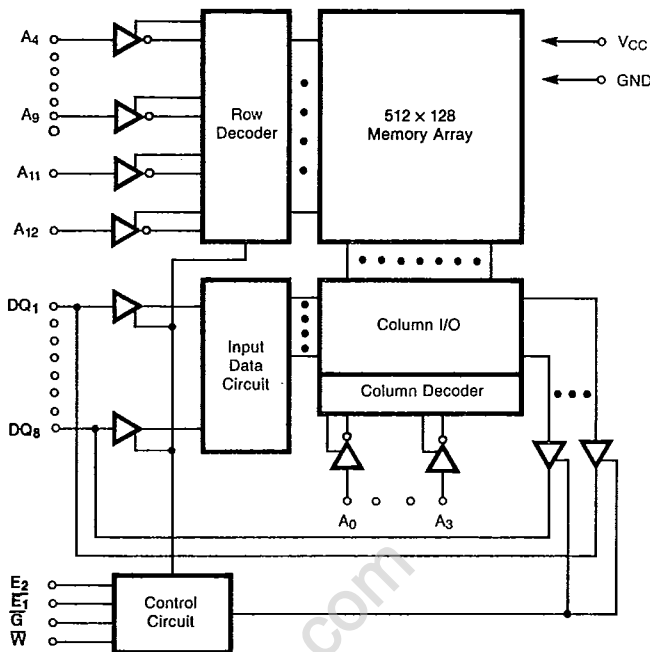
### DESCRIPTION

The Mosel MS6264A is a high performance, low power CMOS static RAM organized as 8192 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ( $\bar{E}_1$ ) and an active High chip enable ( $E_2$ ), as well as an active LOW output enable ( $\bar{G}$ ) and three-state outputs. An automatic power-down feature is included which reduces the chip power by 85% in TTL standby mode, and by over 99% in full power-down mode.

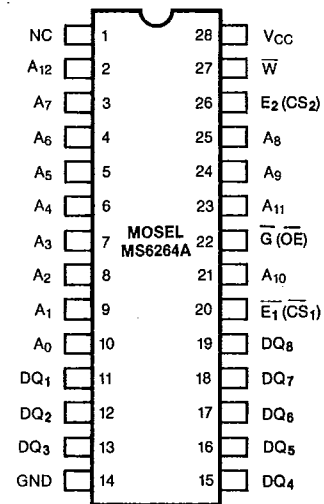
The device is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as  $V_{CC} = 2V$ .

The MOSEL MS6264A is available in the JEDEC standard 28 pin 600 mil wide DIP, in the space saving 300 mil wide DIP, and in surface mount packages.

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATIONS



**MOSEL** 914 W. Maude Avenue, Sunnyvale, CA 94086 (408) 733-4556

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## MS6264A

## PIN DESCRIPTIONS

**A<sub>0</sub> - A<sub>12</sub> Address Inputs**

These 13 address inputs select one of the 8192 8-bit words in the RAM.

 **$\bar{E}_1$  Chip Enable 1 Input****E<sub>2</sub> Chip Enable 2 Input**

$\bar{E}_1$  is active LOW and E<sub>2</sub> is active high. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

 **$\bar{G}$  Output Enable Input**

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high-impedance state when  $\bar{G}$  is inactive.

 **$\bar{W}$  Write Enable Input**

The write enable input is active LOW and controls read and write operations. With the chip selected, when  $\bar{W}$  is HIGH and  $\bar{G}$  is LOW, output data will be present at the DQ pins; when  $\bar{W}$  is LOW, the data present on the DQ pins will be written into the selected memory location.

**DQ<sub>1</sub> - DQ<sub>8</sub> Data Input/Output Ports**

These 8 bidirectional ports are used to read data from or write data into the RAM.

**V<sub>CC</sub> Power Supply****GND Ground**

## TRUTH TABLE

MODE	$\bar{W}$	$\bar{E}_1$	E <sub>2</sub>	$\bar{G}$	I/O OPERATION	V <sub>CC</sub> CURRENT
Not Selected (Power Down)	X	H	X	X	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
	X	X	L	X	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	H	L	H	H	High Z	I <sub>CC</sub>
Read	H	L	H	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	H	X	D <sub>IN</sub>	I <sub>CC</sub>

## MS6264A

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

SYMBOL	PARAMETER	VALUE	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +125	°C
T <sub>STG</sub>	Storage Temperature	-60 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

## DC ELECTRIC CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6264AL			UNITS
			MIN.	TYP. <sup>(1)</sup>	MAX.	
V <sub>IL</sub>	Guaranteed Input Low Voltage <sup>(2)</sup>		-0.5	—	0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage <sup>(2)</sup>		2.0	—	6.0	V
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	—	2	μA
I <sub>OL</sub>	Output Leakage Current	V <sub>CC</sub> = Max, $\bar{E}_1 = V_{IH}$ or E <sub>2</sub> = V <sub>IL</sub> or $\bar{G} = V_{IH}$ , V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	—	2	μA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8mA	—	—	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4mA	2.4	—	—	V
I <sub>CC</sub>	Operating Power Supply Current	V <sub>CC</sub> = Max, $\bar{E}_1 = V_{IL}$ , E <sub>2</sub> = V <sub>IH</sub> , I <sub>I/O</sub> = 0mA, F = F <sub>max</sub> <sup>(3)</sup>	—	—	100	mA
I <sub>CCSB</sub>	Standby Power Supply Current	V <sub>CC</sub> = Max, $\bar{E}_1 = V_{IH}$ or E <sub>2</sub> = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	—	—	15	mA
I <sub>CCSB1</sub>	Power Down Power Supply Current	V <sub>CC</sub> = Max, $\bar{E}_1 > V_{CC} - 0.2V$ , E <sub>2</sub> < 0.2V V <sub>IN</sub> > V <sub>CC</sub> - 0.2V or V <sub>IN</sub> < 0.2V	—	—	100	μA

1. Typical characteristics are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C.  
 2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.  
 3. F<sub>MAX</sub> = 1/T<sub>RC</sub>

CAPACITANCE<sup>(1)</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>DQ</sub>	Input/Output Capacitance	V <sub>DQ</sub> = 0V	8	pF

1. This parameter is guaranteed and not tested.

# MS6264A

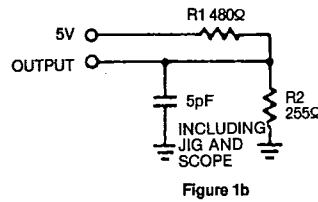
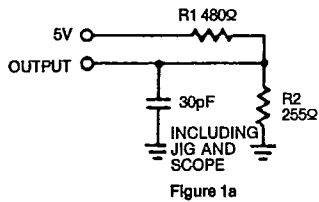
## AC TEST CONDITIONS

## KEY TO SWITCHING WAVEFORMS

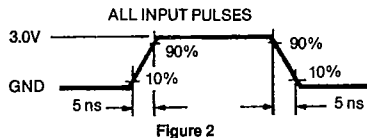
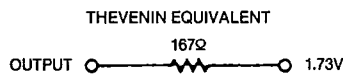
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output	1.5V
Timing Reference Level	

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

## AC TEST LOADS AND WAVEFORMS



Equivalent to:



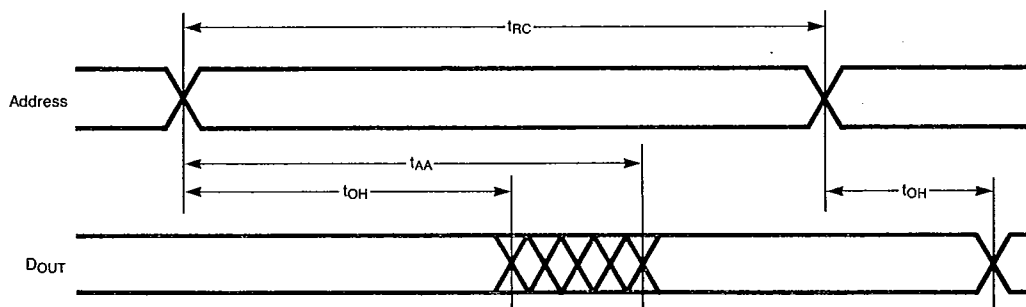
## AC ELECTRICAL CHARACTERISTICS (over the operating range)

### READ CYCLE

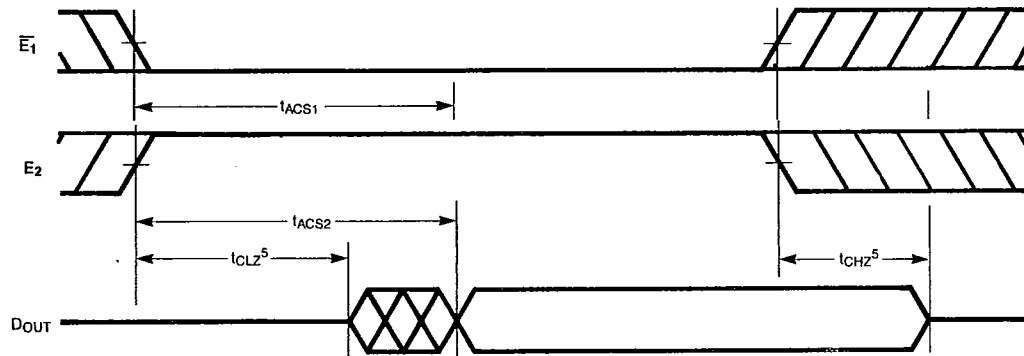
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6264AL-45			MS6264AL-55			MS6264AL-70			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{RC}$	Read Cycle Time	45	—	—	55	—	—	70	—	—	ns
$t_{AVQV}$	$t_{AA}$	Address Access Time	—	—	45	—	—	55	—	—	70	ns
$t_{E1LQV}$	$t_{ACS1}$	Chip Enable Access Time $E_1$	—	—	45	—	—	55	—	—	70	ns
$t_{E2HQX}$	$t_{ACS2}$	Chip Enable Access Time $E_2$	—	—	45	—	—	55	—	—	70	ns
$t_{GLQV}$	$t_{OE}$	Output Enable to Output Valid	—	—	20	—	—	25	—	—	35	ns
$t_{E1LQX}$	$t_{CLZ1}$	Chip Enable to Output Low Z $E_1$	5	—	—	5	—	—	5	—	—	ns
$t_{E2HQX}$	$t_{CLZ2}$	Chip Enable to Output Low Z $E_2$	5	—	—	5	—	—	5	—	—	ns
$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output in Low Z	5	—	—	5	—	—	5	—	—	ns
$t_{E1HQZ}$	$t_{CHZ1}$	Chip Disable to Output in High Z $E_1$	0	—	20	0	—	20	0	—	30	ns
$t_{E2LQZ}$	$t_{CHZ2}$	Chip Disable to Output in High Z $E_2$	0	—	20	0	—	20	0	—	30	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	—	20	0	—	20	0	—	30	ns
$t_{AXQX}$	$t_{OH}$	Output Hold from Address Change	5	—	—	5	—	—	5	—	—	ns

## SWITCHING WAVEFORMS (READ CYCLE)

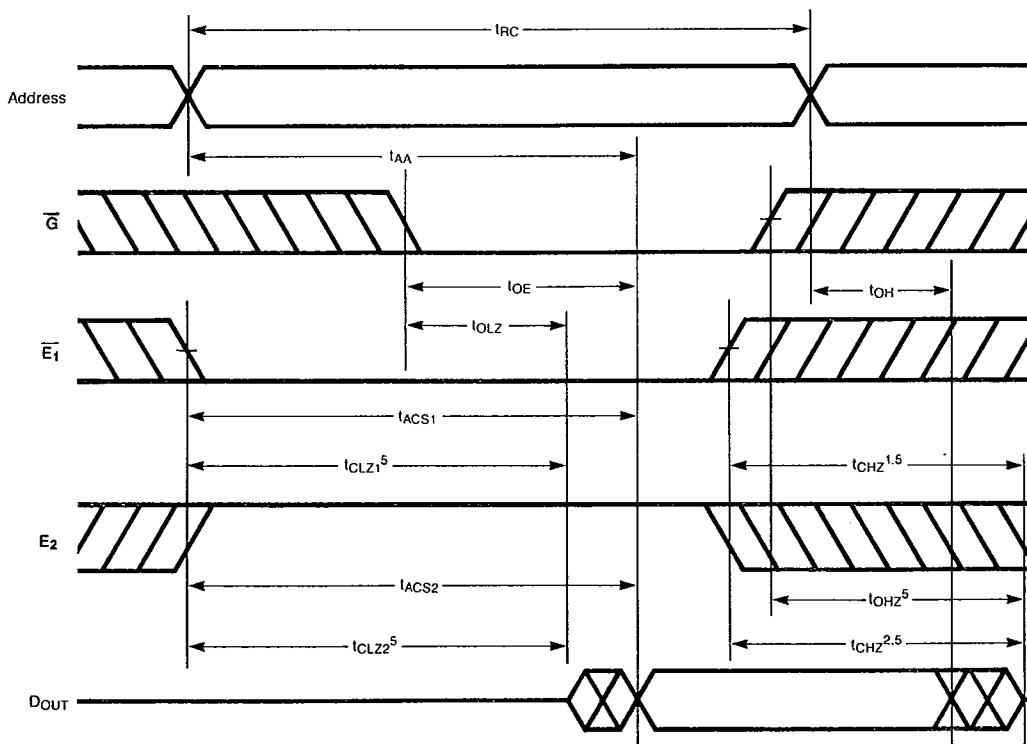
### READ CYCLE NO. 1 (1,2,4)



## READ CYCLE 2 (1,3,4)



## READ CYCLE 3 (1,4)



- NOTES:
- $\bar{W}$  is high for READ cycle.
  - Device is continuously selected  $\bar{E}_1 = V_{IL}$  and  $E_2 = V_{IH}$ .
  - Address valid prior to or coincident with  $\bar{E}_1$  transition low and/or  $E_2$  transition high.
  - $\bar{G} = V_{IL}$ .
  - Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$  as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

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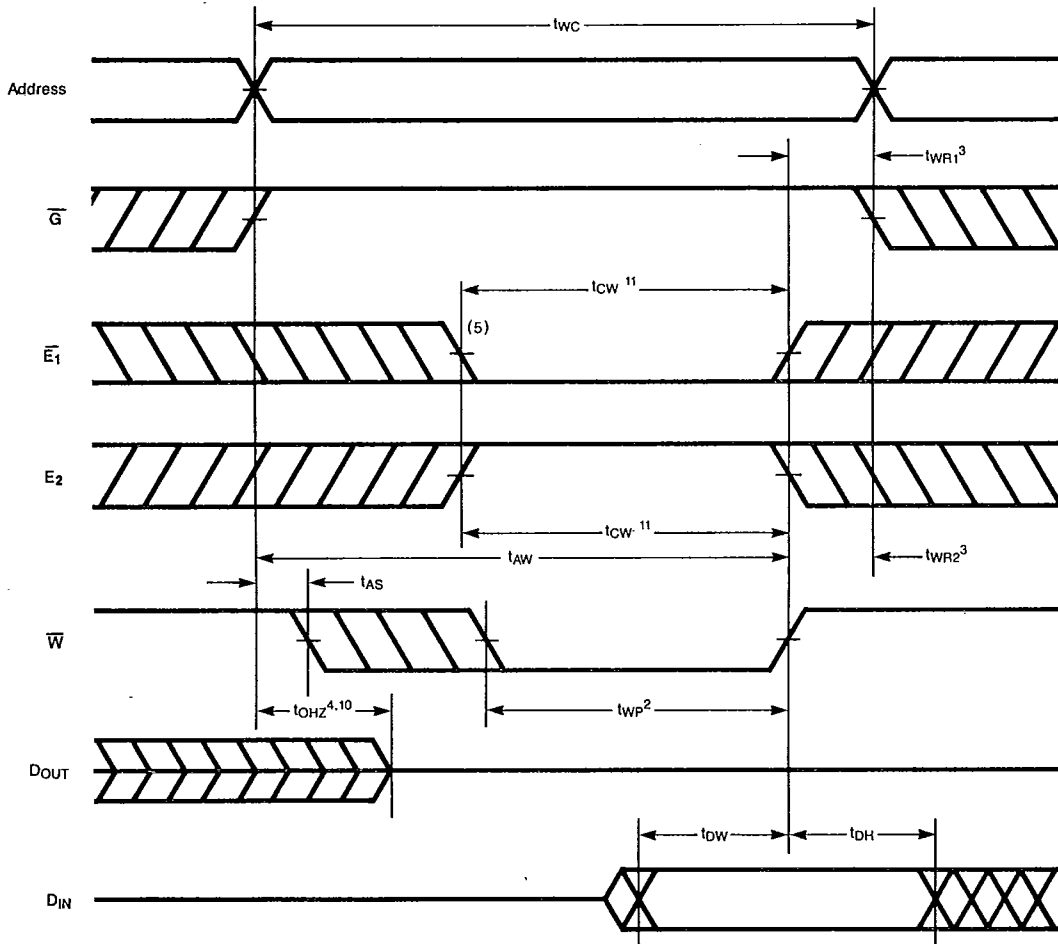
AC ELECTRICAL CHARACTERISTICS (over the operating range)

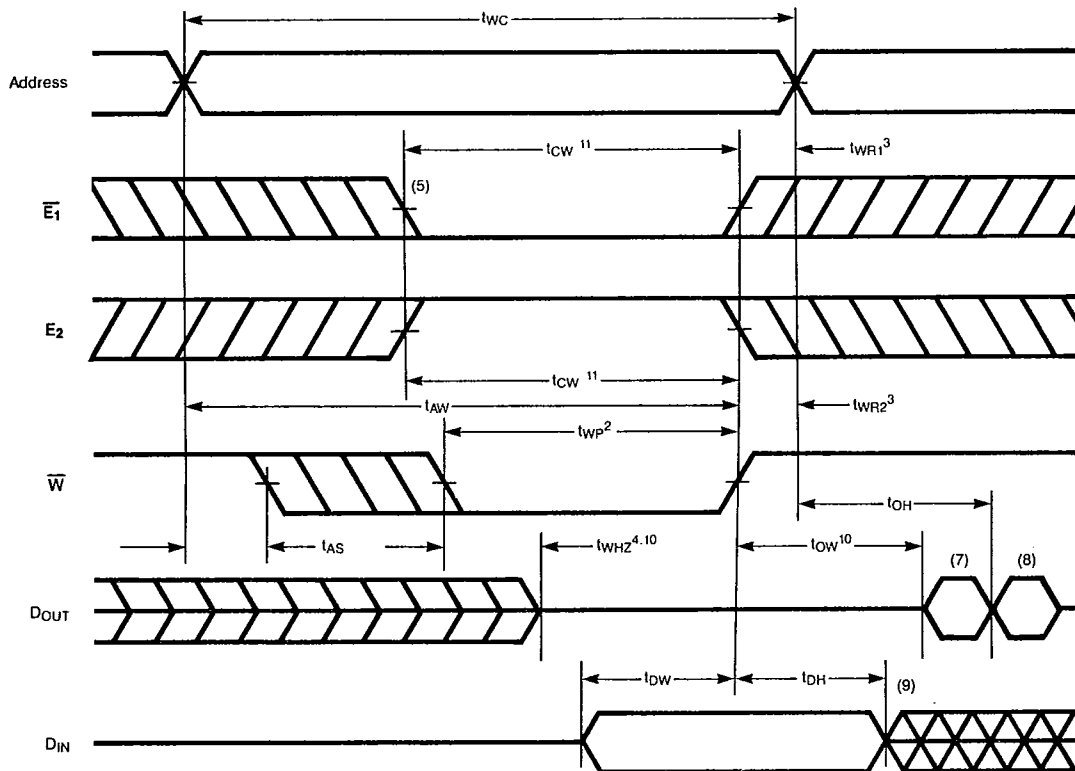
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6264AL-45			MS6264AL-55			MS6264AL-70			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	45	—	—	55	—	—	70	—	—	ns
$t_{E1LWH}$	$t_{CW}$	Chip Enable to End of Write	35	—	—	40	—	—	45	—	—	ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	0	—	—	0	—	—	0	—	—	ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	35	—	—	50	—	—	65	—	—	ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	30	—	—	35	—	—	45	—	—	ns
$t_{WHAX}$	$t_{WR1}$	Write Recovery Time $E_1, W$	0	—	—	3	—	—	5	—	—	ns
$t_{E2LAX}$	$t_{WR2}$	Write Recovery Time $E_2$	0	—	—	3	—	—	5	—	—	ns
$t_{WLOZ}$	$t_{WHZ}$	Write to Output In High Z	0	20	—	0	20	—	0	30	—	ns
$t_{DWWH}$	$t_{DW}$	Data to Write Time Overlap	20	—	—	25	—	—	30	—	—	ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0	—	—	0	—	—	0	—	—	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	20	—	0	25	—	0	30	—	ns
$t_{WHQX}$	$t_{OW}$	Output Active from End of Write	5	—	—	5	—	—	5	—	—	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1<sup>(1)</sup>



WRITE CYCLE 2<sup>(1,6)</sup>

- NOTES:
- $\bar{W}$  must be high during address transitions.
  - The internal write time of the memory is defined by the overlap of  $\bar{E}_1$  and  $E_2$  active and  $\bar{W}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
  - $t_{WR}$  is measured from the earlier of  $\bar{E}_1$  or  $\bar{W}$  going high or  $E_2$  going low at the end of write cycle.
  - During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  - If the  $\bar{E}_1$  low transition or the  $E_2$  high transition occurs simultaneously with the  $\bar{W}$  low transitions or after the  $\bar{W}$  transition, outputs remain in a high impedance state.
  - $\bar{G}$  is continuously low ( $\bar{G} = V_{IL}$ ).
  - $D_{OUT}$  is the same phase of write data of this write cycle.
  - $D_{OUT}$  is the read data of next address.
  - If  $\bar{E}_1$  is low and  $E_2$  is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
  - Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$  as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
  - $t_{CW}$  is measured from the later of  $\bar{E}_1$  going low or  $E_2$  going high to the end of write.

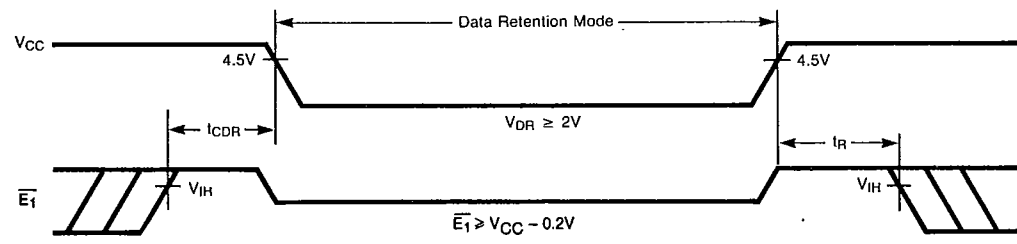
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DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = 0 to +70°C)

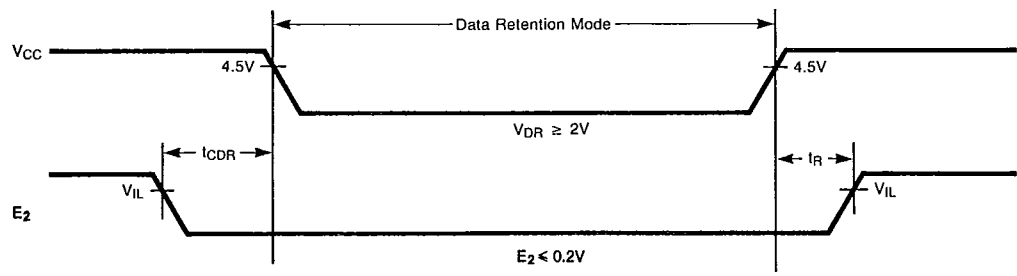
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	$\bar{E}_1 \geq V_{CC} - 0.2V$ , or $E_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
I <sub>CCDR</sub>	Data Retention Current	$\bar{E}_1 \geq V_{CC} - 0.2V$ , or $E_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	2	50	μA
I <sub>IL</sub>	Input Leakage Current		—	—	2	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	—	—	ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	—	—	ns

- 1. V<sub>CC</sub> = 2V, T<sub>A</sub> = +25°C
- 2. t<sub>RC</sub> = Read Cycle Time

LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (1) ( $\bar{E}_1$  Controlled)



LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (2) (E<sub>2</sub> Controlled)







## MS6264A

## ORDERING INFORMATION

SPEED (ns)	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
45	MS6264AL-45NC	Plastic DIP - 300 mil	
45	MS6264AL-45PC	Plastic DIP - 600 mil	0°C to +70°C
45	MS6264AL-45SC	Plastic Small Outline Package	0°C to +70°C
55	MS6264AL-55NC	Plastic DIP - 300 mil	0°C to +70°C
55	MS6264AL-55PC	Plastic DIP - 600 mil	0°C to +70°C
55	MS6264AL-55SC	Plastic Small Outline Package	0°C to +70°C
70	MS6264AL-70NC	Plastic DIP - 300 mil	0°C to +70°C
70	MS6264AL-70PC	Plastic DIP - 600 mil	0°C to +70°C
70	MS6264AL-70SC	Plastic Small Outline Package	0°C to +70°C
45	MS6264AL-45TM	Cer DIP - 300 mil	-55°C to +125°C
45	MS6264AL-45DM	Cer DIP - 600 mil	-55°C to +125°C
45	MS6264AL-45LM	Leadless Chip Carrier	-55°C to +125°C
55	MS6264AL-55TM	Cer DIP - 300 mil	-55°C to +125°C
55	MS6264AL-55DM	Cer DIP - 600 mil	-55°C to +125°C
55	MS6264AL-55LM	Leadless Chip Carrier	-55°C to +125°C
70	MS6264AL-70TM	Cer DIP - 300 mil	-55°C to +125°C
70	MS6264AL-70DM	Cer DIP - 600 mil	-55°C to +125°C
70	MS6264AL-70LM	Leadless Chip Carrier	-55°C to +125°C