MSM6369

T-52-13-07

DOT MATRIX 80 DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM6369GS is a dot matrix LCD's segment driver LSI, which is fabricated by CMOS low power silicon gate technology.

This LSI consists of an 80-bit shift register, 80-bit latch, 80-bit level shifter and an 80-bit 4 level driver.

It receives the display driving data, which consists of 8-bit parallel, from a microcontroller or a MSM6355GS LCD controller LSI, then outputs the LCD driving waveform to the LCD.

The MSM6369GS has a power save function which reduces the MSM6369GS's power consumption.

The MSM6369GS can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be supplied from an external source as an option.

FEATURES

- Supply voltage : 4.5~5.5V
- LCD driving voltage : 20~40V
- Applicable LCD duty : 1/200~1/480
- LCD output : 80
- Bias voltage can be supplied externally.
- Power save function.
- Transmission speed is one eighth in comparison with serail transmission due to 8-bit parallel.
- Can be interfaced with the MSM6355, LCD controller LSI.
- 100 pin Plastic QFP (QFP100-P-1420-K)
- 100 pin Plastic QFP (QFP100-P-1420-L)

PIN CONFIGURATION

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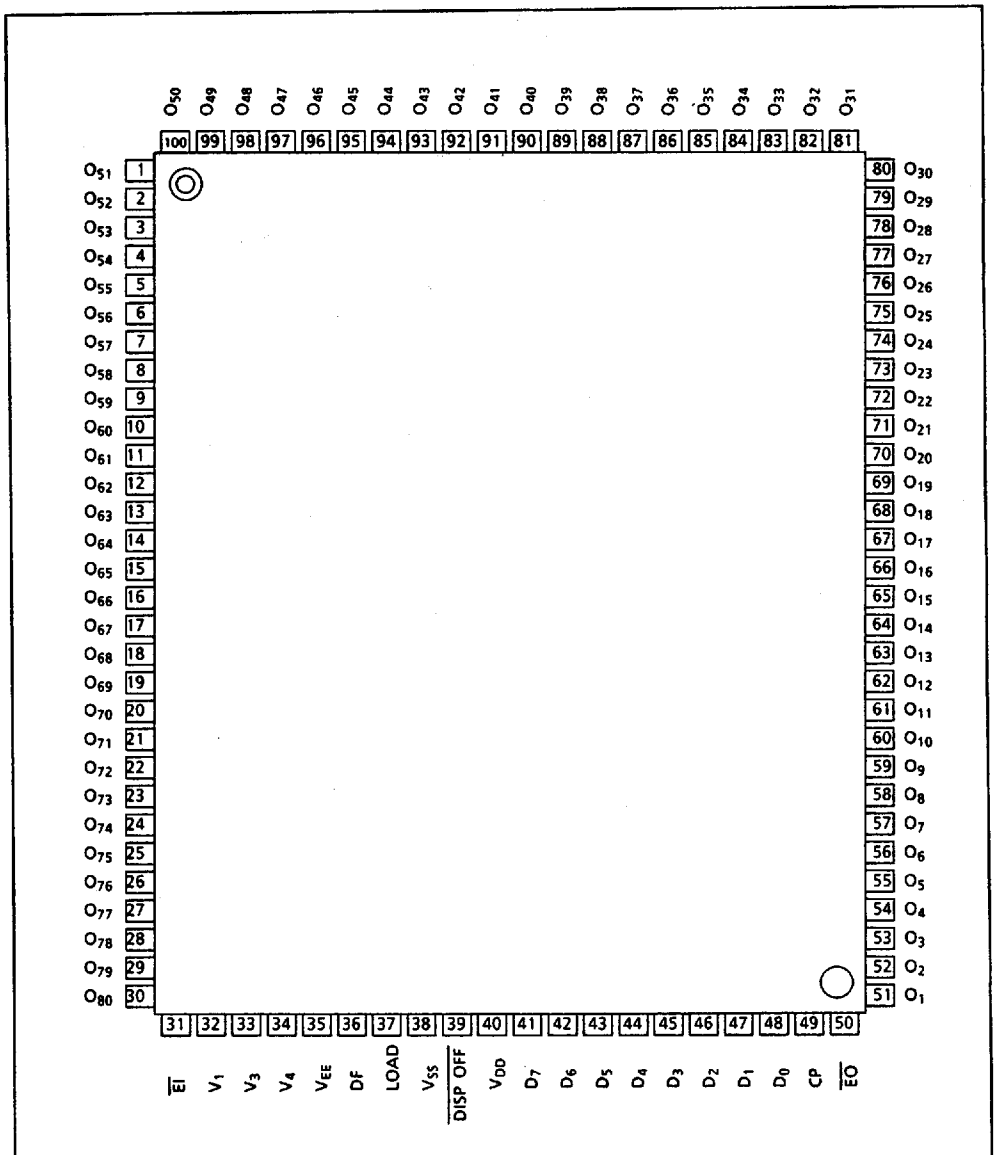

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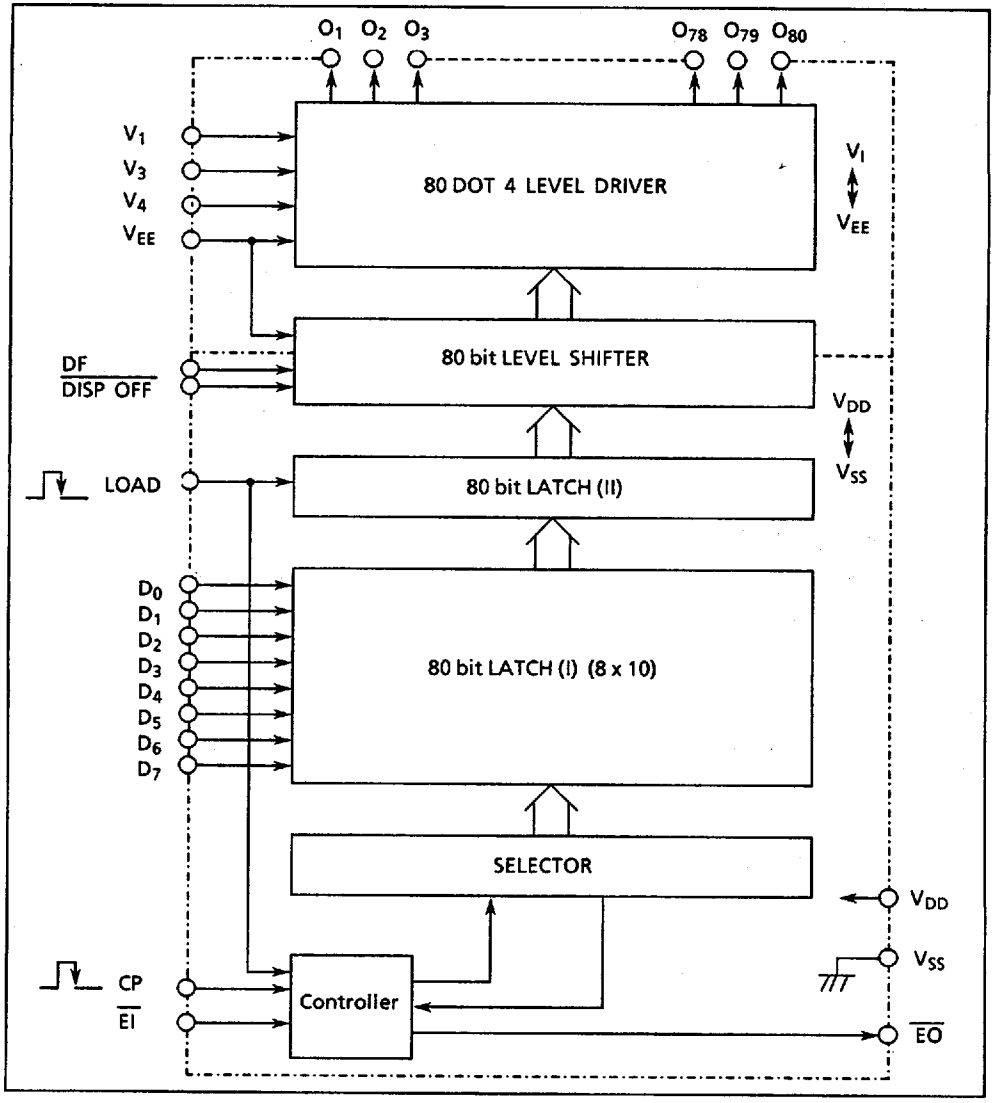
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

DF	LATCH DATA	$\overline{\text{DISP OFF}}$	DRIVER OUT (O_1~O_{80})
L	L	H	V_3
L	H	H	V_1
H	L	H	V_4
H	H	H	V_{EE}
X	X	L	V_1

ABSOLUTE MAXIMUM RATINGS

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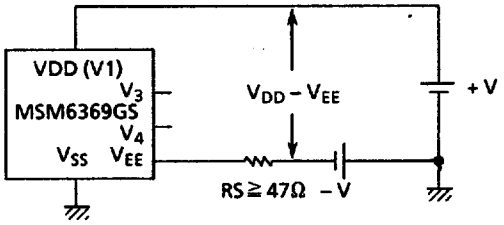
Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage (1)	V_{DD}	Ta = 25°C	− 0.3~	V
Supply Voltage (2)	$V_{DD} - V_{EE}$ *1	Ta = 25°C	0~40	V
	$V_{DD} - V_{EE}$ *1 *2	Ta = 25°C	0~42	
Input Voltage	V_I	Ta = 25°C	− 0.3~V_{DD} + 0.3	V
Storage Temperature	Tstg	−	− 55~ + 150	°C

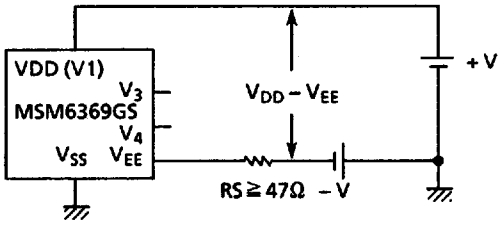
*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$
*2 In case of connecting Resister ($RS \geqq 47\Omega$) at V_{EE} PIN



OPERATING RANGE

Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage (1)	V_{DD}	−	4.5~5.5	V
Supply Voltage (2)	$V_{DD} - V_{EE}$ *1	−	20~38	V
	$V_{DD} - V_{EE}$ *2	−	20~40	
Operating Temperature	Top	−	− 20~ + 75	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$
*2 In case of connecting Resister ($RS \geqq 47\Omega$) at V_{EE} PIN



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DC CHARACTERISTICS

(V_{DD} = 5V ± 10% Ta = −20~+75°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input Voltage	V_{IH} *1	−	0.8V_{DD}	−	−	V
"L" Input Voltage	V_{IL} *1	−	−	−	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	$V_{IH} = V_{DD}$ V_{DD} = 5.5V	−	−	1	µA
"L" Input Current	I_{IL} *1	V_{IL} = 0V V_{DD} = 5.5V	−	−	−1	µA
"H" Output Voltage	V_{OH} *2	I_O = −0.2 mA V_{DD} = 4.5V	V_{DD} − 0.4	−	−	V
"L" Output Voltage	V_{OL} *2	I_O = 0.2 mA V_{DD} = 4.5V	−	−	0.4	V
ON Resistance	R_{ON} *4	$V_{DD} - V_{EE}$ = 35V V_{DD} = 4.5V $\lvert V_N - V_O \rvert$ = 0.25V *3	−	−	1.5	kΩ
Stand-by current consumption	I_{DD} SBY	CP = 4.5MHz V_{DD} = 5.5V $V_{DD} - V_{EE}$ = 35V No Load *5	−	−	2.0 / 0.5	mA
(1) Current Consumption	I_{DD1}	CP = 4.5MHz V_{DD} = 5.5V $V_{DD} - V_{EE}$ = 35V No Load *6	−	−	3 / −1	mA
(2) Curent Consumption	I_V	CP = 4.5MHz V_{DD} = 5.5V $V_{DD} - V_{EE}$ = 35V No Load *7	−	−	100	µA
Input Capacitance	C_I	f = 1MHz	−	5	−	pF

*1 Applicable to LOAD, CP, D_0~D_7, $\overline{EI}$, DF, $\overline{DISP\ OFF}$ terminals.

*2 Applicable to $\overline{EO}$ terminal.

*3 $VN = V_{DD}$~V_{EE}, $V_3 = \frac{19}{21}(V_{DD} - V_{EE})$, $V_2 = \frac{2}{21}(V_{DD} - V_{EE})$, $V_{DD} = V_1$.

*4 Applicable to O_1~O_{80} terminals.

*5 Display data 1010 ..... DF = 40Hz, Current from V_{DD} to V_{SS} when the display data is not processing. (1st Stage / 2nd Stage)

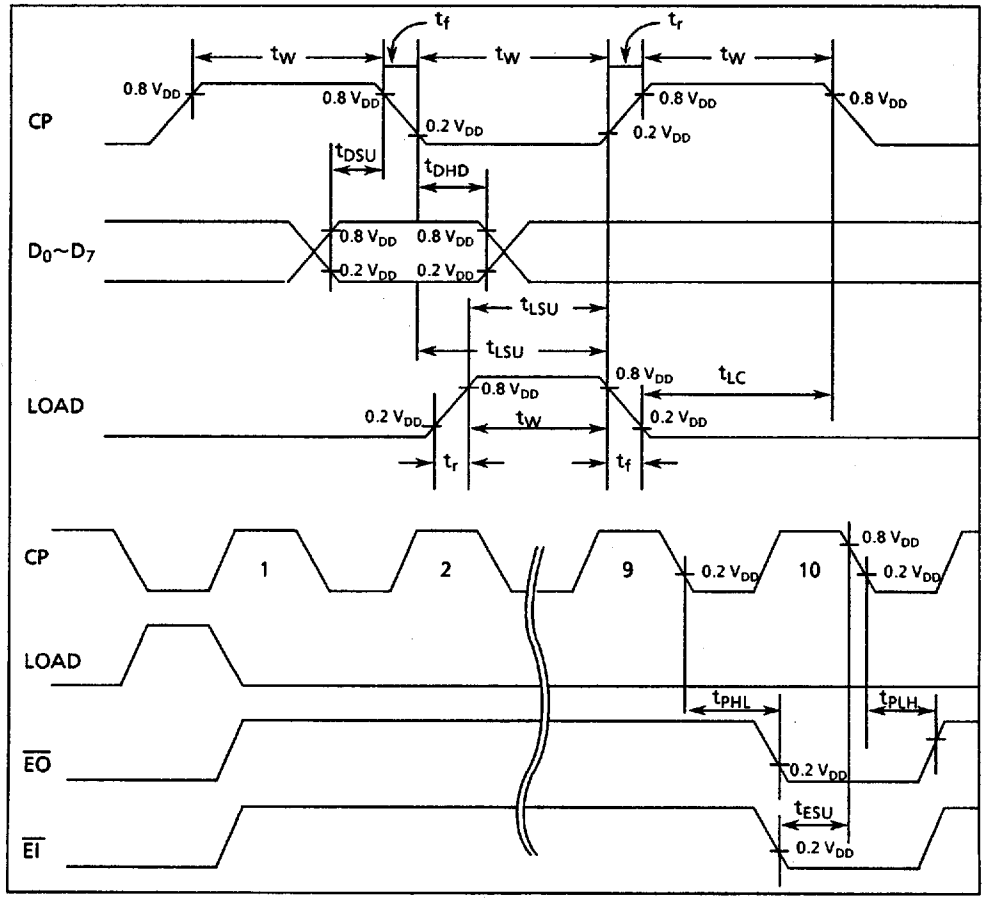
*6 Display data 1010 ..... DF = 40Hz, Current from V_{DD} to V_{EE} and V_{DD} to V_{SS} when the display is processing. (V_{DD} / V_{EE})

*7 Display data 1010 ..... DF = 40Hz, Current on V_1, V_3, V_4 and V_{EE} terminals.

AC CHARACTERISTICS

(V_{DD} = 5V ± 10% Ta = −20~+75°C CL = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum clock frequency	f_{CP}	DUTY = 50%	6	–	–	MHz
Clock load pulse width	t_W	–	63	–	–	ns
Rising/Falling time	t_r, t_f	–	–	–	20	ns
Data set-up time	t_{DSU}	–	50	–	–	ns
Data hold time	t_{DHD}	–	50	–	–	ns
Load set-up time	t_{LSU}	–	80	–	–	ns
Load → Clock time	t_{LC}	–	80	–	–	ns
Propagation delay time	t_{PLH}	–	–	–	116	ns
$\overline{EI}$ set-up time	t_{ESU}	–	50	–	–	ns



PIN DESCRIPTION

- **$\overline{EI}$**

  This is a control input pin for the enable F/F of the IC. When the pin goes high, the built-in counter stops. When the pin goes low, the counter is ready for operation.

- **$\overline{EO}$**

  This is an output pin for the enable F/F of the IC. When a cascade connection is required, connect this pin to the $\overline{EI}$ pin on the next stage.
  When the internal counter is reset by a load pulse, the pin goes high simultaneously. When Serial or Parallel is selected by a shift clock pulse, which is input from the CP pin, and 80 bits are converted, this output pin goes low and the internal counter stops. The pin waits for the next load pulse.
  For cascade connection, see the application circuit example.

- **CP**

  This is a 4-bit parallel shift register clock input pin. Data is shifted at the trailing edge of a clock pulse.
  A clock pulse from this pin is valid when the enable F/F is in the set state, while invalid when it is in the non-set state.

- **LOAD**

  This is an input pin to latch the display data stored in the shift register. At the trailing edge of a load pulse, the display data stored in the shift register is latched. At the trailing edge ( ) of a load pulse, the built-in counter of this IC is reset.

- **DF**

  This is an input pin for a liquid crystal drive waveform AC synchronization signal, which generally inputs a frame inversion signal.

- **V_{DD}, V_{SS}**

  These are power pins of this IC. The V_{DD} pin is generally set to 4.5 to 5.5V. V_{SS} is a grounding pin, which is generally set to 0V.

  Note when turning power on and off
  The liquid crystal drive on this IC chip requires a high voltage. When a high voltage is applied to it with the logic power supply floated, an overcurrent flows. This may damage the IC chip. Be sure to carry out the following power-on and power-off sequences:

  When turning power on:
  First V_{DD} ON, next V_{EE}, V_4, V_3, V_1 ON. Or both at the same time.

  When turning power off:
  First V_{EE}, V_4, V_3, V_1 OFF, next V_{DD} OFF. Or both at the same time.

- **V_1, V_3, V_4, V_{EE}**

These are liquid crystal drive bias voltage pins. Bias voltages by resistance division are generally used. Fig. 1 shows an example of supply of liquid crystal drive bias voltages by resistance division. The V_1 pin may be separated from the V_{DD} pin.

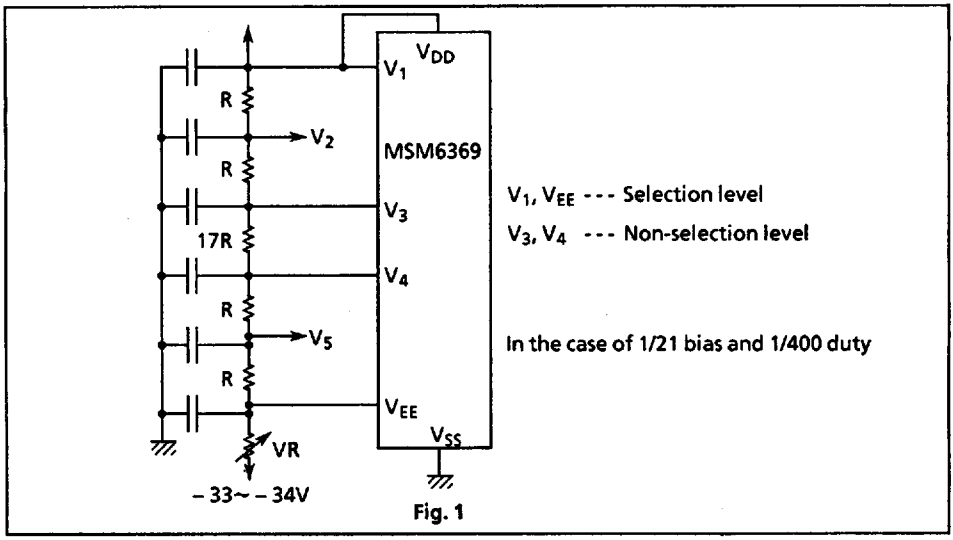


Fig. 1

Fig. 2 shows an example of supply of bias voltages using an operational amplifier. the use of an operational amplifier reduces the bias impedance and the supply current.

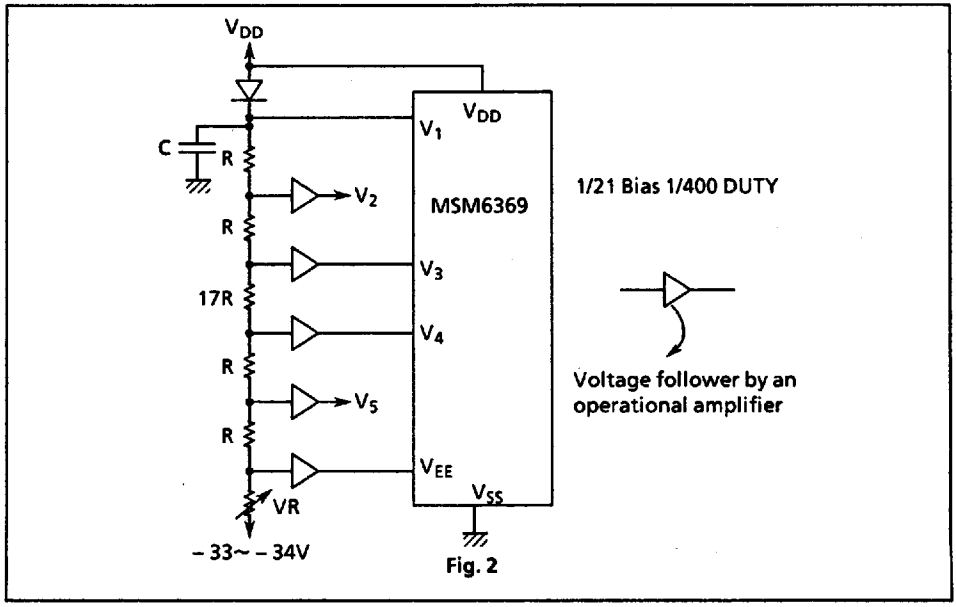


Fig. 2

- **D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7**

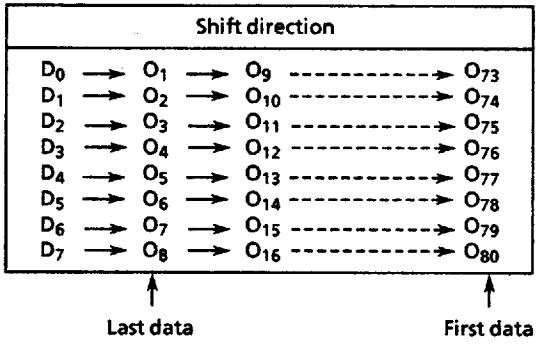
These are 8-bit parallel shift register data input pins. Display data is input in synchronization with a clock pulse. Table 1 gives the relation between D_0 to D_7 or DF an liquid crystal drive output or liquid crystal display.

Table 1

D_0~D_7	DF	Liquid crystal drive output		Liquid crystal display
L	L	Non-selection level	(V_3)	OFF
H	L	Selection level	(V_1)	ON
L	H	Non-selection level	(V_4)	OFF
H	H	Selection level	(V_{EE})	ON

Table 2 gives the relation between the display data input pins D_0, D_1, D_2, and D_7 and the liquid crystal drive output pins O_1 to O_{80}.

Table 2



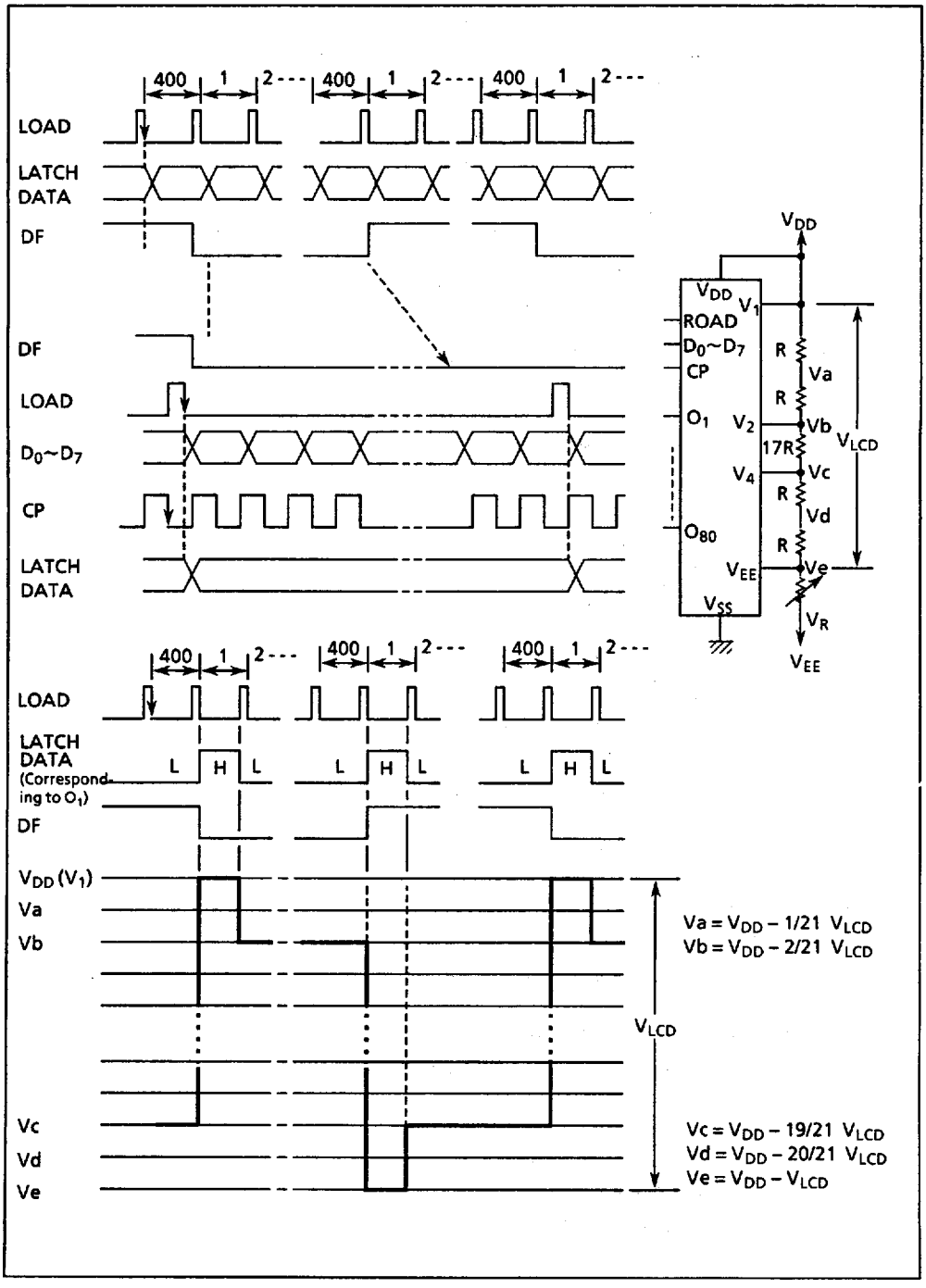
- **O_1 to O_{80}**

These are output pins of the 4-level driver of this IC, which correspond directly to the bits of the shift register. One of the four levels V_1, V_3, V_4, and V_{EE} is selected and output by a combination of the latch contents (display data) and a DF signal. See the truth table. Connect the output pins to the liquid crystal panel on the segment side.

- **$\overline{\text{DISP OFF}}$**

These are input pins to control the output pins O_1 to O_{80}. During low signal input, signals on the V1 level are output from the output pins O_1 to O_{80}. See the truth table.

TIMING CHART (1/400 duty, 1/21 bias)



POWER SAVE FUNCTION

To reduce the power consumption in the case of cascade connection, an enable F/F is installed within the IC (see Fig. 1). When an IC contains this type of enable F/F, display data is transferred. An IC, which does not contain such an enable F/F, enters the non-fetch state and is kept in the low supply current (I_{DD} SBY). The enable F/F setting state is shifted to the next stage sequentially by the pins $\overline{EI}$ and $\overline{EO}$ and the internal counter so that the enable F/F exists in one IC.

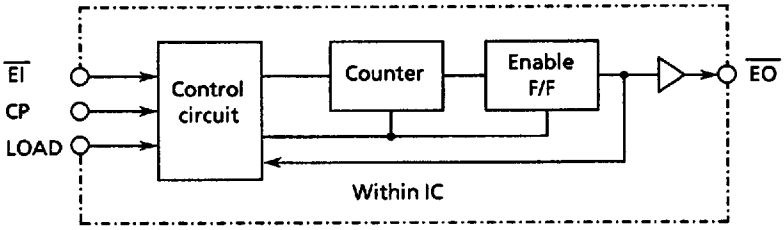
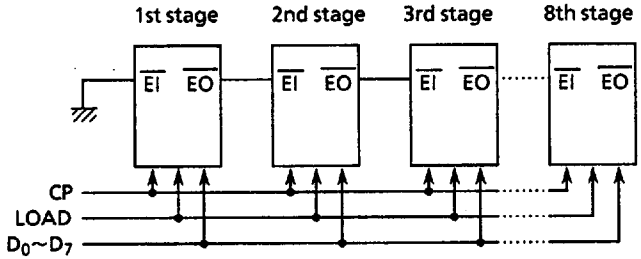
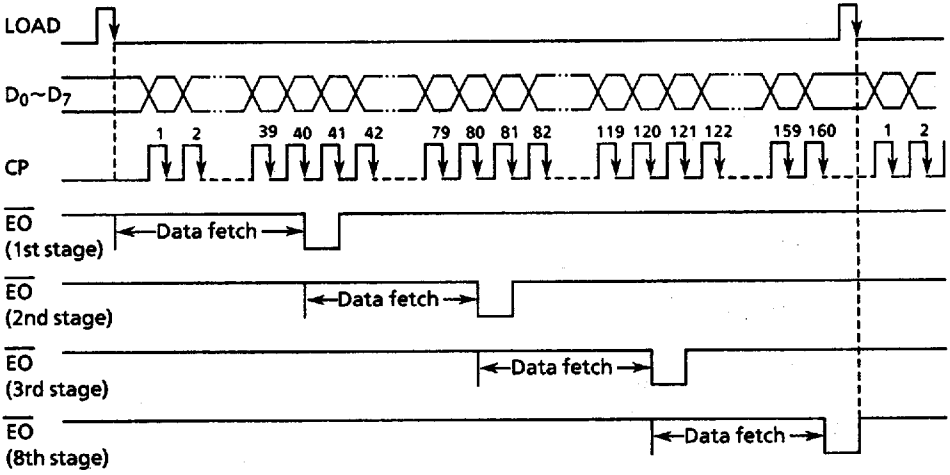


Fig. 1





Time chart in the case of cascade connection

APPLICATION NOTE