

PM50CTJ060-3

INSULATED PACKAGE
FLAT-BASE TYPE

PM50CTJ060-3



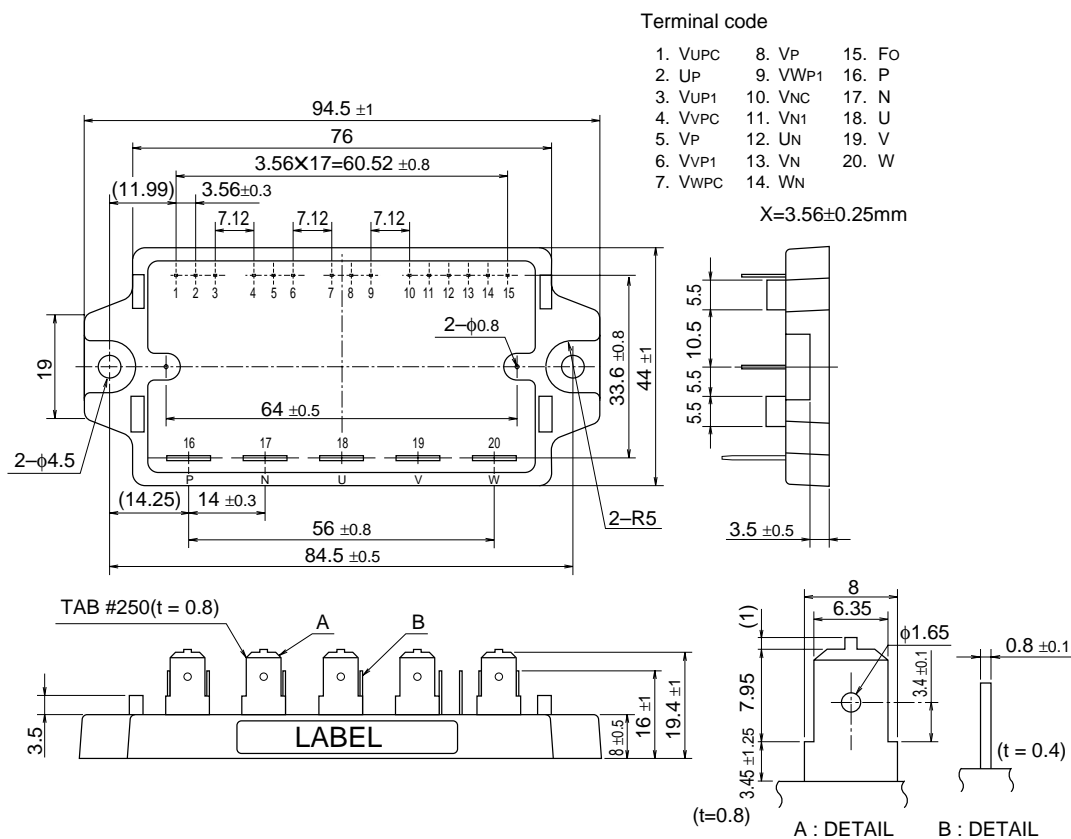
- 4th gen. planer IGBTs are integrated
- 3φ 50A, 600V Current-sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage
- Acoustic noise-less 3.7kW class inverter application

APPLICATION

Air-conditioner, General purpose inverter, servo drives and other motor controls

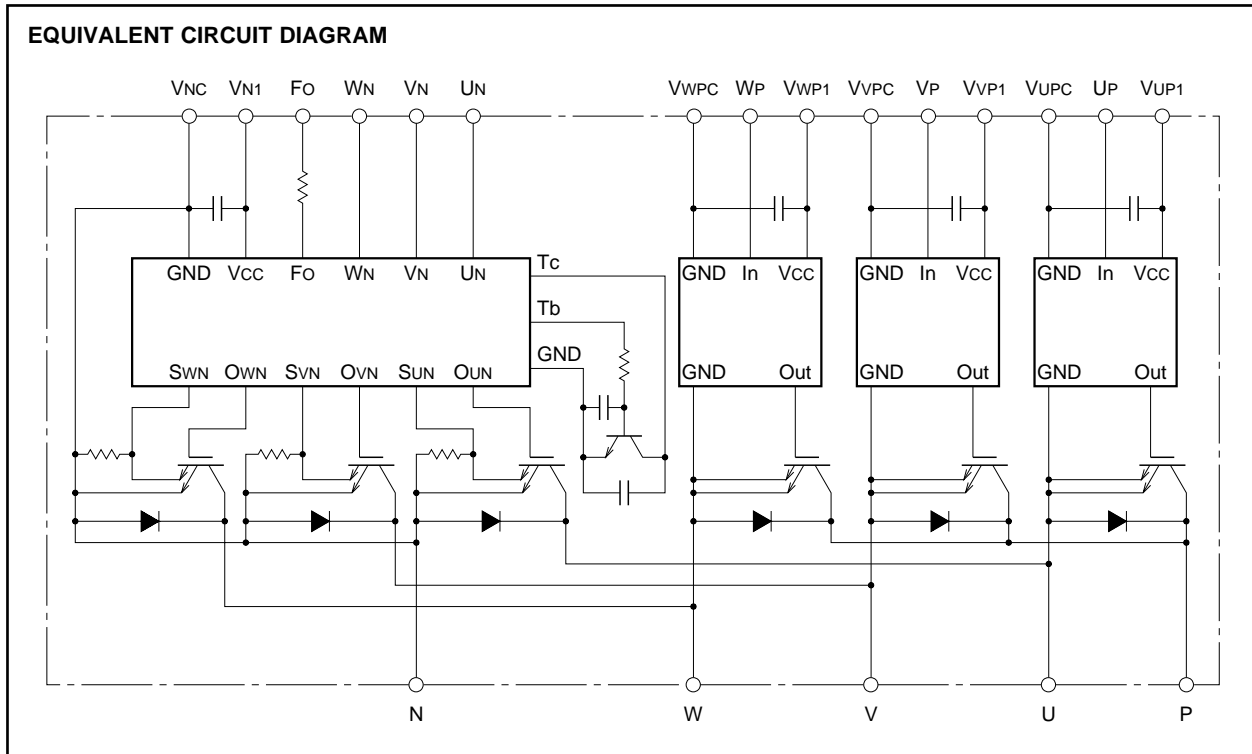
OUTLINE DRAWING

Dimensions in mm



PM50CTJ060-3

INSULATED PACKAGE
FLAT-BASE TYPE



MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	Applied between : P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between : P-N, Surge value	500	V
Vces	Collector-emitter voltage		600	V
$\pm I_C$	Collector current	$T_c = 25^\circ\text{C}$	50	A
$\pm I_{CP}$	Collector current (peak)	$T_c = 25^\circ\text{C}$	100	A
Pc	Collector dissipation	$T_c = 25^\circ\text{C}$	100	W
T_j	Junction temperature		-20 ~ +125*	$^\circ\text{C}$

* The item defines the maximum junction temperature for the power elements (IGBT/Diode) of the IPM to ensure safe operation. However, these power elements can endure junction temperature as high as 150°C instantaneously. To make use of this additional temperature allowance, a detailed study of the exact application conditions is required and, accordingly, necessary information is requested to be provided before use.

CONTROL PART

Symbol	Parameter	Conditions	Ratings	Unit
V _D	Supply voltage	Applied between : VUP1-VUPC, VVP1-VVPC VWP1-VWPC, VN1-VNC	20	V
I _{CIN}	Input current	At : UP, VP, WP, UN, VN, WN terminals	20	mA
V _{FO}	Fault output supply voltage	Applied between : FO-VNC	20	V
I _{FO}	Fault output current	Sink current of FO terminals	20	mA

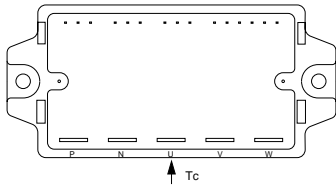
PM50CTJ060-3

INSULATED PACKAGE
FLAT-BASE TYPE

TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC(PROT)}	Supply voltage protected by OC & SC	V _D = 13.5 ~ 16.5V, Inverter part, T _j = 125°C start	400	V
T _C	Module case operating temperature	(Note 1)	-20 ~ +100	°C
T _{stg}	Storage temperature		-40 ~ +125	°C
V _{iso}	Isolation voltage	60Hz, sinusoidal, Charged part to Base, AC · 1 min.	2500	V _{rms}

Note 1 : T_c measurement point.



THERMAL RESISTANCES

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case thermal resistances	Inverter IGBT part (per 1/6 module)	—	—	1.2	°C / W
R _{th(j-c)F}		Inverter FWD part (per 1/6 module)	—	—	2.9	°C / W
R _{th(c-f)}	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.4	°C / W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	V _D = 15V, I _{CIN} = 10mA I _C = 50A, Pulsed (Fig. 1)	T _j = 25°C	—	1.8	2.6	V
			T _j = 125°C	—	2.0	3.0	
V _{EC}	FWD forward voltage	-I _C = 50A, V _D = 15V, I _{CIN} = 0mA (Fig. 2)		—	2.5	3.5	V
t _{on}	Switching time	V _D = 15V, I _{CIN} = 0mA↔10mA V _{CC} = 300V, I _C = 50A T _j = 125°C Inductive Load (Upper-Lower Arm) (Fig. 3)		0.5	1.0	2.0	μs
t _{rr}				—	0.1	—	μs
t _{c(on)}				—	0.3	0.9	μs
t _{off}				—	3.0	4.0	μs
t _{c(off)}				—	1.0	2.0	μs
I _{CES}	Collector-emitter cutoff current	V _{CE} = V _{CE(s)} , V _D = 15V (Fig. 4)		T _j = 25°C	—	1	mA
				T _j = 125°C	—	10	

PM50CTJ060-3

**INSULATED PACKAGE
FLAT-BASE TYPE**

CONTROL PART

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
ID	Circuit current	VD = 15V, ICIN = 0mA	VN1-VNC	—	25	35	mA
			VXP1-VXPC	—	5	10	
Ith(ON)	Input on threshold current	At : UP-VUPC, VP-VVPC, WP-VWPC	1	3	5	mA	
Ith(OFF)	Input off threshold current	UN · VN · WN-VNC terminals	1	3	5	mA	
OC	Over current trip level	-20°C ≤ Tj ≤ 125°C, VD = 15V (Fig. 5, 6) (Lower Arm only)	65	91	—	A	
SC	Short circuit trip level	-20°C ≤ Tj ≤ 125°C, VD = 15V (Fig. 5, 6) (Lower Arm only)	—	130	—	A	
toff(OC)	Over current delay time	VD = 15V (Fig. 5, 6)	—	10	—	µs	
OT	Over temperature protection	Baseplate	Trip level	100	110	120	°C
OTr		Temperature detection, VD = 15V	Reset level	—	90	—	°C
UV	Supply circuit under voltage protection	-20°C ≤ Tj ≤ 125°C (Lower Arm only)	Trip level	11.5	12.0	12.5	V
UVr			Reset level	—	12.5	—	V
Ifo(H)	Fault output current	VD = 15V, VFO = 15V (Note 2)	—	—	0.01	mA	
Ifo(L)			—	10	15	mA	
tFO	Minimum fault output pulse width	VD = 15V (Note 2)	1.0	1.8	—	ms	

Note 2 : Fault output is given only when the internal OC, SC, OT & UV protections schemes of lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M4	0.98	1.18	1.47	N·m
—	Weight		—	80	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VCC	Supply voltage	Applied across P-N terminals	0	300	400	V
VD		Applied between : VUP1-VUPC, VVP1-VVPC VWP1-VWPC, VN1-VNC	13.5	15.0	16.5	V
ICIN(ON)	Input on current	At : UP, VP, WP, UN, VN, WN terminals	5	10	20	mA
ICIN(OFF)	Input off current		0	—	1	mA
fPWM	PWM input frequency	For IPM's each input signals, (Fig. 7)	—	—	8	kHz
tdead	Arm shoot-through blocking time	For IPM's each input signals, (Fig. 7)	3.5	—	—	µs

PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input signals should be turned on from its off state.
After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing "OC" and "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

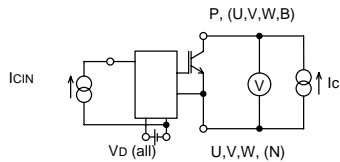


Fig.1 VCE(sat) Test

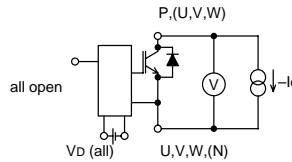


Fig.2 VEC Test

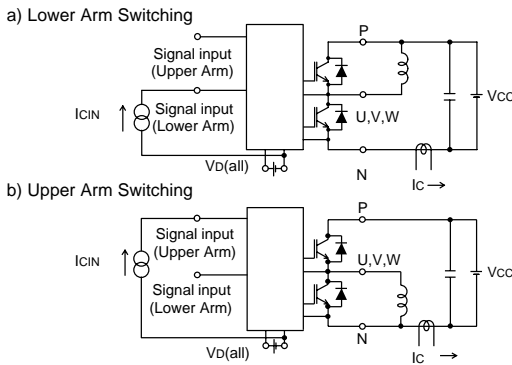


Fig. 3 Switching time Test circuit and waveform

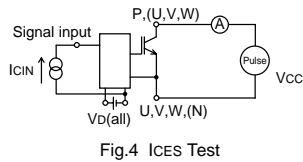


Fig.4 ICES Test

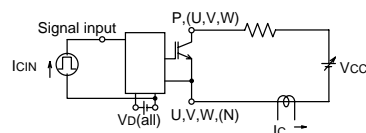


Fig. 5 OC and SC Test

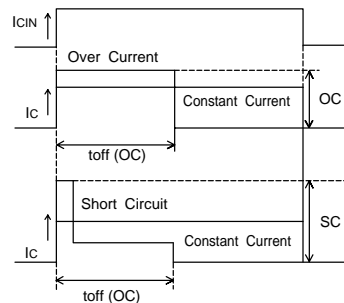


Fig. 6 OC and SC Test waveform

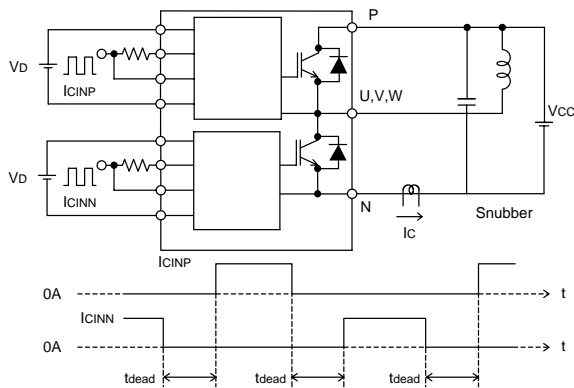
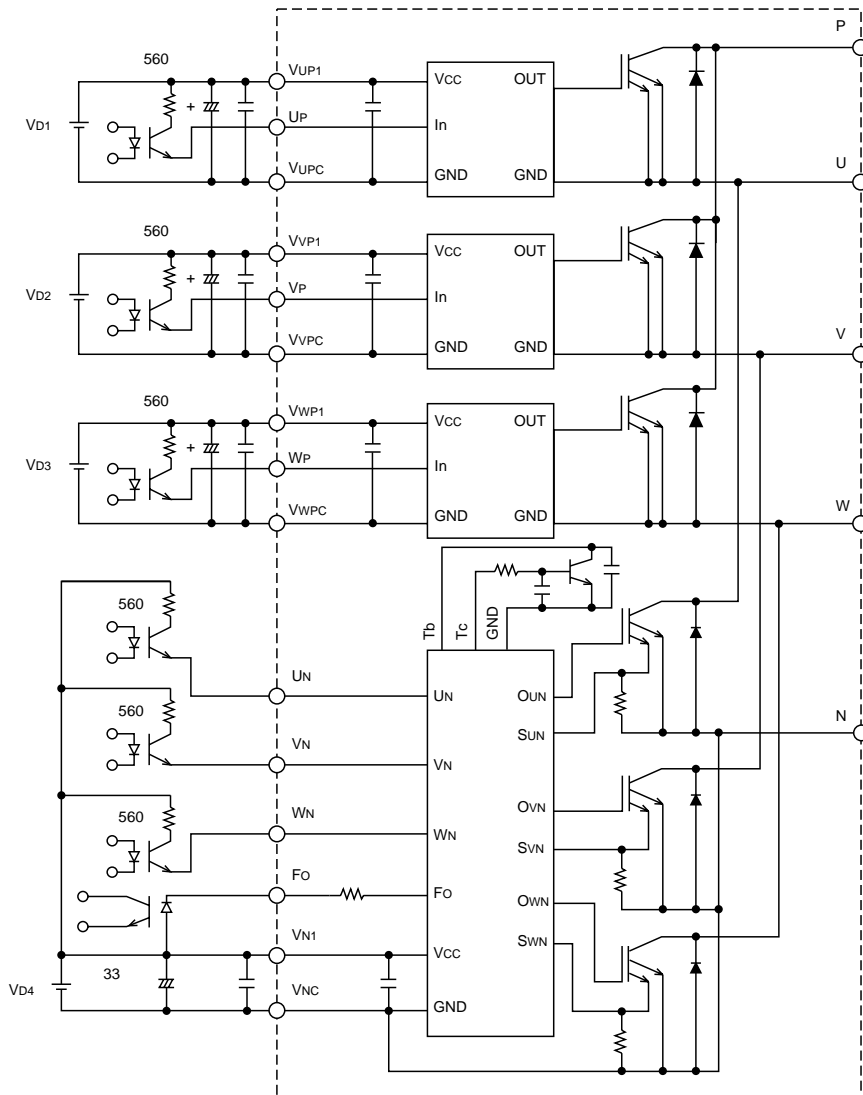


Fig. 7 Dead time measurement point example

PM50CTJ060-3

INSULATED PACKAGE
FLAT-BASE TYPE



NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each switching opto-coupler.
- Slow switching opto-coupler : CTR = 100%~200%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.