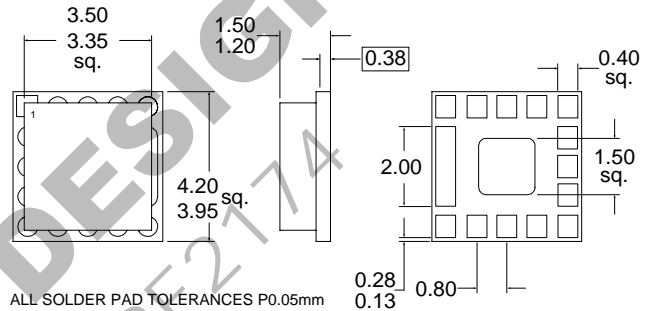


Typical Applications

- 3V DCS1800 (PCN) Cellular Handsets
- 3V DCS1900 (PCS) Cellular Handsets
- 3V Dual-Band/Triple-Band Handsets
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- GPRS Compatible

Product Description

The RF2140 is a high power, high efficiency power amplifier module offering high performance in GSM or GPRS applications. The device is manufactured on an advanced GaAs HBT process, and has been designed for use as the final RF amplifier in DCS1800/1900 hand held-digital cellular equipment and other applications in the 1700MHz to 2000MHz band. On-board power control provides over 65dB of control range with an analog voltage input, and provides power down with a logic "low" for standby operation. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power and efficiency characteristics. The RF2140 can be used together with the RF2138 for dual-band operation. The device is packaged in an ultra-small ceramic package, minimizing the required board space.



ALL SOLDER PAD TOLERANCES P0.05mm

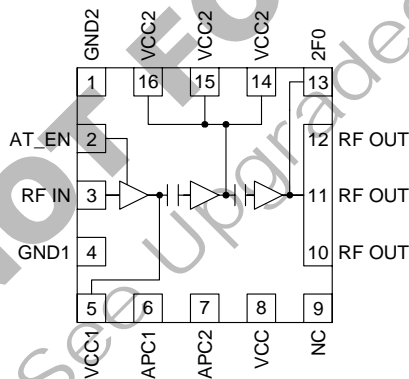
Optimum Technology Matching® Applied

- Si BJT       GaAs HBT       GaAs MESFET  
 Si Bi-CMOS       SiGe HBT       Si CMOS

Package Style: MP16K01A

Features

- Single 2.7V to 4.8V Supply Voltage
- +33dBm Output Power at 3.5V
- 27dB Gain with Analog Gain Control
- 51% Efficiency
- 1700MHz to 1950MHz Operation
- Supports DCS1800 and PCS1900



Functional Block Diagram

Ordering Information

- RF2140      3V DCS Power Amplifier  
 RF2140 PCBA      Fully Assembled Evaluation Board

RF Micro Devices, Inc.  
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<http://www.rfmd.com>

# RF2140

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V <sub>DC</sub>
Power Control Voltage (V <sub>APC</sub> )	-0.5 to +3.0	V
Enable Voltage (V <sub>AT_EN</sub> )	-0.5 to +3.0	V
DC Supply Current	1500	mA
Input RF Power	+13	dBm
Duty Cycle at Max Power	50	%
Output Load VSWR	10:1	
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C



**Caution!** ESD sensitive device.

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POWER AMPLIFIERS

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					Temp=25 °C, V <sub>CC</sub> =3.5V, V <sub>APC1,2</sub> =2.6V, V <sub>AT_EN</sub> =2.6V, P <sub>IN</sub> =+6dBm, Freq=1710MHz to 1910MHz, 25% Duty Cycle, pulse width=1154µs
Operating Frequency Range		1710 to 1785 1850 to 1910		MHz MHz	See application schematic for tuning details. A different tuning is required.
Usable Frequency Range		1700 to 2000		MHz	
Maximum Output Power	+32 +31.5	+33 +32.8 +31.5		dBm dBm dBm	Temp=25 °C, V <sub>CC</sub> =3.5V, V <sub>APC1,2</sub> =2.6V Temp=+25 °C, V <sub>CC</sub> =3.2V, V <sub>APC1,2</sub> =2.6V Temp=+85 °C, V <sub>CC</sub> =3.2V, V <sub>APC1,2</sub> =2.6V
Total Efficiency	+29.5 45	+30 51 51 15 10		dBm %	Temp=25 °C, V <sub>CC</sub> =2.7V, V <sub>APC1,2</sub> =2.6V Temp=+85 °C, V <sub>CC</sub> =2.7V, V <sub>APC1,2</sub> =2.6V At P <sub>OUT,MAX</sub> , V <sub>CC</sub> =3.5V At P <sub>OUT,MAX</sub> , V <sub>CC</sub> =3.0V
Recommended Input Power Range	+5	+7	+9	dBm	P <sub>OUT</sub> =+20 dBm P <sub>OUT</sub> =+10 dBm
Output Noise Power			-79	dBm	RBW=100kHz, 1805MHz to 1880MHz and 1930MHz to 1990MHz, P <sub>OUT,MIN</sub> <P <sub>OUT</sub> <P <sub>OUT,MAX</sub> , P <sub>IN,MIN</sub> <P <sub>IN</sub> <P <sub>IN,MAX</sub> , V <sub>CC</sub> =3.0V to 5.0V
Forward Isolation		-37 -40	-30 -35	dBm dBm	V <sub>APC1,2</sub> =0.2V, P <sub>IN</sub> =+10 dBm V <sub>APC1,2</sub> =0.2V, P <sub>IN</sub> =+6 dBm
Second Harmonic		-60	-45	dBc	
Third Harmonic		-65	-50	dBc	
Fourth Harmonic		-50	-45	dBc	
Fifth Harmonic		-50	-45	dBc	
Sixth Harmonic		-50	-45	dBc	
All Other Non-Harmonic Spurious			-36	dBm	
Input Impedance		50		Ω	
Input VSWR			2.2:1 3:1		P <sub>OUT,MAX</sub> -5dB<P <sub>OUT</sub> <P <sub>OUT,MAX</sub> P <sub>OUT</sub> <P <sub>OUT,MAX</sub> -5dB
Output Load VSWR	10:1				Spurious<-36dBm, V <sub>APC1,2</sub> =0.2V to 2.6V, RBW=100kHz
Output Load Impedance		4.5-j3.9		Ω	Load Impedance presented at RF OUT pin

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Power Control</b>					
Power Control "ON"			2.6	V	Maximum P <sub>OUT</sub> , Voltage supplied to the input
Power Control "OFF"	0.2	0.5		V	Minimum P <sub>OUT</sub> , Voltage supplied to the input
Attenuator Enable "ON"	2.5	2.6	2.85	V	For maximum isolation when V <sub>APC</sub> is low
Attenuator Enable "OFF"	0.2	0.5		V	For power down mode
Power Control Range	62	68		dB	V <sub>APC1,2</sub> =0.2V to 2.6V, V <sub>AT_EN</sub> =2.6V, P <sub>IN</sub> =+10dBm
Gain Control Slope		100		dB/V	P <sub>OUT</sub> =-10dBm to +33dBm
APC Input Capacitance			10	pF	DC to 2MHz
APC Input Current		4.5	5	mA	V <sub>APC1,2</sub> =2.6V
			10	μA	V <sub>APC1,2</sub> =0V
AT_EN Input Current			500	μA	V <sub>AT_EN</sub> =2.6V, V <sub>APC1,2</sub> =0V
			10	μA	V <sub>AT_EN</sub> =0V, V <sub>APC1,2</sub> =0V
Turn On/Off Time			100	ns	
<b>Power Supply</b>					
Power Supply Voltage	2.7	3.5	4.8	V	Specifications
			5.5	V	Nominal operating limits, P <sub>OUT</sub> <+33dBm
				V	With maximum output load VSWR 6:1, P <sub>OUT</sub> <+33dBm
Power Supply Current	55	1.3	295	A	DC Current at P <sub>OUT,MAX</sub>
		1	10	mA	Idle Current, P <sub>IN</sub> <-30dBm
		1	10	μA	P <sub>IN</sub> <-30dBm, V <sub>APC1,2</sub> =0.2V
		1	10	μA	P <sub>IN</sub> <-30dBm, V <sub>APC1,2</sub> =0.2V, Temp=+85°C

# RF2140

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POWER AMPLIFIERS

Pin	Function	Description	Interface Schematic
1	<b>GND2</b>	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance. This pin is internally connected to the ground slug.	See pin 15.
2	<b>AT_EN</b>	Control input for the PIN diode. The purpose of the PIN diode is to attenuate the RF input drive level when the $V_{APC}$ is low. This serves both to reduce the leakage through the device cause by self biasing when driving with high level at the RF input, as well as to maintain a good input match when the bias of the input stage is turned off. When this pin is "high" the PIN diode control is turned on. See the Theory of Operation for more details.	
3	<b>RF IN</b>	RF Input. This is a 50Ω input, but the actual impedance depends on the interstage matching network connected to pin 5. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
4	<b>GND1</b>	Ground connection for the pre-amplifier stage. Keep traces physically short and connect immediately to the ground plane for best performance. It is important for stability that this pin has it's own vias to the groundplane, to minimize any common inductance.	See pin 3.
5	<b>VCC1</b>	Power supply for the pre-amplifier stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the inter-stage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	See pin 3.
6	<b>APC1</b>	Power Control for the driver stage and pre-amplifier. When this pin is "low," all circuits are shut off. A "low" is typically 0.5V or less at room temperature. A shunt bypass capacitor is required. During normal operation this pin is the power control. Control range varies from about 1.0V for -10dBm to 2.6V for +33dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application information for more details. The maximum current into this pin is 5mA when $V_{APC1}=2.6V$ , and 0mA when $V_{APC}=0V$ .	
7	<b>APC2</b>	Power Control for the output stage. See pin 6 for more details.	See pin 6.
8	<b>VCC</b>	Power supply for the bias circuits.	See pin 6.
9	<b>NC</b>	Not connected. Connect this pin to the ground plane for compatibility with future packages.	
10	<b>RF OUT</b>	RF Output and power supply for the output stage. Bias voltage for the final stage is provided through this wide output pin. An external matching network is required to provide the optimum load impedance.	
11	<b>RF OUT</b>	Same as pin 10.	Same as pin 10.
12	<b>RF OUT</b>	Same as pin 10.	Same as pin 10.
13	<b>2F0</b>	Connection for the second harmonic trap. This pin is internally connected to the RF OUT pins. The bonding wire together with an external capacitor form a series resonator that should be tuned to the second harmonic frequency in order to increase efficiency and reduce spurious outputs.	Same as pin 10.
14	<b>VCC2</b>	Same as pin 15.	

Pin	Function	Description	Interface Schematic
15	VCC2	Power supply for the driver stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Please refer to the application schematic for proper configuration, and note that position and value of the components are important.	<p>The schematic shows a shunt inductor connected between the VCC2 supply and the output node. A series capacitor is connected between the output node and the GND2 ground. The output node is also connected to the base of a transistor, which is biased from previous stages.</p>
16	VCC2	Same as pin 15.	Same as pin 15.
Pkg Base	GND	Ground connection for the output stage. This pad should be connected to the groundplane by vias directly under the device. A short path is required to obtain optimum performance, as well as to provide a good thermal path to the PCB for maximum heat dissipation.	

**NOT FOR NEW DESIGNS**  
 See Upgraded Product RF2174

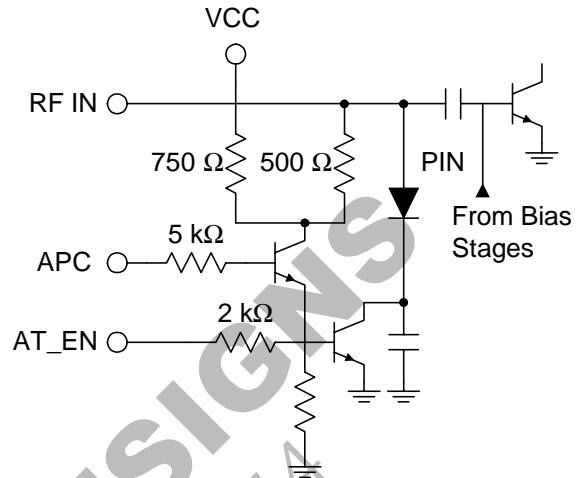
## Theory of Operation and Application Information

The RF2140 is a three-stage device with 28 dB gain at full power. Therefore, the drive required to fully saturate the output is +5dBm. Based upon HBT (Heterojunction Bipolar Transistor) technology, the part requires only a single positive 3V supply to operate to full specification. Power control is provided through a single pin interface, with a separate Power Down control pin. The final stage ground is achieved through the large pad in the middle of the backside of the package. First and second stage grounds are brought out through separate ground pins for isolation from the output. These grounds should be connected directly with vias to the PCB ground plane, and not connected with the output ground to form a so called "local ground plane" on the top layer of the PCB. The output is brought out through the wide output pad, and forms the RF output signal path.

The amplifier operates in near Class C bias mode. The final stage is "deep AB", meaning the quiescent current is very low. As the RF drive is increased, the final stage self-biases, causing the bias point to shift up and, at full power, draws about 1500mA. The optimum load for the output stage is approximately  $4.5\Omega$ . This is the load at the output collector, and is created by the series inductance formed by the output bond wires, vias, and microstrip, and 2 shunt capacitors external to the part. The optimum load impedance at the RF Output pad is  $4.5-j3.9\Omega$ . With this match, a  $50\Omega$  terminal impedance is achieved. The input is internally matched to  $50\Omega$  with just a blocking capacitor needed. This data sheet defines the configuration for GSM operation.

The input is DC coupled; thus, a blocking cap must be inserted in series. Also, the first stage bias may be adjusted by a resistive divider with high value resistors on this pin to  $V_{PC}$  and ground. For nominal operation, however, no external adjustment is necessary as internal resistors set the bias point optimally.

When the device is driven at maximum input power self biasing would occur. This results in less isolation than one would expect, and the maximum output power would be about -15dBm. If the drive power to the PA is turned on before the GSM ramp-up, higher isolation is required. In order to meet the GSM system specs under those conditions, a PIN diode attenuator connected to the input can be turned on. The figure below shows how the attenuator and its controls are connected.



The current through the PIN diode is controlled by two signals: AT\_EN and APC. The AT\_EN signal allows current through the PIN diode and is an on/off function. The APC signal controls the amount of current through the PIN diode. Normally, the AT\_EN signal will be derived from the VCO ENABLE signal available in most GSM handset designs. If maximum isolation is needed before the ramp-up, the AT\_EN signal needs to be turned on before the RF power is applied to the device input. The current into this pin is not critical, and can be reduced to a few hundred micro amps with an external series resistor. Without the resistor, the pin will draw about  $700\mu A$ .

Because of the inverting stage at the APC input, the current through the PIN diode is inverted from the APC voltage. Thus, when  $V_{APC}$  is high for maximum output power, the attenuator is turned off to obtain maximum drive level for the first RF stage. When  $V_{APC}$  is low for maximum isolation, the attenuator is be turned on to reduce the drive level and to avoid self-biasing.

The PIN diode is dimensioned such that a low  $V_{APC}$  the impedance of the diode is about 50 Ohm. Since the input impedance of the first RF stage become very high when the bias is turned off, this topology will maintain a good input impedance over the entire  $V_{APC}$  control range.

VCC1 and VCC2 provide supply voltage to the first and second stage, as well as provides some frequency selectivity to tune to the operating band. Essentially,

the bias is fed to this pin through a short microstrip. A bypass capacitor sets the inductance seen by the part, so placement of the bypass cap can affect the frequency of the gain peak. This supply should be bypassed individually with 100pF capacitors before being combined with  $V_{CC}$  for the output stage to prevent feedback and oscillations.

The RF OUT pin provides the output power. Bias for the final stage is fed to this output line, and the feed must be capable of supporting the approximately 1.5A of current required. Care should be taken to keep the losses low in the bias feed and output components. A narrow microstrip line is recommended because DC losses in a bias choke will degrade efficiency and power.

While the part is safe under CW operation, maximum power and reliability will be achieved under pulsed conditions. The data shown in this data sheet is based on a 12.5% duty cycle and a 600 $\mu$ s pulse, unless specified otherwise.

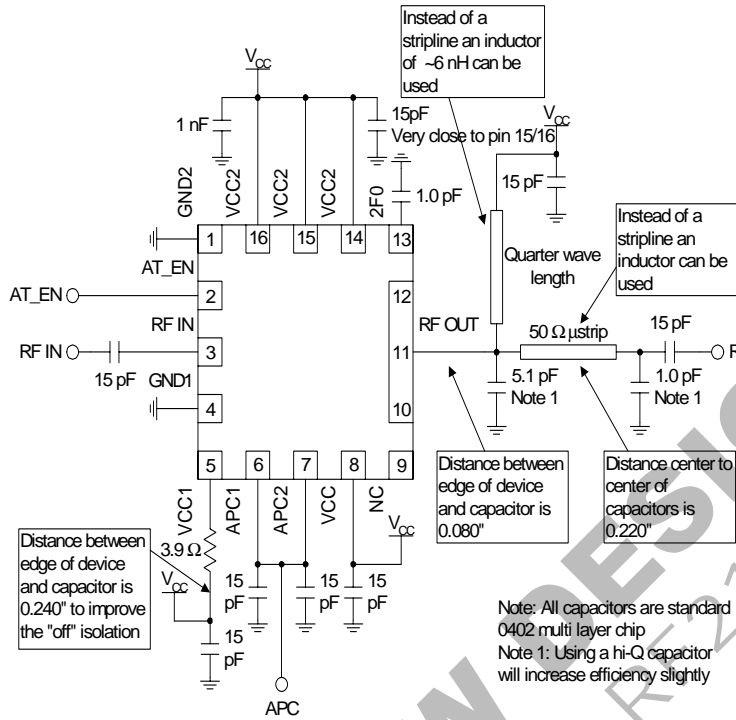
The part will operate over a 3.0V to 5.0V range. Under nominal conditions, the power at 3.5V will be greater than +32dBm at +85°C. As the voltage is increased, however, the output power will increase. Thus, in a system design, the ALC (Automatic Level Control) Loop will back down the power to the desired level. This must occur during operation, or the device may be damaged from too much power dissipation. At 5.0V, over +36dBm may be produced; however, this level of power is not recommended, and can cause damage to the device.

The HBT breakdown voltage is >20V, so there is no issue with overvoltage. However, under worst-case conditions, with the RF drive at full power during transmit, and the output VSWR extremely high, a low load impedance at the collector of the output transistors can cause currents much higher than normal. Due to the bipolar nature of the devices, there is no limitation on the amount of current the device will sink, and the safe current densities could be exceeded.

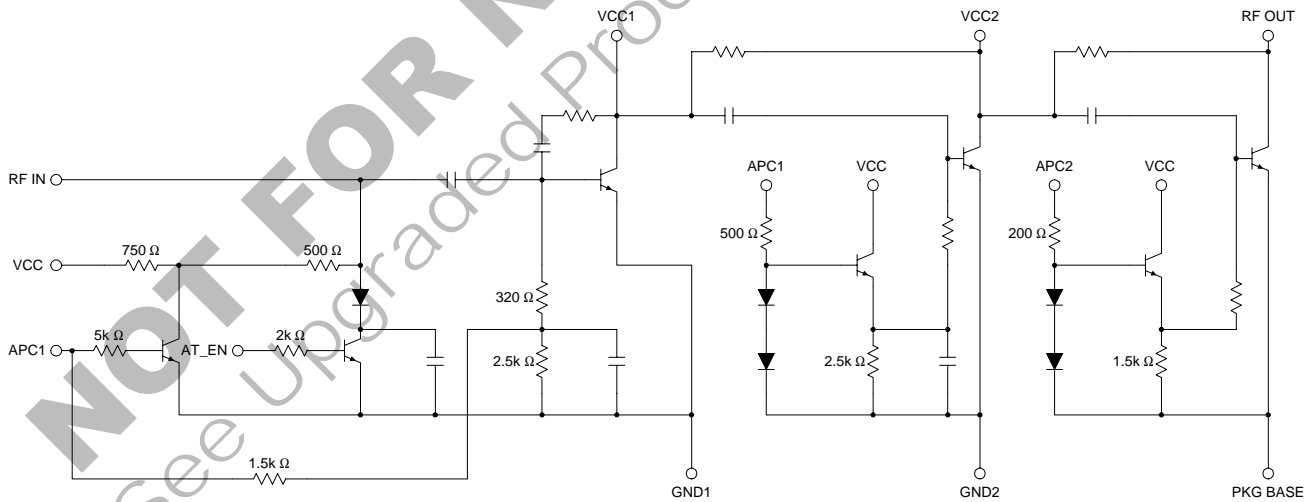
High current conditions are potentially dangerous to any RF device. High currents lead to high channel temperatures and may force early failures. The RF2140 includes temperature compensation circuits in the bias network to stabilize the RF transistors, thus limiting the current through the amplifier and protecting the devices from damage. The same mechanism works to compensate the currents due to ambient temperature variations.

To avoid excessively high currents it is important to control the  $V_{APC}$  when operating at supply voltages higher than 4.0V, such that the maximum output power is not exceeded.

## Application Schematic

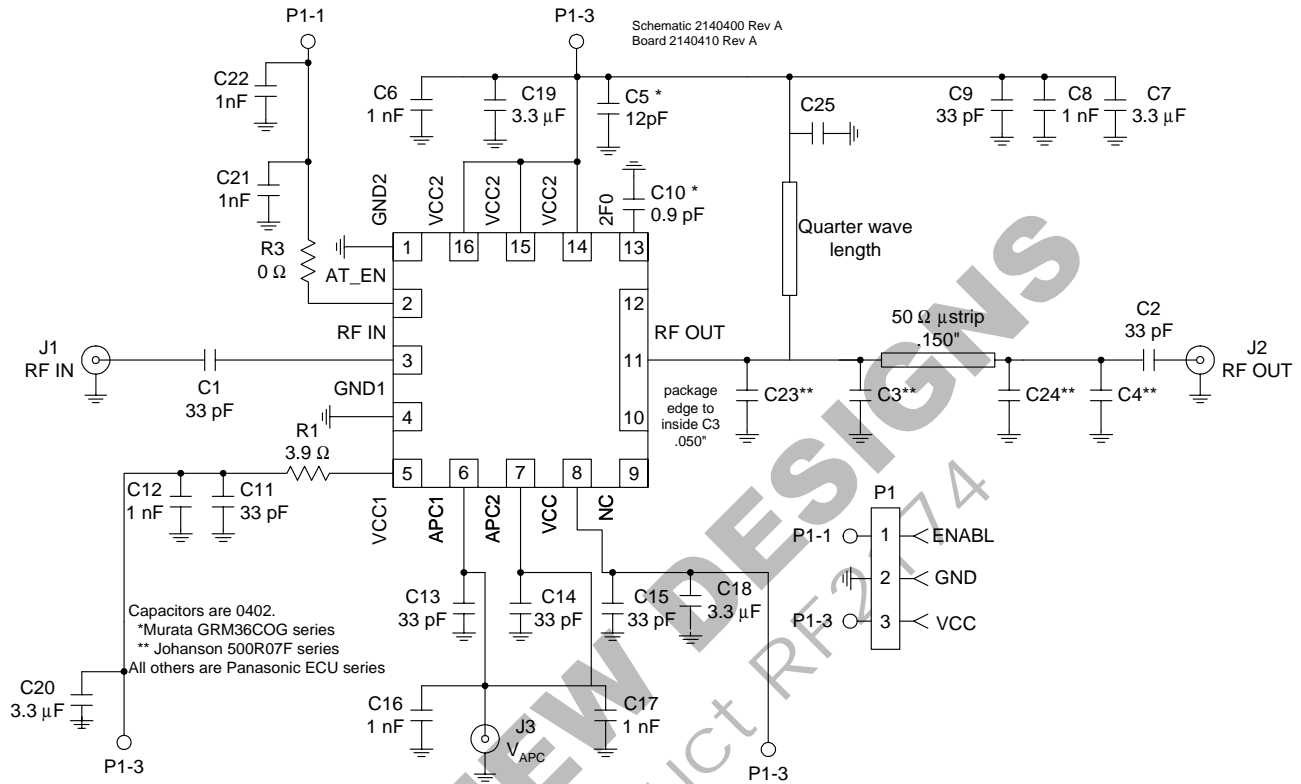


## Internal Schematic





## Evaluation Board Schematic (Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)



Band	C3 (pF)	C4 (pF)	C23 (pF)	C24 (pF)	C25 (pF)
DCS	5.1	1.8	N/I	N/I	N/I
PCS	3.9	1.2	0.5	0.6	0.5

# RF2140

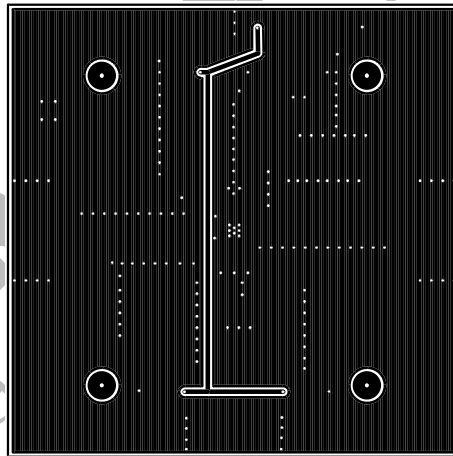
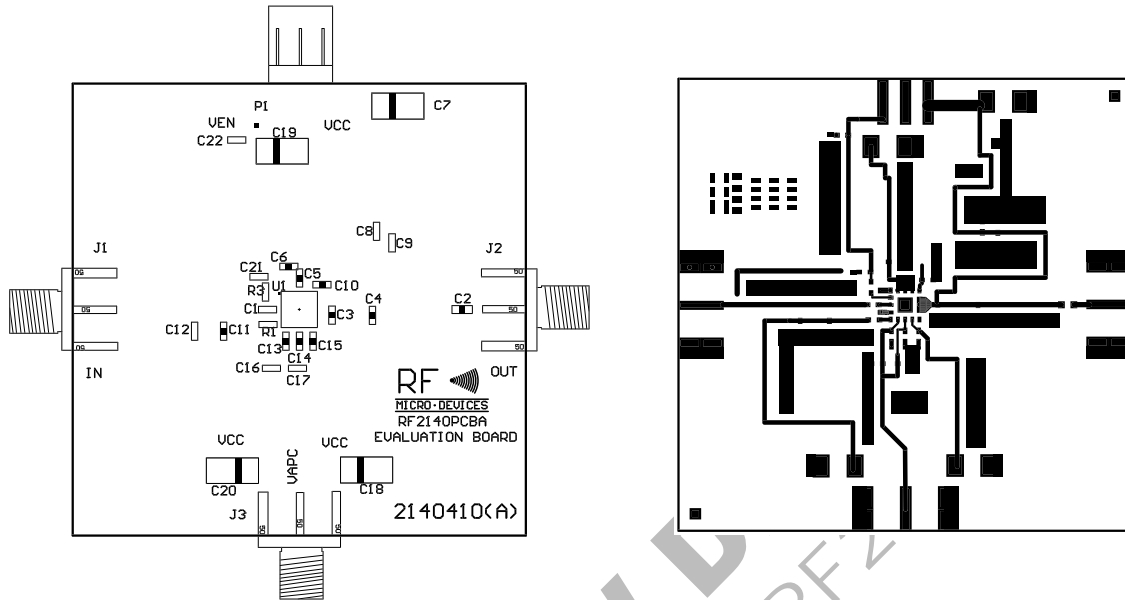
## Evaluation Board Layout

Board size 2.0" x 2.0"

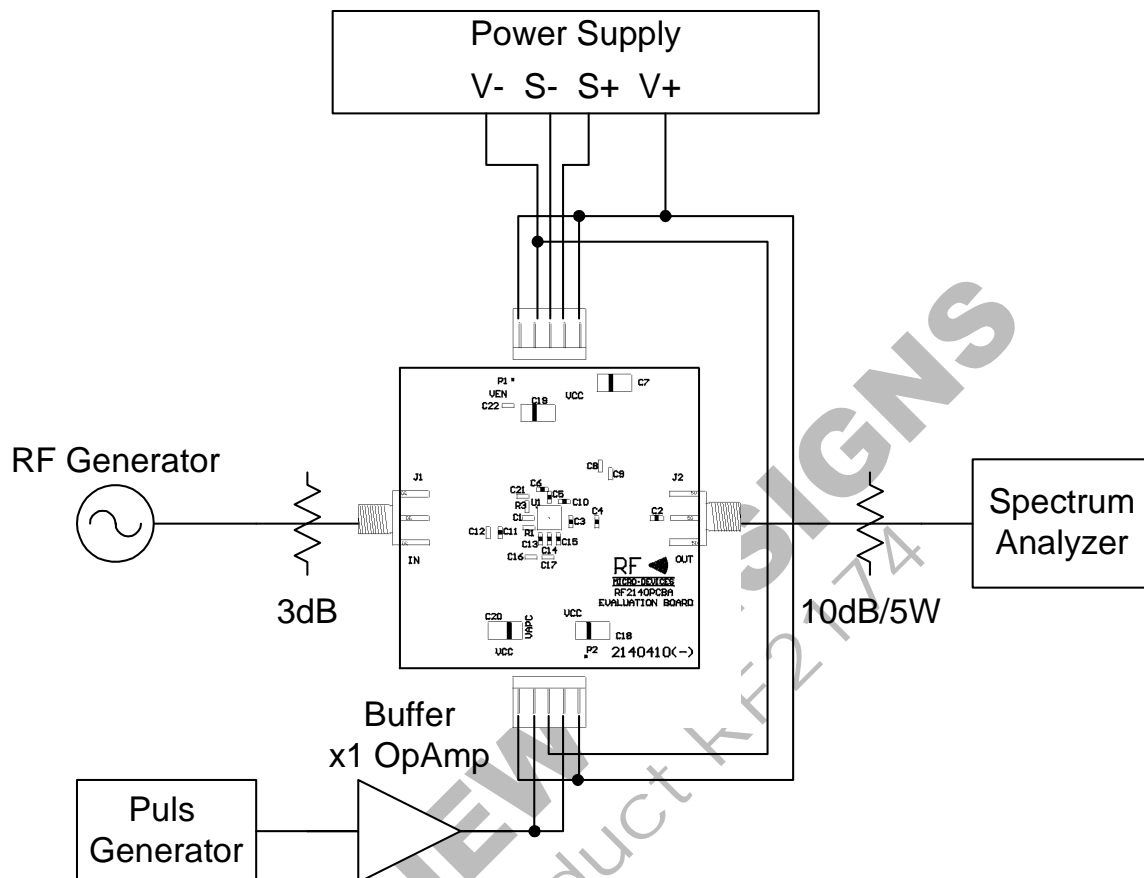
Board Thickness 0.014"; Board Material FR-4; Multi-Layer

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POWER AMPLIFIERS



## Typical Test Setup



A buffer amplifier is recommended because the current into the  $V_{APC}$  changes with voltage. As an alternative, the voltage may be monitored with an oscilloscope.

## Notes about testing the RF2140

The test setup shown above includes two attenuators. The 3dB pad at the input is to minimize the effects that the switching of the input impedance of the PA has on the signal generator. When  $V_{APC}$  is switched quickly, the resulting input impedance change can cause the signal generator to vary its output signal, either in output level or in frequency. Instead of an attenuator an isolator may also be used. The attenuator at the output is to prevent damage to the spectrum analyzer, and should be able to handle the power.

It is important not to exceed the rated supply current and output power. When testing the device at higher than nominal supply voltage, the  $V_{APC}$  should be adjusted to avoid the output power exceeding +36dBm. During load-pull testing at the output it is important to monitor the forward power through a directional coupler. The forward power should not exceed +36dBm, and  $V_{APC}$  needs to be adjusted accordingly. This simulates the behavior for the power control loop in this respect. To avoid damage, it is recommended to set the power supply to limiting the current during the burst, not to exceed the maximum current rating.

**NOT FOR NEW DESIGNS**  
See Upgraded Product RF2174