CMOS 8-Bit Microcontroller

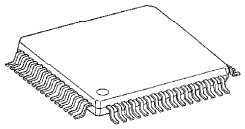
TMP86CM23U, TMP86CP23U

The TMP86CM23/CP23 are the high-speed, high-performance and low power consumption 8-bit microcomputer, including ROM, RAM, Multiply Accumulate Unit, LCD driver, multi-function timer/counter, serial interface (UART/SIO), a 10-bit AD converter and two clock generators on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CM23U	32 K × 8 bits	1.5 K × 8 bits	P-LQFP64-1010-0.50	TMP86PM23U
*TMP86CP23U	48K × 8 bits	2.0 K × 8 bits		*TMP86PS23U

*Under Development

P-LQFP64-1010-0.50



TMP86CM23U
TMP86CP23U

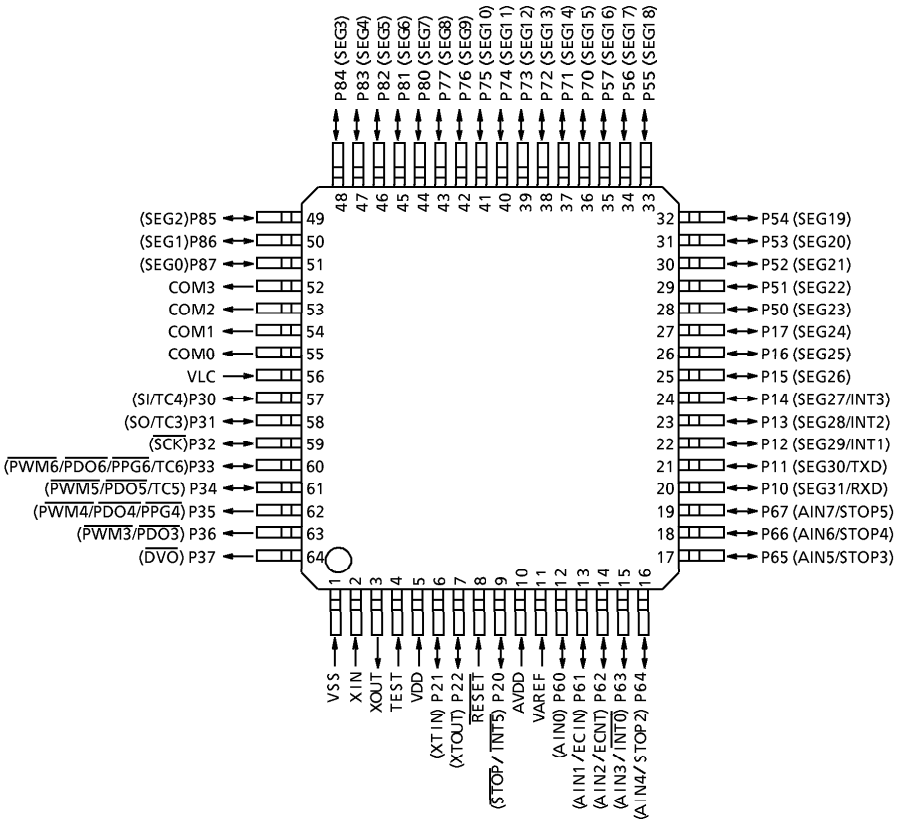
Features

- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types and 731 basic instructions
- 20 interrupt sources (External: 5, Internal: 15)
- Input/Output ports (48 pins)
  (Out of which 32 pins are also used as SEG pins)
- Output ports (3 pins)
- 18-bit timer counter: 1 ch
  - Timer, Event counter, Pulse width measurement, Frequency measurement modes
- 8-bit timer counter: 4 ch
  - Timer, Event counter, PWM output, Programmable divider output, PPG output modes
- Real Time Counter
- Time Base Timer

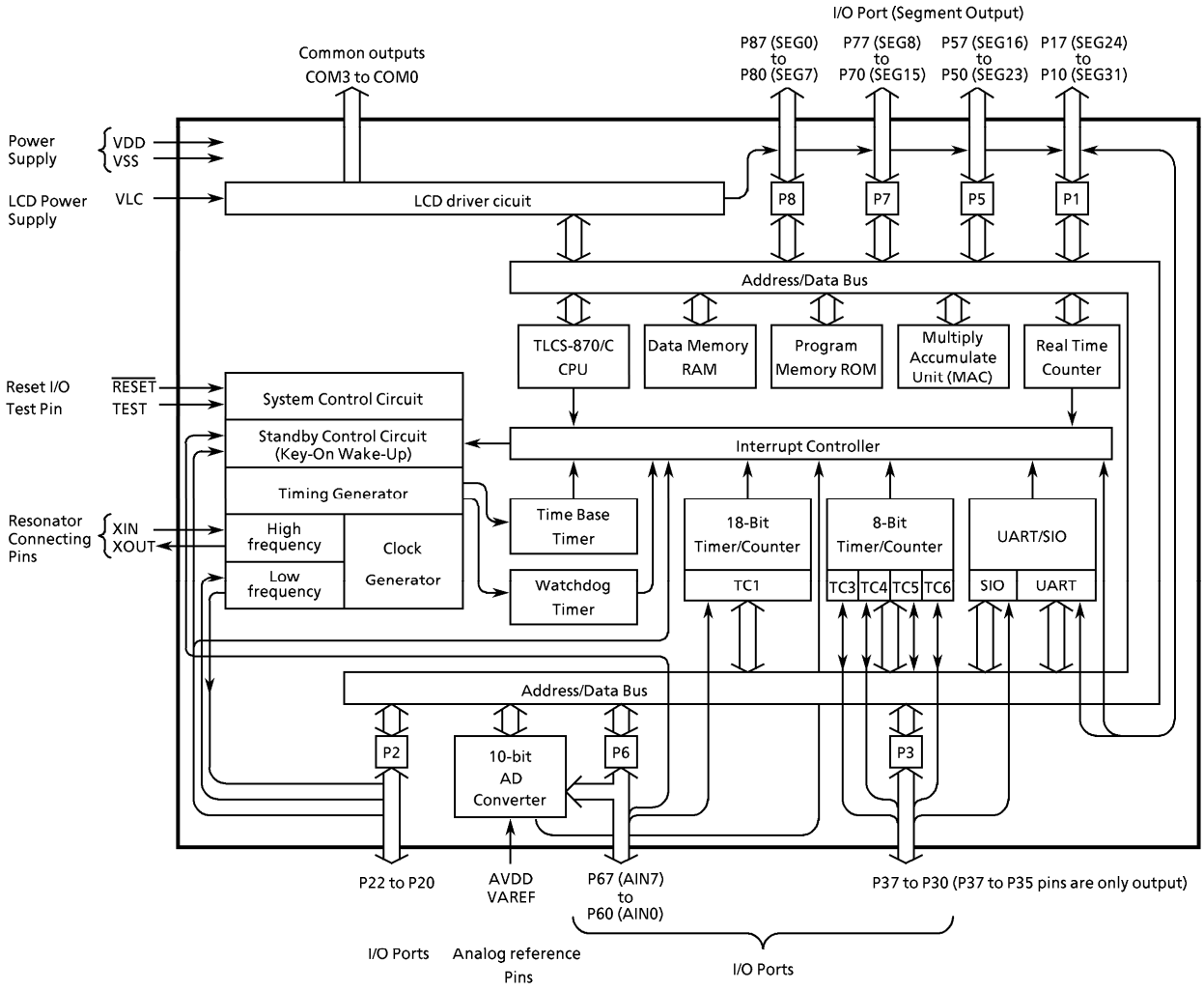
- ◆ Divider output function
- ◆ Watchdog Timer
  - Interrupt source/internal reset generate (programmable)
- ◆ Serial interface
  - 8-bit UART: 1ch
  - 8-bit SIO: 1ch
- ◆ 10-bit successive approximation type AD converter
  - Analog input: 8 ch
- ◆ Multiply accumulate unit (MAC)
  - Multiply or MAC mode are selectable
  - Signed or unsigned operation are selectable
- ◆ Four key-on wake-up pins
- ◆ LCD driver/controller
  - With display memory (16 bytes)
  - LCD direct drive capability (Max 32 seg × 4 com)
  - 1/4, 1/3, 1/2duties or static drive are programmably selectable
- ◆ Dual clock operation
  - Single/dual-clock mode
- ◆ Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/capacitor back-up. Port output hold/High-impedance.
  - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by falling edge of TBTCR<TBTCK> setting.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interruputs.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interruputs.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by falling edge of TBTCR<TBTCK> setting.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- ◆ Wide operating voltage: 1.8 to 5.5 V at 4.2 MHz/32.768 kHz,
  2.7 to 5.5 V at 8 MHz/32.768 kHz,
  3.5 to 5.5 V at 16 MHz/32.768 kHz

Pin Assignments (Top View)

P-LQFP64-1010-0.50



Block Diagram



Pin Functions

Pin Name	Input/Output	Function		
P17 (SEG24)	I/O (Output)	8-bit programmable input/output port (tri- state). Each bit of this port can be individually configured as an input or an output under software control.When used as an input port, an external interrupt input or a UART data input, the P1LCR and P1CR must be cleared to "0". When used as UART output, the P1LCR must be cleared to "0", and the P1CR and P1DR must be set to "1".When used as a LCD segment output, the P1LCR must be set to "1".		LCD segment outputs
P16 (SEG25)	I/O (Output)			
P15 (SEG26)	I/O (Output)			
P14 (SEG27, INT3)	I/O (I/O)		External interrupt 3 input	
P13 (SEG28, INT2)	I/O (I/O)		External interrupt 2 input	
P12 (SEG29, INT1)	I/O (I/O)		External interrupt 1 input	
P11 (SEG30, TXD)	I/O (Output)		UART data output	
P10 (SEG31, RXD)	I/O (I/O)		UART data input	
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch.When used as an input port, an external interrupt input or stop mode release signal input, the P2DR must be set to "1".	Resonator connecting pins(32.768 kHz) For inputting external clock, XTIN is used and XTOUT is opened.	
P21 (XTIN)	I/O (Input)			
P20 ($\overline{INT5}$, $\overline{STOP}$)	I/O (Input)		External interrupt input 5 or STOP mode release signal input	
P37 ($\overline{DVO}$)	Output (Output)	3-bit output port with latch(Nch high current output).When used as a timer/counter output or a divider output, the P3DR must be set to "1".	Divider output	
P36 ($\overline{PWM3}$, $\overline{PDO3}$)	Output (Output)		Timer counter 3 output	
P35 ($\overline{PWM4}$, $\overline{PDO4}$, $\overline{PPG4}$)	Output (Output)		Timer counter 4 output	
P34 ($\overline{PWM5}$, $\overline{PDO5}$, TC5)	I/O (I/O)	5-bit input/output port with latch(P33 and P34 ports are Nch high current output).When used as a timer/counter output or a serial interface output, the P3DR must be set to "1". When used as a timer/counter input or a serial interface input, the P3DR must be set to "1" after P3OUTCR is cleared to "0".	Timer counter 5 input/output	
P33 ($\overline{PWM6}$, $\overline{PDO6}$, $\overline{PPG6}$, TC6)	I/O (I/O)		Timer counter 6 input/output	
P32 ($\overline{SCK}$)	I/O (I/O)		Serial clock input/output	
P31 (SO, TC3)	I/O (I/O)		Serial data output, Timer counter 3 input	
P30 (SI, TC4)	I/O (Input)		Serial data input, Timer counter 4 input	
P57 (SEG16) to P50 (SEG23)	I/O (Output)	8-bit programmable input/output port (tri- state). Each bit of this port can be individually configured as an input or an output under software control.When used as a LCD segment output, the P5LCR must be set to "1".	LCD segment output	
P67 (AIN7, STOP5)	I/O (Input)	8-bit programmable input/output port (tri- state). Each bit of this port can be individually configured as an input or an output under software control.When used as an input port or a timer/ counter input, the P6CR2 must be set to "1" after P6CR1 is cleared to "0". When used as an analog input or a key on wake up input, the P6CR2 must be cleared to "0" after P6CR1 is cleared to "0".	STOP5 input	AD converteranalog inputs
P66 (AIN6, STOP4)	I/O (Input)		STOP4 input	
P65 (AIN5, STOP3)	I/O (Input)		STOP3 input	
P64 (AIN4, STOP2)	I/O (Input)		STOP2 input	
P63 (AIN3, $\overline{INT0}$)	I/O (Input)		External interrupt 0 input	
P62 (AIN2, ECNT)	I/O (Input)		Timer counter 1 input	
P61 (AIN1, ECIN)	I/O (Input)		Timer counter 1 input	
P60 (AIN0)	I/O (Input)			
P77 (SEG8) to P70 (SEG15)	I/O (Output)	8-bit programmable input/output port (tri- state). Each bit of this port can be individually configured as an input or an output under software control.When used as a LCD segment output, the P7LCR must be set to "1".	LCD segment outputs	
P87 (SEG0) to P80 (SEG7)	I/O (Output)	8-bit programmable input/output port (tri- state). Each bit of this port can be individually configured as an input or an output under software control.When used as a LCD segment output, the P8LCR must be set to "1".	LCD segment outputs	
COM3 to COM0	Output	LCD common outputs		
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.		
$\overline{RESET}$	Input	Reset signal input		
TEST	Input	Test pin for out-going test. Be fixed to low.		
VDD, VSS	Power supply	+ 5 V, 0 (GND)		
VAREF		Analog reference voltage inputs(High)		
AVDD		AD circuit power supply		
VLC		LCD drive power supply		

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86CM23/CP23 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86CM23/CP23 memory address map. The general-purpose registers are not assigned to the RAM address space.

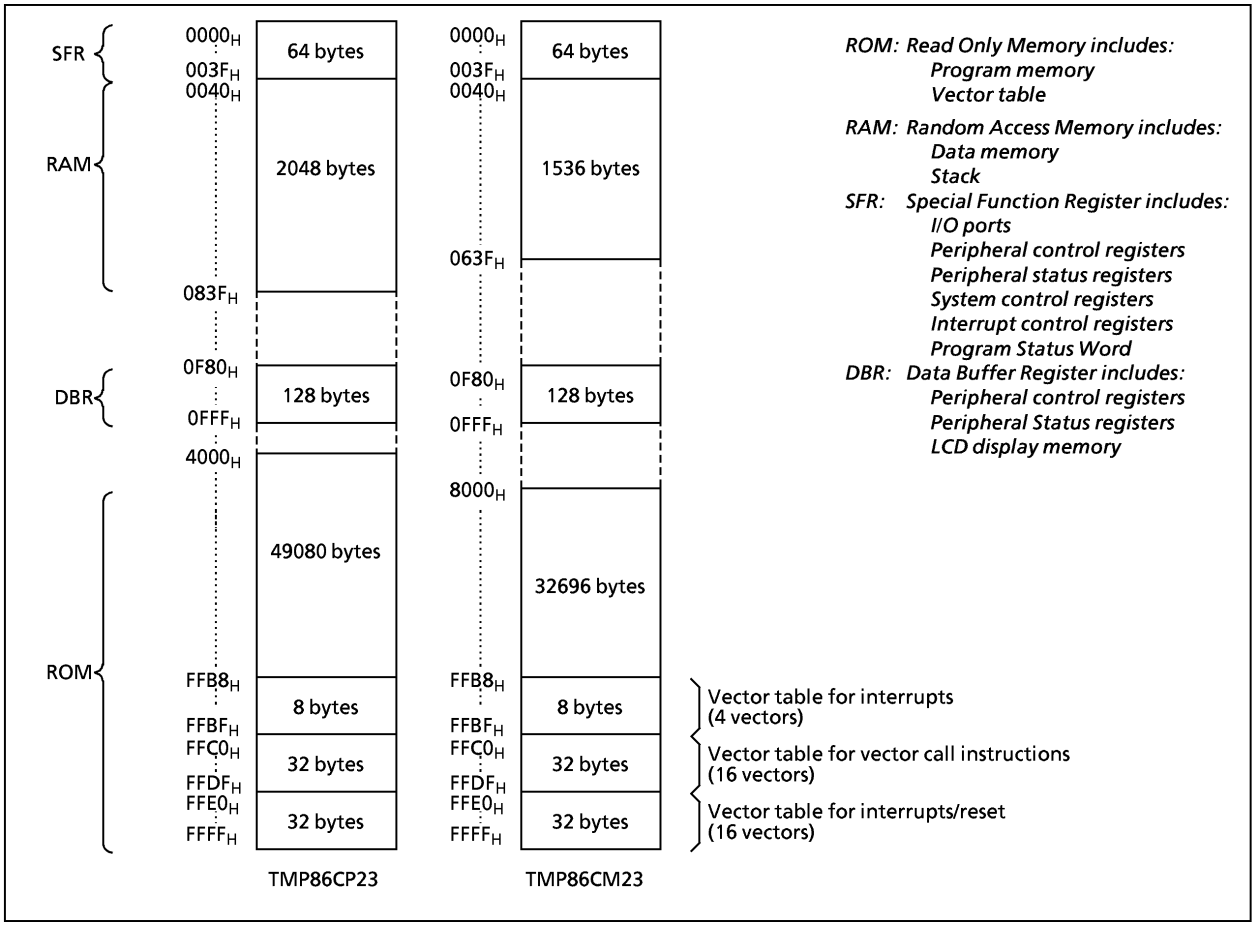


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86CM23 has a 32 K×8 bits (address 8000_H to $FFFF_H$), TMP86CP23 has a 48×8 bits (address 4000_H to $FFFF_H$) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}		– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P1, P30 to P34, P5, P6, P7, P8 Port	– 1.8	mA
	I_{OUT2}	P1, P2, P30 to P32, P5, P6, P7, P8 Port	3.2	
	I_{OUT3}	P33 to P37 Port	30	
Output Current (Total)	ΣI_{OUT1}	P1, P30 to P34, P5, P6, P7, P8 Port	– 30	
	ΣI_{OUT2}	P33 to P37 Port	80	
	ΣI_{OUT3}	P1, P2, P30 to P32, P5, P6, P7, P8 Port	60	
Power Dissipation [T_{opr} = 85°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	3.5	5.5	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW1, 2 mode			
				SLEEP0, 1, 2 mode			
				STOP mode			
Input high Level	V_{IH1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input low Level	V_{IL1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 1.8 to 5.5 V		1.0	4.2	MHz
			V_{DD} = 2.7 to 5.5 V			8.0	
			V_{DD} = 3.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V		–	–	± 2	μA
	I_{IN2}	Sink open drain, Tri-state						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input Resistance	R_{IN1}	TEST pull-down			–	–	± 2	kΩ
	R_{IN2}	RESET pull-up			100	220	450	
Output Leakage Current	I_{LO}	Sink open drain, Tri-state	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V		–	–	± 2	μA
Output High Voltage	V_{OH2}	C-MOS, Tri-st Port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA		4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P3 Port	V_{DD} = 4.5 V, I_{OL} = 1.6mA		–	–	0.4	
Out put Low Current	I_{OL}	High current Port (P33 to P37 Port)	V_{DD} = 4.5 V, I_{OL} = 1.6mA		–	–	0.4	mA
Supply Current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3/0.2 V fc = 16 MHz fs = 32.768 kHz	TMP86CM23	–	10.5	15.0	
Supply Current in IDLE 0, 1, 2 mode					–	6.5	10.0	
Supply Current in SLOW 1 mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz LCD driver is not enable.		–	10	21	μA
Supply Current in SLEEP 1 mode					–	7.5	16.0	
Supply Current in SLEEP 0 mode					–	5.0	12.0	
Supply Current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3/0.2 V fc = 16 MHz fs = 32.768 kHz	TMP86CP23	–	T.B.D	T.B.D	mA
Supply Current in IDLE 0, 1, 2 mode					–	T.B.D	T.B.D	
Supply Current in SLOW 1 mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz LCD driver is not enable.		–	T.B.D	T.B.D	μA
Supply Current in SLEEP 1 mode					–	T.B.D	T.B.D	
Supply Current in SLEEP 0 mode					–	T.B.D	T.B.D	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V		–	0.5	10	
Segment Output Low Resistance	R_{OS1}	SEG Pin			–	20	–	kΩ
Common Output Low Resistance	R_{OC1}	COM Pin			–	20	–	
Segment Output High Resistance	R_{OS2}	SEG Pin			–	200	–	
Common Output High Resistance	R_{OC2}	COM Pin			–	200	–	
Segment/Common Output Voltage	$V_{O2/3}$	SEG/COM Pin	V_{DD} = 5.0 V VLC = 2.0 V		3.8	–	4.2	V
	$V_{O1/2}$				3.3		3.7	
	$V_{O1/3}$				2.8		3.2	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V
Note 2: Input current (I_{IN1}, I_{IN2}); The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.
Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.
Note 5: Output resistors R_{OS} and R_{OC} indicate "ON" when switching levels.
Note 6: $V_{O2/3}$ indicates the output voltage at the 2/3 level when operating in the 1/4 or 1/3 duty mode.
Note 7: $V_{O1/2}$ indicates the output voltage at the 1/2 level when operating in the 1/2 duty or static mode.
Note 8: $V_{O1/3}$ indicates the output voltage at the 1/3 level when operating in the 1/4 or 1/3 duty mode.
Note 9: When using LCD, it is necessary to consider values of Ros 1/2 and Roc 1/2.

AD Conversion Characteristics

(V_{SS} = 0.0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit (Note 6)	A_{VDD}		V_{DD}			
Analog Reference Voltage Range (Note 4)	$\triangle V_{AREF}$		3.5	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 5.5 V V_{SS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		$V_{DD} = A_{VDD}$ = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.0 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 2	

(V_{SS} = 0.0 V, 2.7 V ≦ V_{DD} < 4.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit (Note 6)	A_{VDD}		V_{DD}			
Analog Reference Voltage Range (Note 4)	$\triangle V_{AREF}$		2.5	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 4.5 V V_{SS} = 0.0 V	–	0.5	0.8	mA
Non linearity Error		$V_{DD} = A_{VDD}$ = 2.7 V, V_{SS} = 0.0 V V_{AREF} = 2.7 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 2	

(V_{SS} = 0.0 V, 2.0 V ≦ V_{DD} < 2.7 V, Topr = – 40 to 85°C) Note 5
(V_{SS} = 0.0 V, 1.8 V ≦ V_{DD} < 2.0 V, Topr = – 10 to 85°C) Note 5

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		A_{VDD} – 0.9	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit (Note 6)	A_{VDD}		V_{DD}			
Analog Reference Voltage Range (Note 4)	$\triangle V_{AREF}$	1.8 V ≦ V_{DD} < 2.0 V	1.8	–	–	
		2.0 V ≦ V_{DD} < 2.7 V	2.0	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 2.7 V V_{SS} = 0.0 V	–	0.3	0.5	mA
Non linearity Error		$V_{DD} = A_{VDD}$ = 1.8 V, V_{SS} = 0.0 V V_{AREF} = 1.8 V	–	–	± 4	LSB
Zero Point Error			–	–	± 4	
Full Scale Error			–	–	± 4	
Total Error			–	–	± 4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.10.2 Register Framing".
Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} - V_{SS}$
Note 5: When AD is used with V_{DD} < 2.7 V, the guaranteed temperature range varies with the operating voltage.
Note 6: The AVDD pin should be fixed on the VDD level even though AD converter is not used.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 3.5 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.25	–	4	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.5	–	4	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

(V_{SS} = 0 V, V_{DD} = 1.8 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.95	–	4	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 4.2 MHz	–	119.05	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

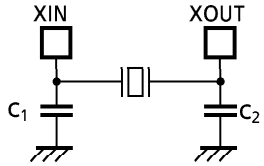
Timer Counter 1 input (ECIN) Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

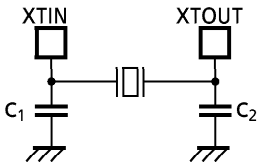
Parameter	Symbol	Condition		Min	Typ.	Max	Unit
TC1 input (ECIN input)	t_{TC1}	Frequency measurement mode V_{DD} = 3.5 to 5.5 V	Single edge count	–	–	16	MHz
			Both edge count	–	–		
		Frequency measurement mode V_{DD} = 2.7 to 5.5 V	Single edge count	–	–	8	
			Both edge count	–	–		
		Frequency measurement mode V_{DD} = 1.8 to 5.5 V	Single edge count	–	–	4.2	
			Both edge count	–	–		

Recommended Oscillating Conditions - 1

(V_{SS} = 0 V, V_{DD} = 1.8 to 5.5 V, Topr = – 40 to 85°C)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL:
http://www.murata.co.jp/search/index.html