DATA SHEET

74ABT648

Octal transceiver/register, inverting (3-State)

Product data
Supersedes data of 1998 Jun 08

2002 Dec 13

Philips
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Octal bus transceiver/register, inverting (3-State) 74ABT648

FEATURES

- Combines 74ABT245 and 74ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: +64 mA / –32 mA
- Power-up 3-state
- Power-up reset
- Live insertion/extraction permitted
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT648 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT648 transceiver/register consists of bus transceiver circuits with inverting 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. Outputs from real-time, or stored registers will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74ABT648.

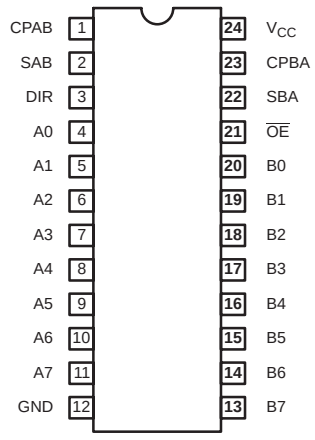
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	5.9	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0 V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0 V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5 V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
24-Pin plastic SO	–40 °C to +85 °C	74ABT648D	SOT137-1
24-Pin Plastic TSSOP Type I	–40 °C to +85 °C	74ABT648PW	SOT355-1

PIN CONFIGURATION

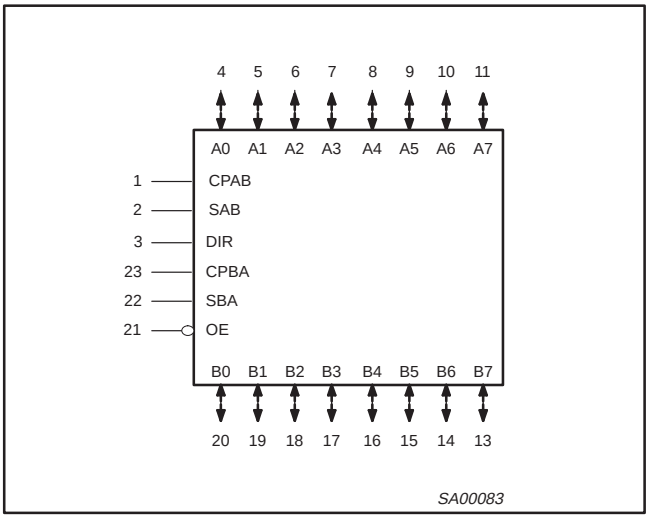


SA00082

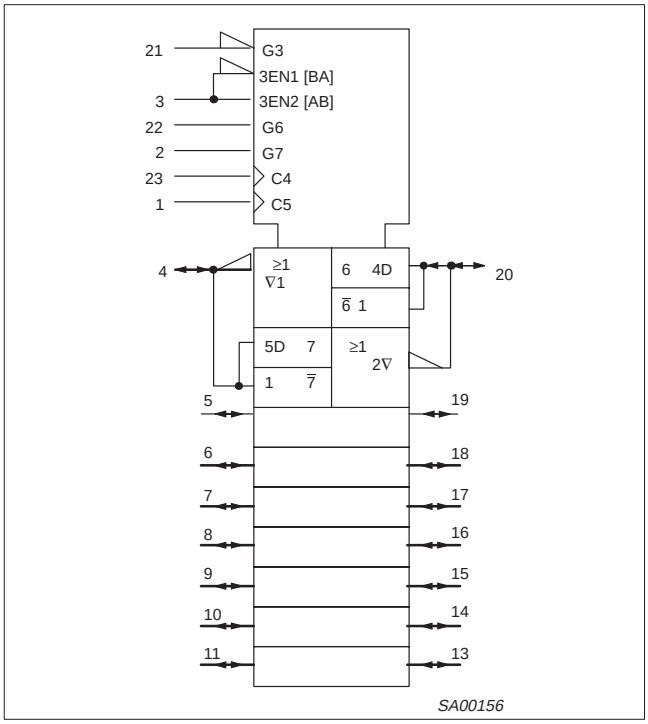
PIN DESCRIPTION

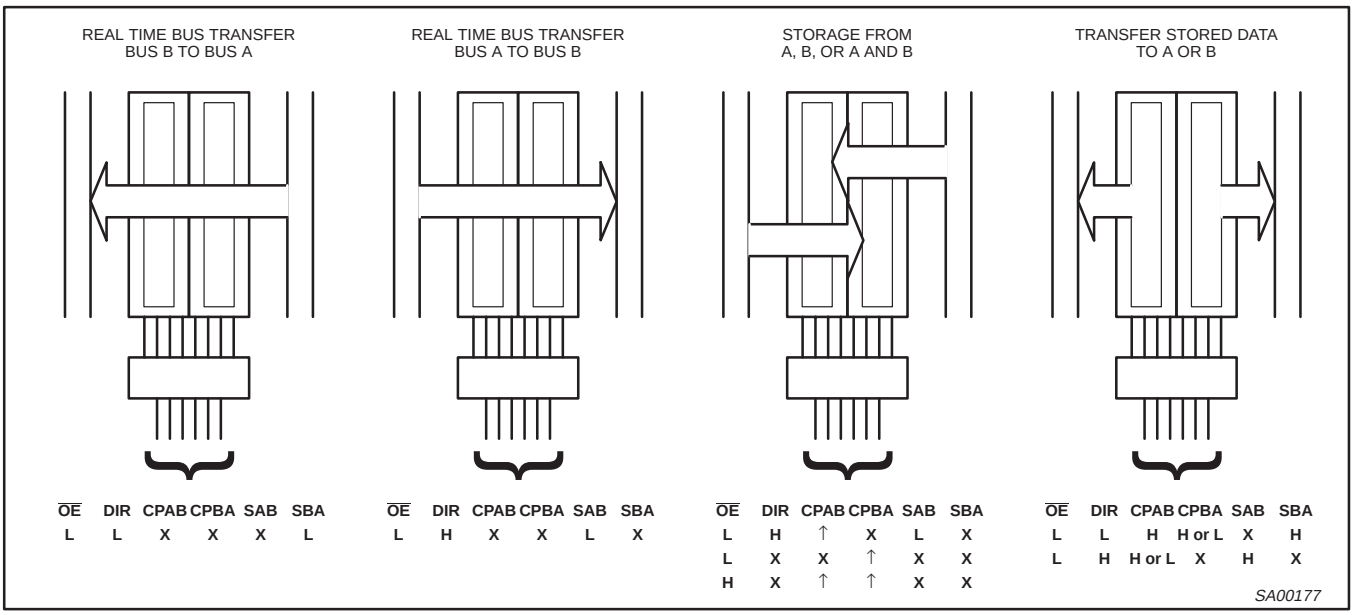
PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-LOW)
12	GND	Ground (0 V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



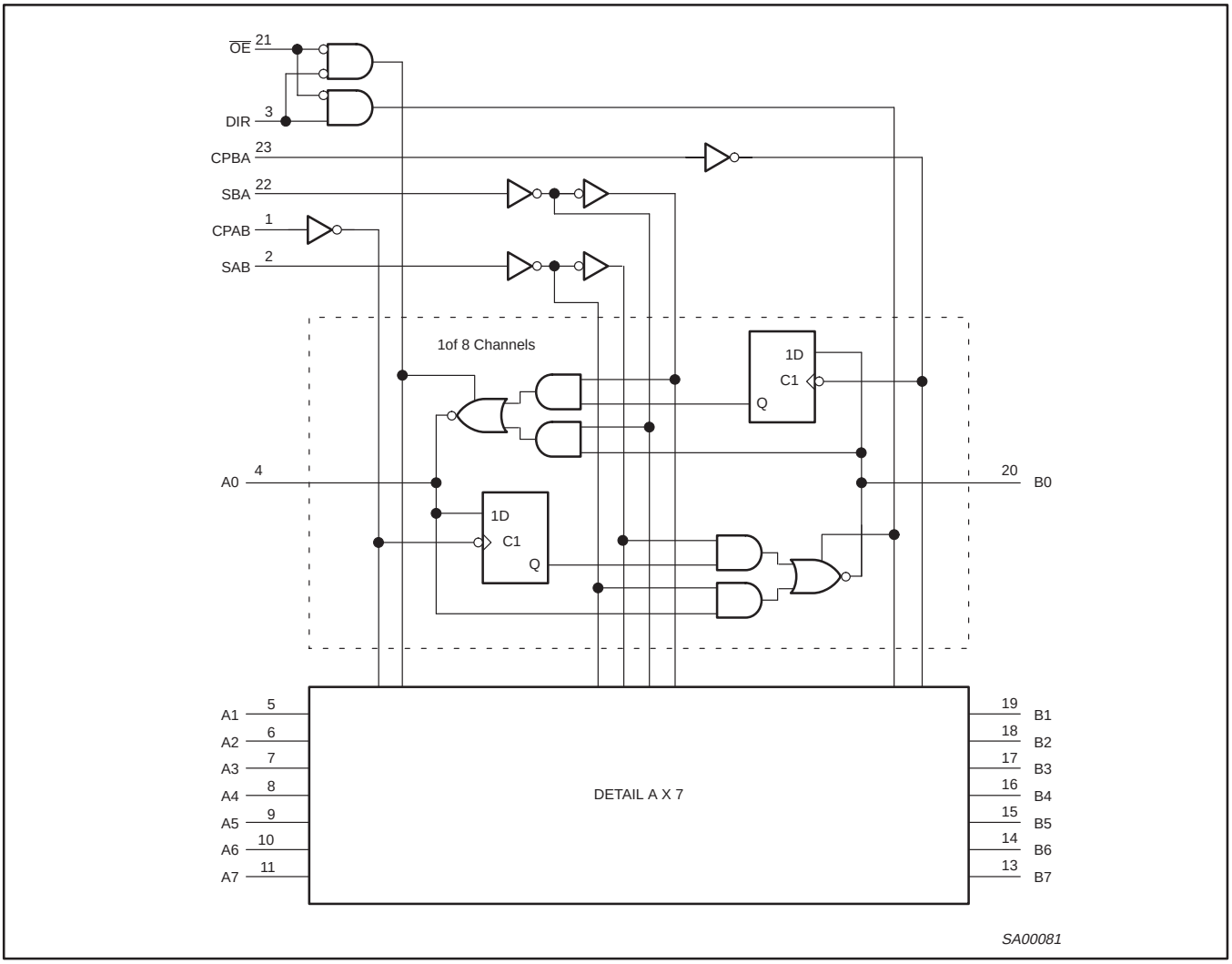


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0		V
V_{IL}	LOW-level Input voltage		0.8	V
I_{OH}	HIGH-level output current		–32	mA
I_{OL}	LOW-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V; I_{IK} = –18 mA		–0.9	–1.2		–1.2	V
V_{OH}	HIGH-level output voltage		V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V
			V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V
			V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.3		2.0		V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
V_{OL}	LOW-level output voltage		V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_{OFF}	Power-off leakage current		V_{CC} = 0.0 V; V_I or $V_O \leq$ 4.5 V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]		V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
I_I	Input leakage current	Control pins	V_{CC} = 5.5 V; V_I = GND or 5.5 V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5 V; V_I = GND or 5.5 V		±5	±100		±100	µA
$I_{IH} + I_{OZH}$	3-State output HIGH current		V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output LOW current		V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output HIGH leakage current		V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5 V; V_O = 2.5 V	–50	–65	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5 V; Outputs HIGH, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5 V; Outputs LOW, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND; V_{CC} = 5.5 V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 msec. From V_{CC} = 2.1 to V_{CC} = 5 V ± 10% a transition time of up to 100 µsec is permitted.

AC CHARACTERISTICS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V			T_{amb} = –40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	200		125		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	5.3 5.9	6.8 7.4	2.2 1.7	7.8 8.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2 3	1.0 1.5	3.6 4.2	5.1 5.6	1.0 1.5	6.1 6.3	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	2 3	1.5 1.5	4.9 5.4	6.1 6.9	1.5 1.5	7.1 7.7	ns
t_{PZH} t_{PZL}	Output enable time OE to An or Bn	5 6	1.0 2.1	4.3 5.5	5.3 7.4	1.0 2.1	6.3 8.8	ns
t_{PHZ} t_{PLZ}	Output disable time OE to An or Bn	5 6	1.5 1.5	6.2 6.0	7.3 7.0	1.5 1.5	8.3 7.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	5 6	1.2 2.5	4.8 6.0	5.7 9.0	1.2 2.5	6.7 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	5 6	1.5 1.5	5.9 6.3	6.7 7.2	1.5 1.5	7.7 8.2	ns

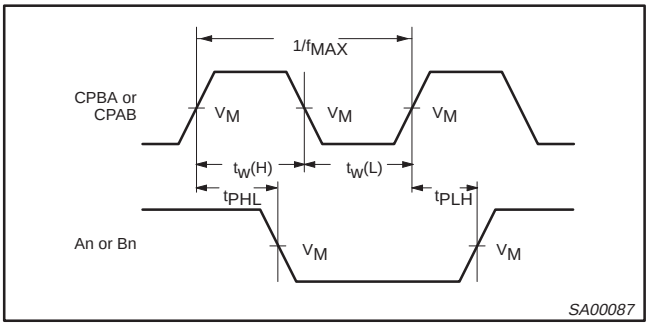
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

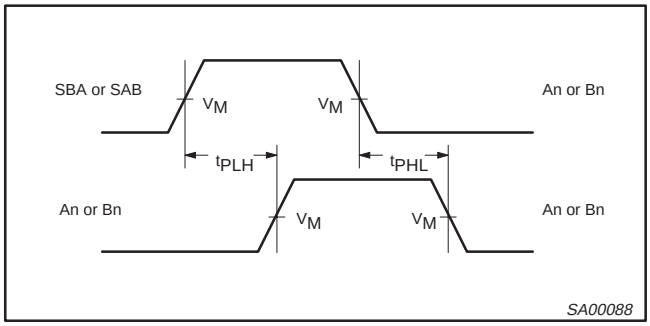
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V		T_{amb} = -40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V	
			Min	Typ	Min	
t_s(H) t_s(L)	Set-up time An to CPAB, Bn to CPBA	4	3.0 3.0	1.5 1.0	3.0 3.0	ns
t_h(H) t_h(L)	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	–0.4 –1.0	0.0 0.0	ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	1	3.5 4.0	2.6 1.0	3.5 4.0	ns

AC WAVEFORMS

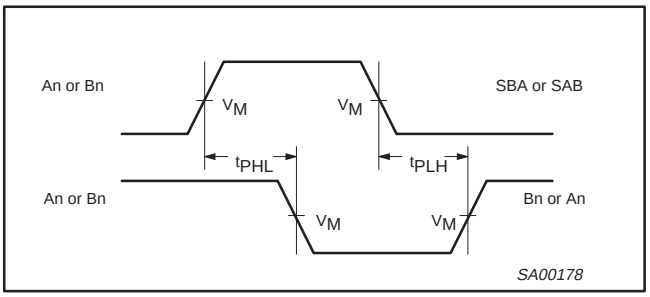
V_M = 1.5 V, V_{IN} = GND to 3.0 V



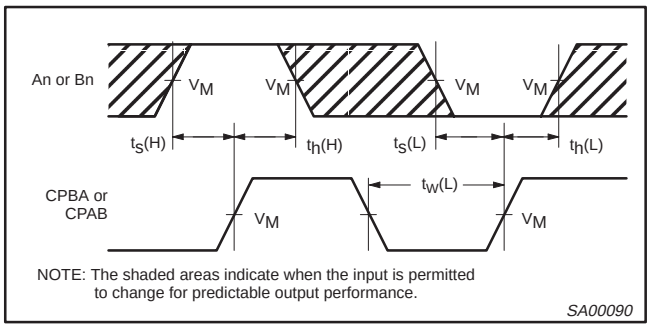
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



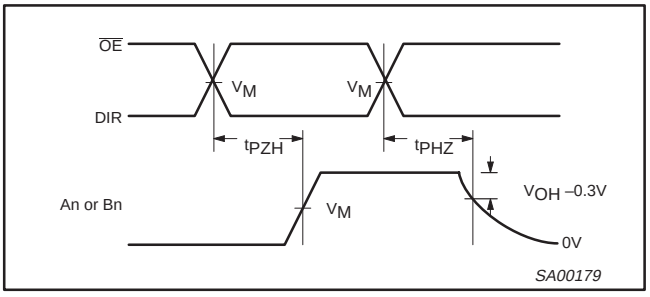
Waveform 2. Propagation Delay, SAB to Bn or SBA to An



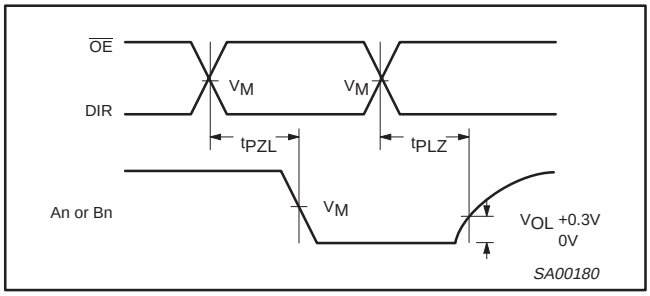
Waveform 3. Propagation Delay, An to Bn or Bn to An, and SBA to An or SAB to Bn



Waveform 4. Data Set-up and Hold Times

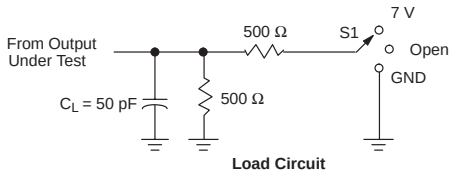


Waveform 5. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level



Waveform 6. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

TEST CIRCUIT AND WAVEFORM



Load Circuit

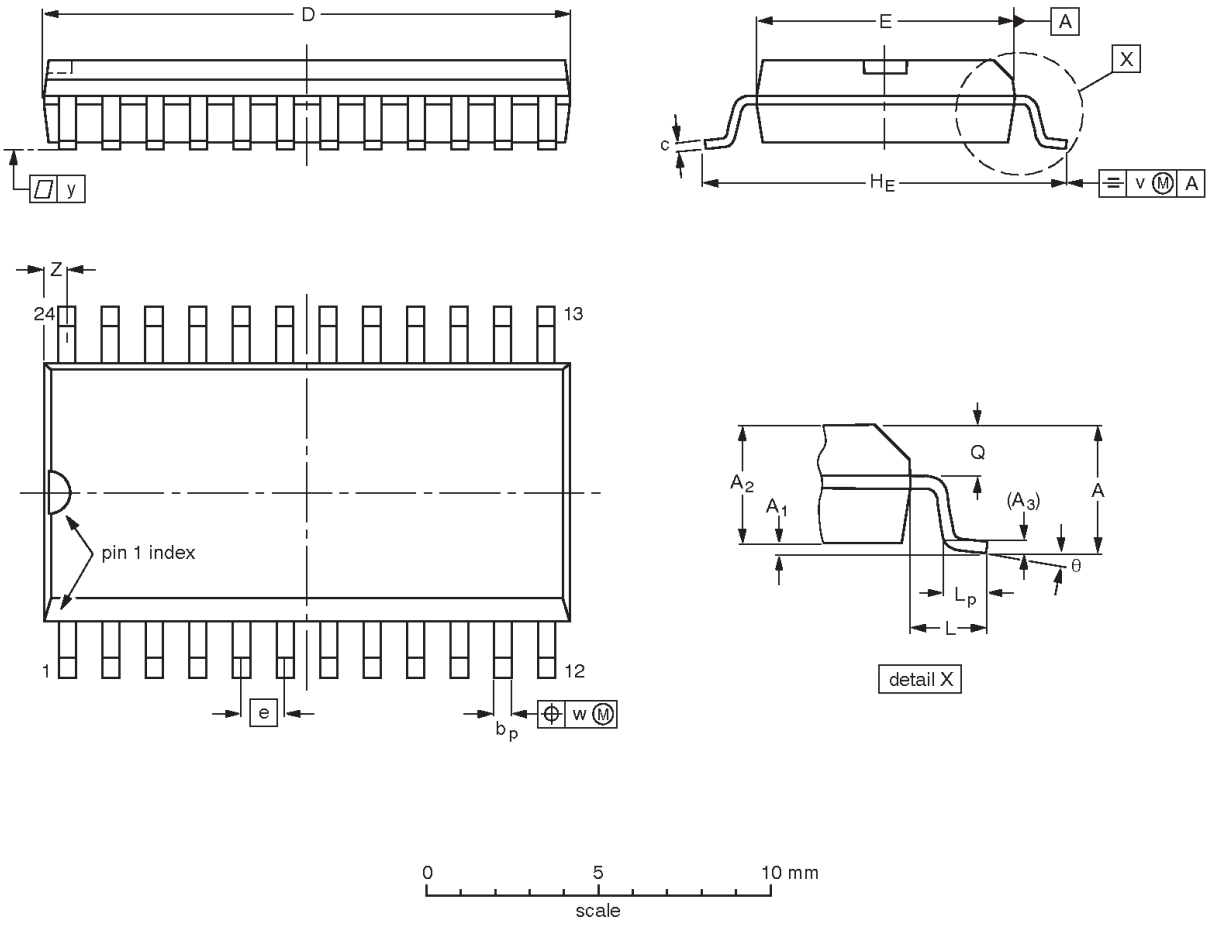
TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

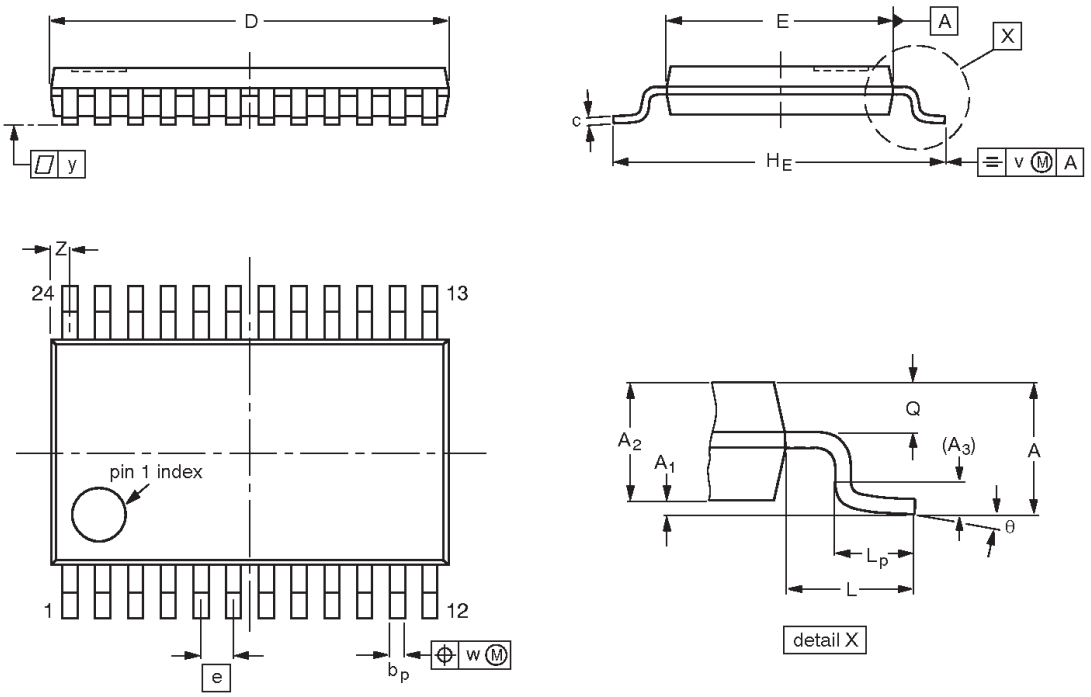
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20021213	**Product data (9397 750 10848); ECN 853-1613 29294 of 12 December 2002. Supersedes data of 08 June 1998 (9397 750 04022).** Modifications: ● Ordering information table: remove “North America” column; remove 74ABT648N and 74ABT648DB package offerings.
_2	19980608	**Product specification (9397 750 04022). ECN 853-1613 19516 of 08 June 1998. Supersedes data of 17 April 1995.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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