SONY CX20116/CXA1066K

8 bit, 100 MHz Flash A/D Converter

Description

The CX20116/CXA1066K are the 8 bit ultra high speed A/D Converter IC capable of digitizing analog signals at rates from DC to 110 MSPS. These A/Ds can be utilized in many varied applications. A wide analog input band width satisfies the characteristics for high definition television systems.

Features

- Resolution at 8 bit ±½ LSB
- Ultla high speed operation with maximum conversion rate of 110 MSPS
- Full scale input band width of: 60 MHz (−1dB)
  90 MHz (−3dB)
- Low input capacitance at 35 pF (Typ.)
- Low power consumption at 1.2W (Typ.)

Structure

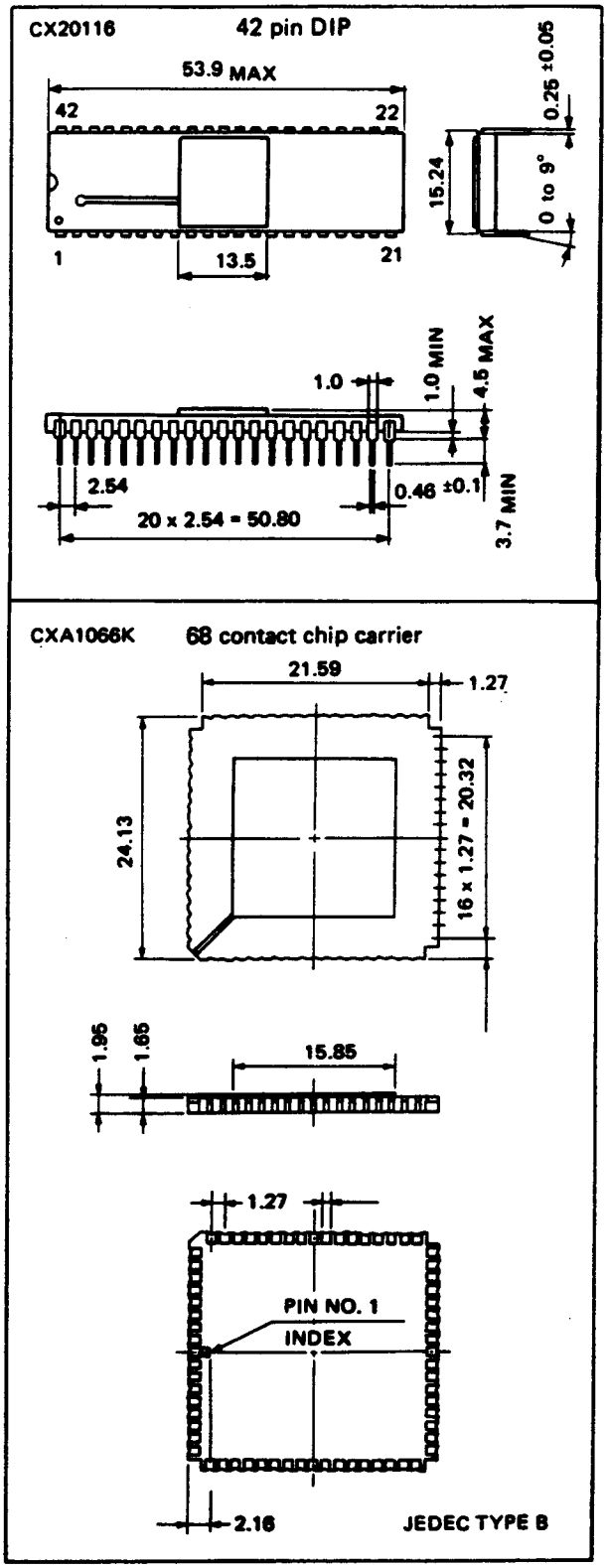
Bipolar silicon monolithic IC

Applicatipns

- High speed signal processing
- High definition video system

Package Outline

Unit: mm



50496A-ST

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}		0 to −7	V
• Analog input voltage	V_{IN}		0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}		0.5 to V_{EE}	V
	$\lvert V_{RT}-V_{RB}\rvert$		2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV		0.5 to −4	V
• V_{RM} pin input current	IVRM		−3 to +3	mA
• Digital output current	I_{D0} to I_{D7}		0 to −10	mA
• Operating temperature	Ta	CX20116	−25 to +100	°C
	Tc	CXA1066K	−25 to +125	°C*1
• Storage temperature	Tstg		−55 to +150	°C
• Allowable power dissipation	P_D	CX20116	3.1	W
		CXA1066K	2.3	W

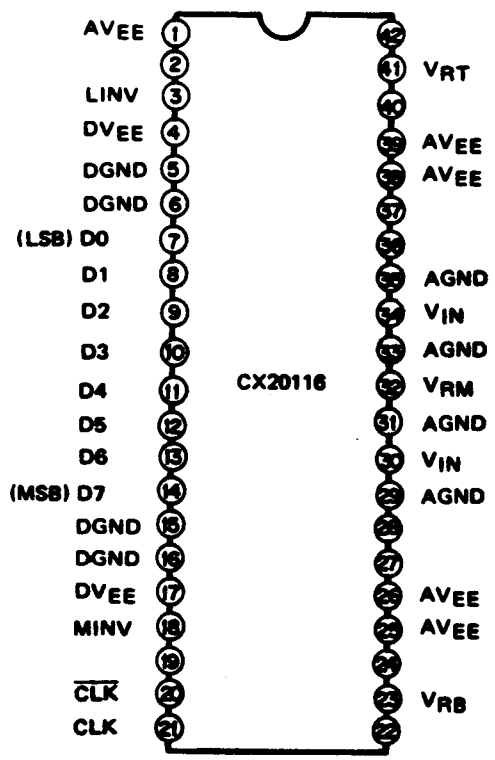
*1 Heat sinking is required above 54°C ambient.

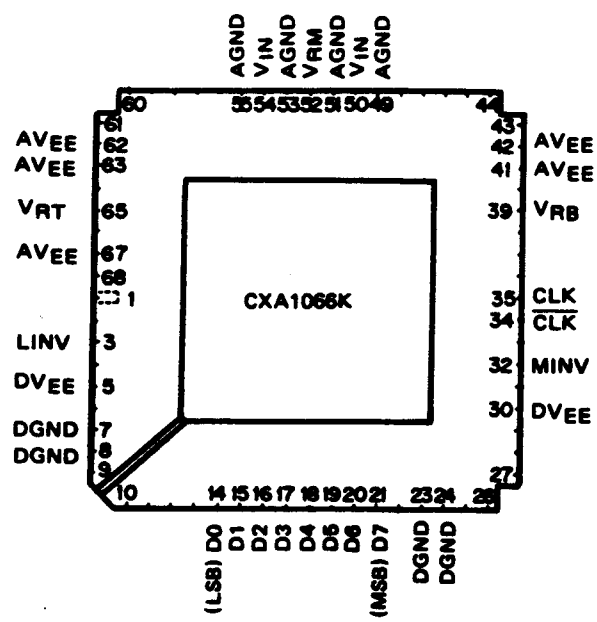
Recommended Operating Conditions

		Min	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}—DV_{EE}	−0.05	0	0.05	V
	AGND—DGND	−0.05	0	0.05	V
• Reference input voltege	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	7.5			ns
	Tpw0	2.5			ns

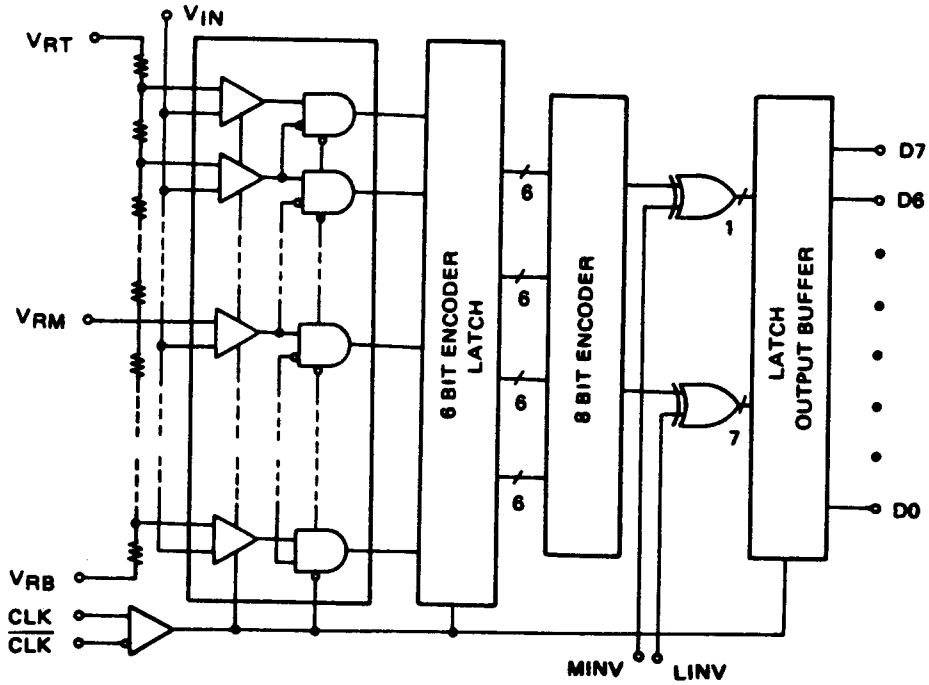
Pin Configuration (Top View)

The pin numbers without indication are empty pins. (not connected)





Block Diagram



Pin Description

No.		Symbol	Function
CX20116	CXA1066K		
1, 25, 26, 38, 39	41, 42, 62, 63, 67	AVEE	Analog VEE, −5.2V (Typ.). Coupled with about 6Ω between DVEE.
3	3	LINV	Input pin for output polarity inversion of D0 (LSB) to D6. (See the Code Table)
4, 17	5, 30	DVEE	Digital VEE, −5.2V (Typ.).
5, 6, 15, 16	7, 8, 23, 24	DGND	Digital GND, which is separated from the Analog GND.
7 to 14	14 to 21	D0 to D7	Digital data output pin, ECL level. D0: LSB to D7: MSB. Pull-down resistors are necessary externally.
18	32	MINV	Input pin for output polarity inversion of D7 (MSB) (See the Code Table). ECL level. "0" level is held when it is released.
20	34	$\overline{CLK}$	Inverse clock input pin, ECL level.
21	35	CLK	Clock input pin, ECL level.
23	39	VRB	Reference voltage (bottom), −2V (Typ.).
29, 31, 33,35	49, 51, 53, 55	AGND	Analog GND
30, 34	50, 54	VIN	Analog input, input voltage range is VRT to VRB
32	52	VRM	Middle point of the reference voltage, it can be used as a linearity correction pin.
41	65	VRT	Reference voltage (Top), 0V (Typ.).
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	1, 2, 4, 6, 9 to 13, 22, 25 to 29, 31, 33, 36 to 38, 40, 43 to 48 56 to 61, 64, 66, 68		Empty pins (not connected), 2 and 19 are used to be grounded to DGND, the others are used to be grounded to AGND.

Electrical Characteristics

(T_a=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

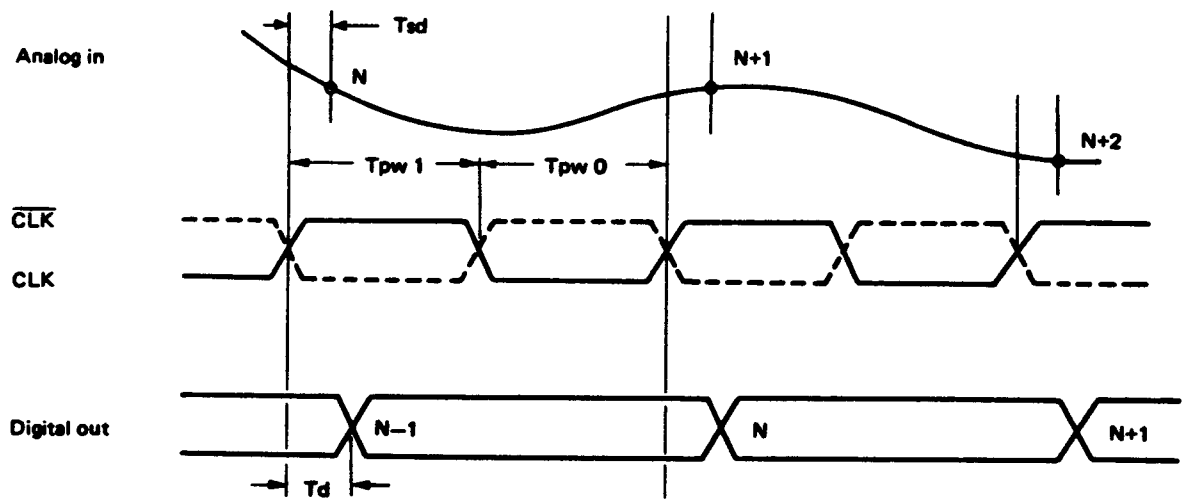
Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN}=0 to −2V, fin=1 kHz, ramp	110			MSPS
Supply current		I_{EE}		−180	−220	−260	mA
Analog input capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog input bias current		I_{IN}	V_{IN}=−1V		150	220	μA
Reference resistor		Rr (V_{RT} to V_{RB})		70	80	100	Ω
Offset voltage	V_{RT}			14	17	20	mV
	V_{RB}			6	9	12	mV
Digital input voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital input current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital output voltage		V_{OH}	R_L=620Ω to V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output data delay		Td	R_L=620Ω to V_{EE}	3.0	3.5	4.2	ns
Non-linearity error			Fc=110 MSPS			±½	LSB
Differential non-linearity error			Fc=35 MSPS			±½	LSB
Differential gain		DG	NTSC 40 IRE mod. ramp, Fc=110 MSPS			1.5	%
Differential phase		DP				0.5	deg.
Aperture jitter		Taj			15		ps
Sampling delay		Tsd		1.9	2.2	2.5	ns

Output Coding

	MINV LINV	0 0	0 1	1 0	1 1
	0V	111...11	100...00	011...11	000...00
	.	111...10	100...01	011...10	000...01
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
V_{IN}	.	100...00	111...11	000...00	011...11
	.	011...11	000...00	111...11	100...00
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	.	000...01	011...10	100...01	111...10
	−2V	000...00	011...11	100...00	111...11

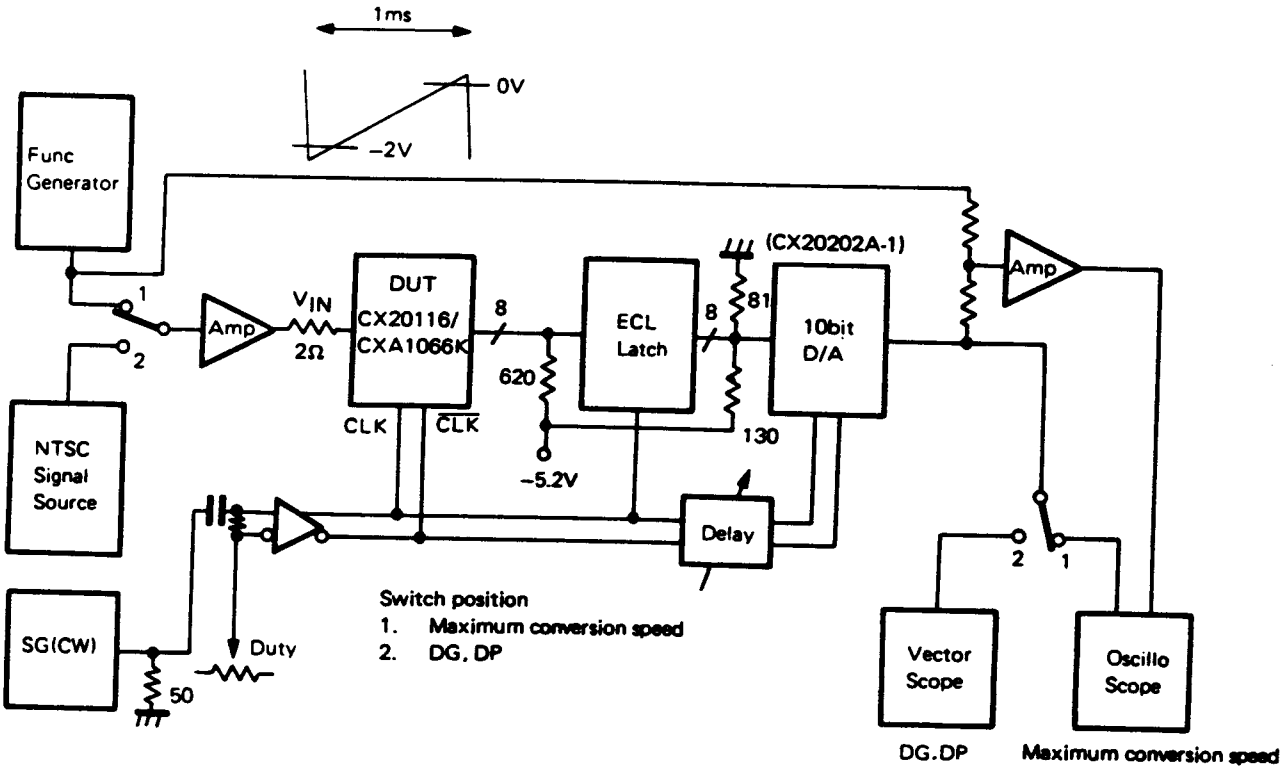
1: V_{IH}, V_{OH}
0: V_{IL}, V_{OL}

Timing Chart

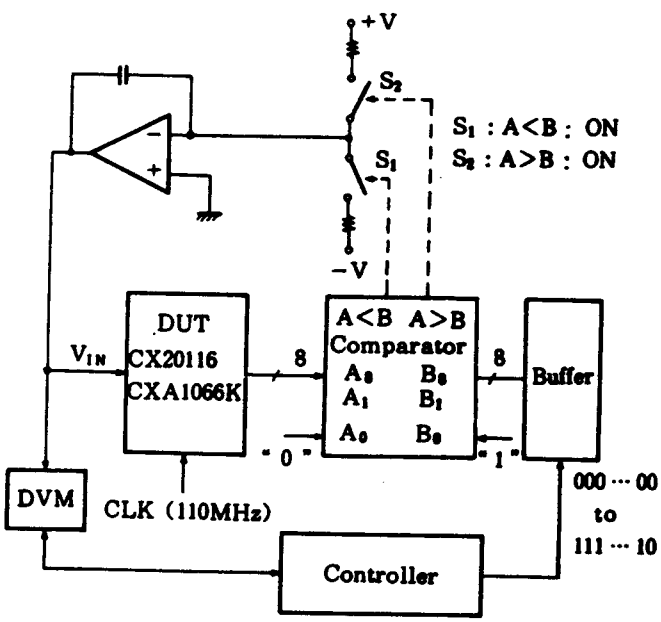


Electrical Characteristics Test Circuit

Maximum conversion speed test circuit
Differential gain error test circuit
Differential phase error test circuit

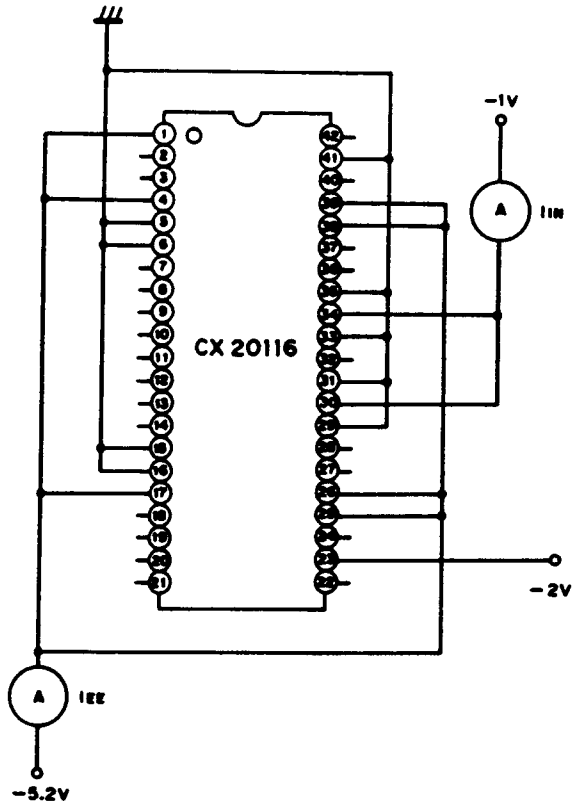


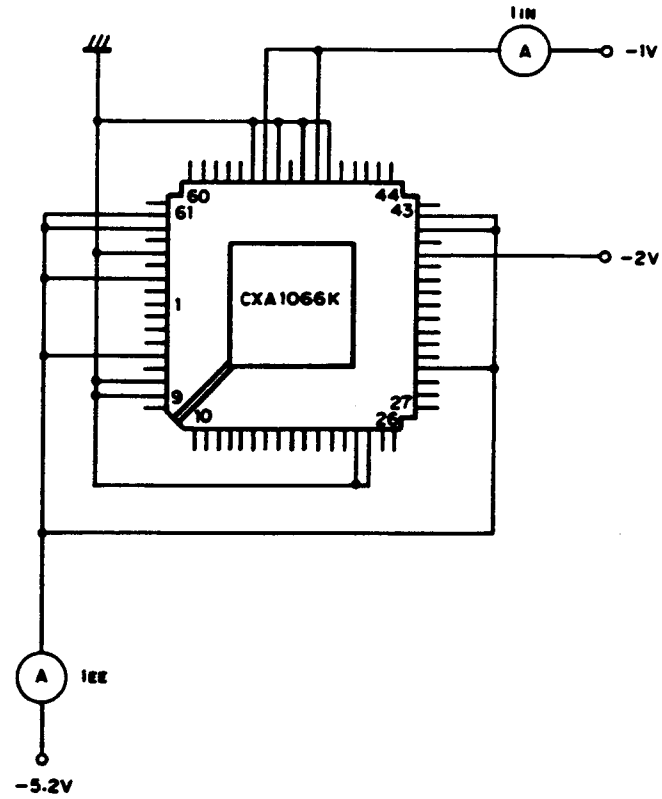
Differential Non-linearity Test Circuit



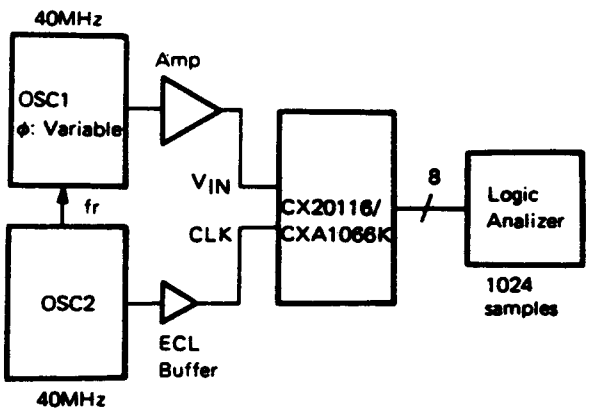
Power Supply Current Test Circuit

Analog input bias current test circuit

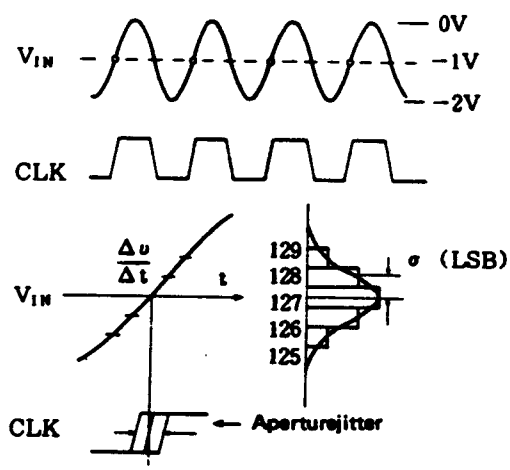




Sampling Delay Test Circuit
Aperture jitter test circuit



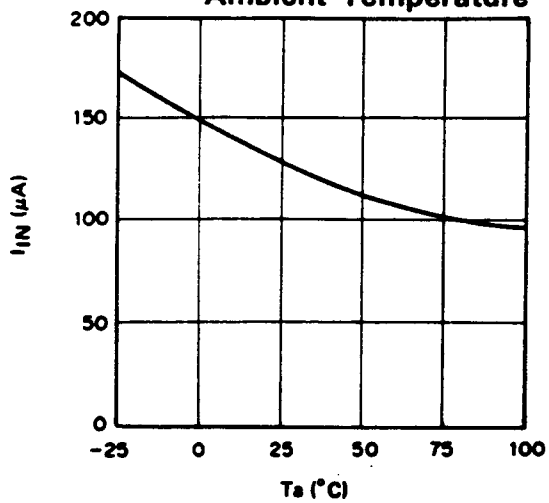
Aperture jitter test method



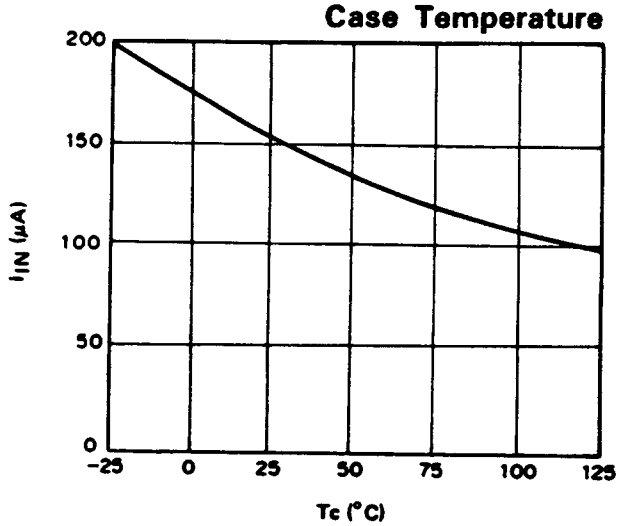
If the output distribution code is σ (LSB), when the maximum slew rate point is sampled at the analog input signal and the equivalent frequency clock, the aperture jitter Taj becomes:

$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / (\frac{256}{2} \times 2\pi f)$$

CX20116
Input Bias Current vs. Ambient Temperature



CXA1066K
Input Bias Current vs. Case Temperature



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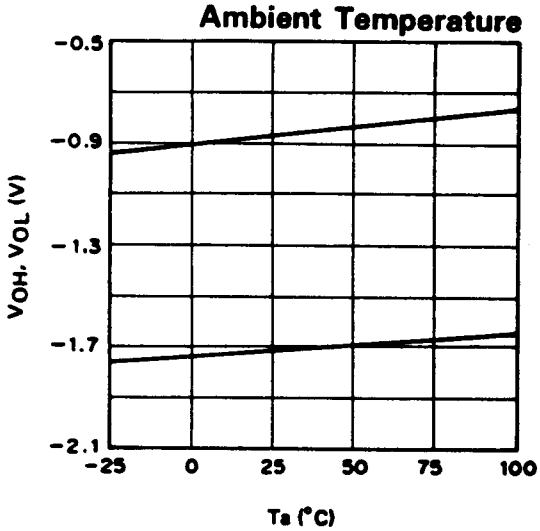
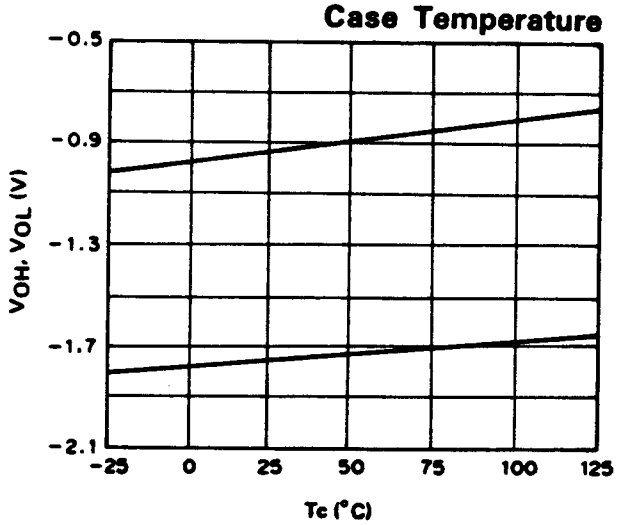
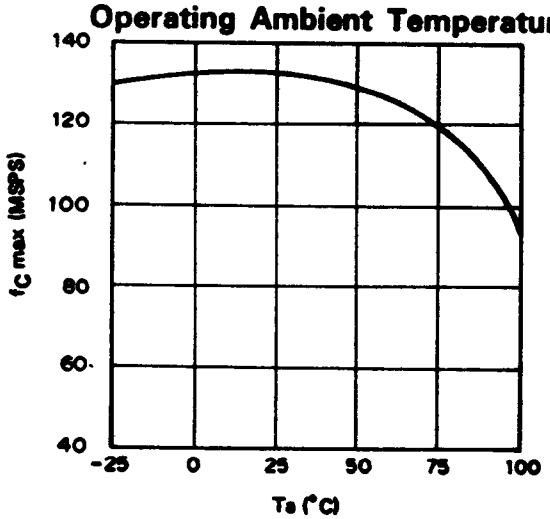
Digital Output Voltage vs. Ambient Temperature



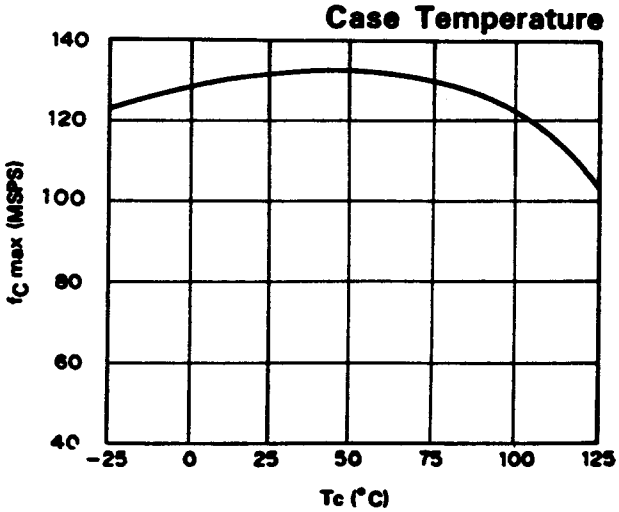
CXA1066K
Digital Output Voltage vs. Case Temperature



CX20116
Maximum Conversion Rate vs. Operating Ambient Temperature



CXA1066K
Maximum Conversion Rate vs. Case Temperature



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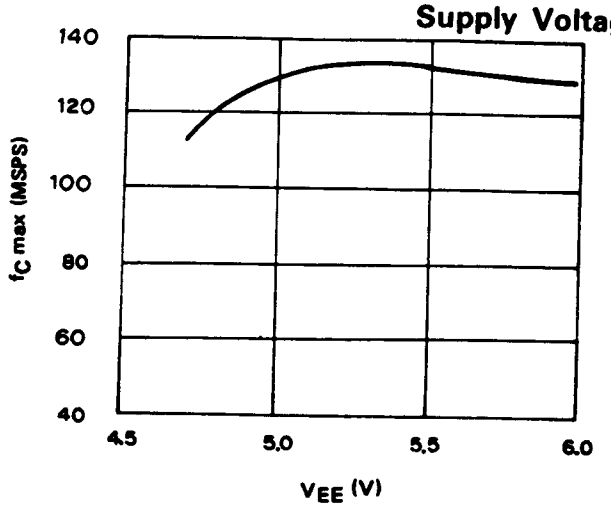
Maximum Conversion Frequency vs. Supply Voltage



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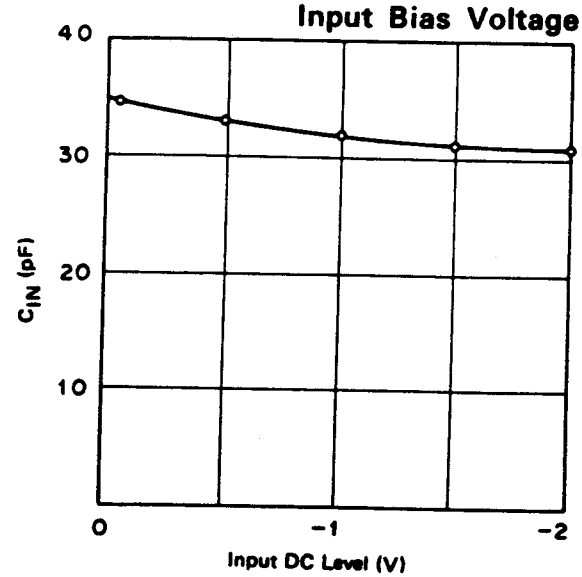
Analog Input Capacitance vs. Input Bias Voltage



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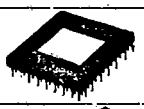
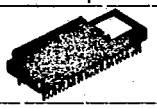
Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic