HD153035F
56-Mbps Data Channel Processor

HITACHI

Under Development

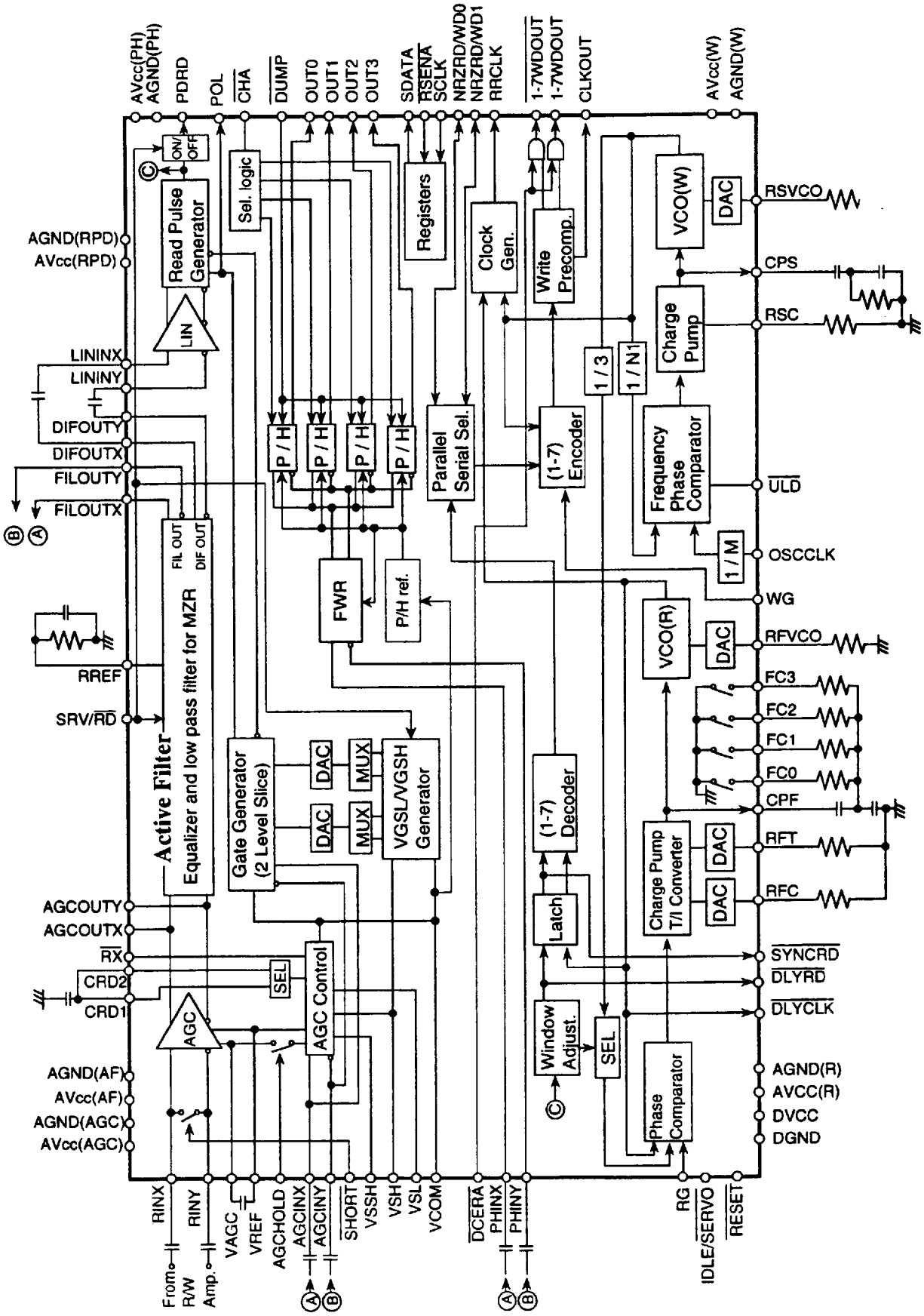
Description

The HD153035F is a 56 Mbps 1-7 ENDEC data separator with built-in read pulse detector, active filter, frequency synthesizer and synchronizer developed for use in magnetic disk drives. In read mode the HD153035F decords the read wave form output from the read/write amplifier into an NRZ signal. In write mode it encodes the NRZ signal output from the controller into a 1-7 RLL code.

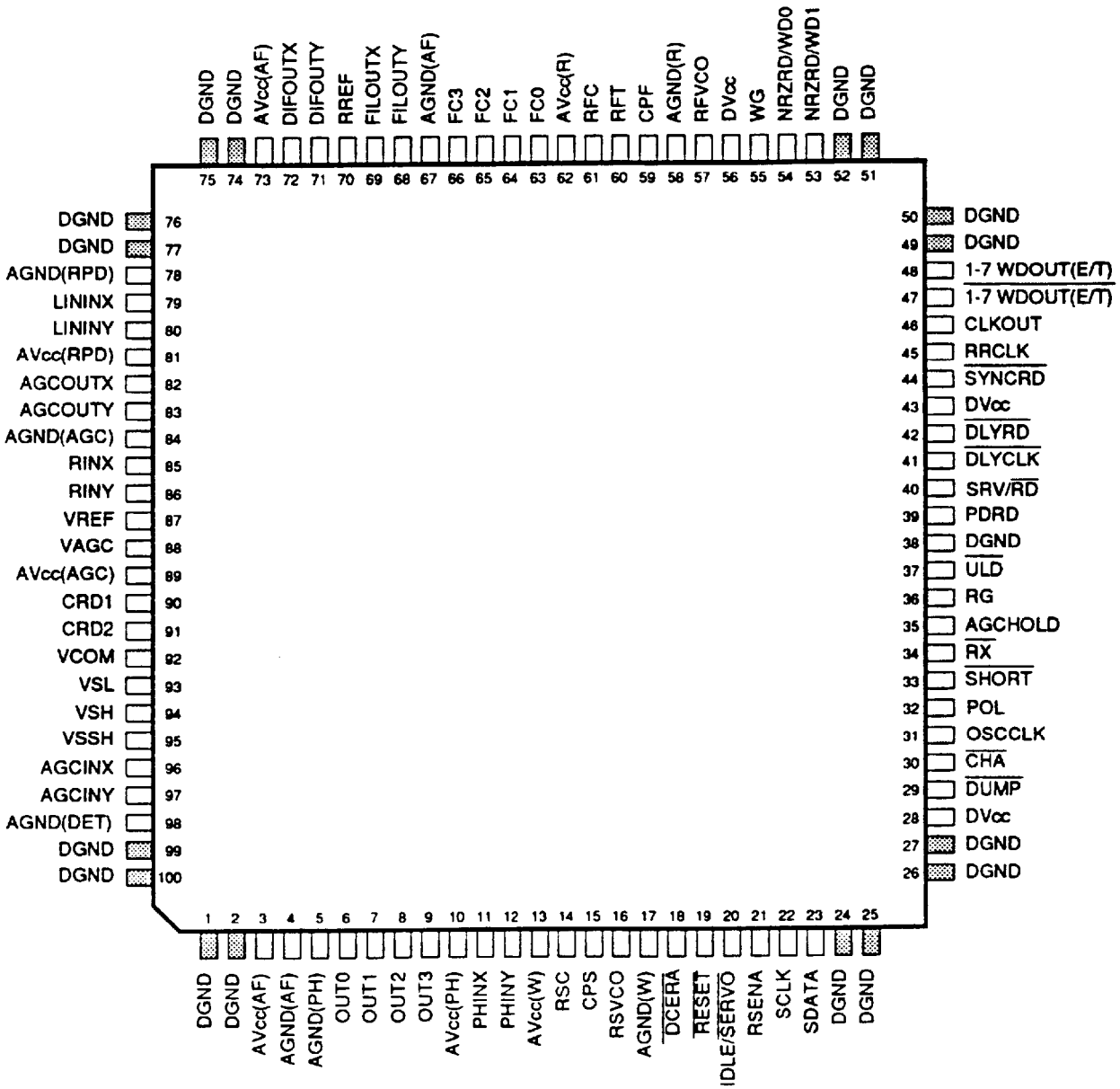
Features

- Maximum NRZ data transfer rate : 56Mbps.
- Data transfer clock frequency : 1.5 data transfer rate (84MHz maximum).
- Settings are micro-computer programmable.
- On-chip frequency synthesizer generates encode clock for writing (1% steps at f_{MAX}/f_{MIN}=2.55).
- Programmable window centering adjustment and window monitoring functions.
- User-selectable single zone recording or multiple zone recording options. The following are programmable for multiple zone recording : VCO center frequency (192 settings), loop Filter constant (2 settings), charge pump current levels (8 settings), T/I converter output current (8 settings), active filter cutoff frequency for servo and data modes (128 settings).
- Dual-mode phase detector compares both phase and frequency to ensure a wide capture range.
- Separate active filter 7-bit programmable cut-off frequencies.
- Two sets of 4-bit High and Low slice levels for reliable pulse detection .
- 1-7WDOUT outputs are selectable differential pseudo-ECL or TTL pair for high speed transfer without timing error.
- High-speed acquisition can be accomplished with highly stable reproduction by switching between normal-gain and high-gain modes, and by switching loop filter constants.
- VCO oscillation timing capacitor is built in for better noise immunity.
- PLL characteristic frequency and damping rate are defined without 2T-8T (1-7RLL) signal cycle.
- Built-in AGC amplifier for stable reproduction despite varying media and head characteristics.
- Gate generator eliminates incorrect read pulse problems that occur with time-domain filtering with appropriate slice-level setting.
- Head resolution can be increased without incorrect read pulse worries.
- AGC amplifier gain can be set to zero during writing.
- Built-in write phase compensation function with programmable delay time.
- Early or Late write pre-compensation amounts can be programmed independently.
- Built-in active filter with 7-bit programmable cut-off frequency.
- High speed data transfer inputs and outputs are done via complementary TTL output pairs.
- Hi-BiCMOS process achieves high speed with low power dissipation .
- Idle mode and power down functions.
- QFP-100 pin package suitable for compact surface mounting (resin size : 14mm x 14mm)
- Required only a single 5V supply.

2. Block diagram



3. Pin arrangement



(Top view)

4. Pin Functions

Pin Name	Pin No.	Type	Function
RG (Read gate)	36	In	High level at the input selects read mode. This signal switches the clock for counters and internal circuits, and begins phase synchronization of the decode clock generator's VFO with the 1-7 decode data.
PHINX PHINY	11 12	In	Differential inputs for the servo Peak/Hold circuit.
$\overline{\text{RESET}}$	19	In	Low input initializes internal circuits. Drive this line low at power-up. Low input also locks the two built-in VCOs to their center frequencies. Keep this line high during normal operation.
OSCCLK (Oscillator clock)	31	In	Clock synthesizer's reference clock input. The frequency synthesizer generates encode clock frequencies from the input on this line. Data writing is synchronized with the encode clock. When not reading data, the decode clock generator's VFO is also synchronized with frequency 1.5 times the data transfer rate.
$\overline{\text{1-7WDOUT}}$ 1-7WDOUT (Write Data outputs)	48 47	Out	1-7 RLL Write Data Differential Output. Pseudo ECL/TTL are available by bit 6 of register"$hD". When this bit is "H", these outputs are TTL. When this bit is "L", these outputs are ECL.These Pin provide the 1-7WDOUT write data that goes to the Read/Write amplifier after the write pre-compensation. When WG goes high, 1-7WDOUT pin are output mode.
CLKOUT	46	Out	This clock is for the external write pre-compensation in the Write mode. This clock(TTL level) is synchronized with 1-7WD.
$\overline{\text{ULD}}$ (Unlock detect)	37	Out	Error output from the encode clock generator's frequency synthesizer. ULD goes low to indicate that the PLL in the encode clock generator's frequency synthesizer has lost lock. The disk controller should immediately halt the write operation. Data must be written again from the beginning.
RSVCO	16	External component required	Connect a resistor to set the center frequency of the VCO in the encode clock generator's frequency synthesizer.
CPS	15	External component required	Current output to an external loop filter.
RSC	14	External component required	Connect a resistor to set the charge pump output current for the encode clock generator's frequency synthesizer.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
RFC	61	External component required	Connect a resistor to set the charge pump output current for the decode clock generator's VFO. The charge pump current level is set by GAC[5:3] and CPO[4:0] registers.
RFT	60	External component required	Connect a resistor to set the T/I converter's sampling feedback gain to 1(nominal). The T/I converter's output current is determined by this resistor, and registers VFC[4:0] & GAC[2:0] & TIO[4:0].
CPF	59	External component required	Current output to the external loop filter.
RREF	70	External component required	Connect to a resistor to set the reference current for the Active Filter's DAC.
FC0 FC1 FC2 FC3	63 64 65 66	External component required	Connect to a loop filter resistor to set the attenuation ζ of the PLL. Each line is grounded through an MOS switch is selected by PLL gain mode and bit 6 of register GAC.

Bit 6 of register GAC	PLL gain mode	Pin			
		FC0	FC1	FC2	FC3
"0"	High	ON	ON	OFF	OFF
	Normal	ON	OFF	OFF	OFF
"1"	High	OFF	OFF	ON	ON
	Normal	OFF	OFF	ON	OFF

RFVCO	57	External component required	Connect to a resistor to set the center frequency of the VCO in the decode clock generator's VFO.
SRV/$\overline{RD}$	40	Input	"H":Servo Mode,"L":Read Mode. In the servo mode ,"CFCB" register set the A/F's cutoff frequency and VGSLB register set the gate slice low level. In the read mode ,"CFCA" register set the A/F's cutoff frequency and VGSLA register set the gate slice level.
RINX RINY	85 86	Differen-tial input	Differential input lines for the signal read from the recording medium.
LININX LININY	79 80	Differen-tial input	Differential input lines for the zero-crossing comparator. Normally connect to DIFOUTX/Y of the active filter with bypass capacitors.
AGCINX AGCINY	96 97	Differen-tial input	Differential input lines for the AGC output amplitude detector. Connect to FILOUTX/Y outputs of the AF with bypass capacitors.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$\overline{RX}$	34	In	TTL-level input that switches the AGC loop on or off. $\overline{RX}$ input: High → AGC loop on. $\overline{RX}$ input: Low → AGC loop off.
AGCHOLD	35	In	TTL-Level input that locks the AGC amplifier gain. When AGCHOLD goes High the gain is locked at its immediately preceding value.
AGCOUTX AGCOUTY	82 83	Differential output	Differential output lines for monitor from the AGC amplifier. The outputs are open-emitter type and would need ext. 1~10K pulldowns.
VREF	87	Monitor line	Monitor line for the AGC amplifier reference voltage.
VAGC	88	Monitor line	Monitor line for the AGC amplifier gain setting voltage.
PDRD	39	Out	Output line for the data read from disk as reshaped into digital data by the read pulse detector. When SRV/$\overline{RD}$(40Pin) goes high, PDRD outputs read data pulse. When SRV/$\overline{RD}$ goes low, PDRD is disenable mode.
VCOM	92	External component required	Reference voltage output line for the AGC output amplitude detector and the Gate generator.
VSL	93	External component requird	Voltage input line for seting the low slice level of AGC output amplitude detector. Corresponds to the discharge current threshold. Normally this level is set 67% of the VSH level.
VSH	94	External component required	Voltage input line for settiing the high slice level of the AGC output amplitude detector. Corresponds to the charge current threshold
VSSH	95	External component required	Voltage inputline for setting the fast attack(high gain) high slice voltage of the AGC output amplitude detector. Normally this level is set 160% of the VSH level.
IDLE/$\overline{SERVO}$	20	In	The input is used in combination with the two Mode bits in the PCN register to reduce power consumption in the Idle mode. When PCN= 00, device is in the R/W normal mode, all circuits are ON. When PCN = 11, device is in the Sleep mode, all circuits are OFF except the I/O and logic. When PCN = 10, then depending on the logic level of the IDLE/$\overline{SERVO}$ pin; if it is High, then chip is in the Idle mode and all circuits are OFF except for the I/O, logic, and the bias CKT's; if it is Low, then the device is in the Servo mode and the I/O, logic, bias CKT's, AGC, active filter, Read Pulse Detector, and Peak/Hold should be ON with only the RD PLL and the WR PLL being OFF.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
CRD1	90	External component required	In reading the normal data, the charge /discharge current output line for the AGCoutput amplitude detector. connected to 91PIN (CRD2)
CRD2	91	External component required	External capacitor is needed for AGC output amplitude detector.
FILOUTX FILOUTY	69 68	Differential output	Differential output line from Active Filter. Connect to AGCINX,Y and PHINX,Y through capacitors.
DIFOUTX DIFOUTY	72 71	Differential output	Differential output line from Active Filter. Connect to LININX,Y through capacitors.
$\overline{\text{SHORT}}$	33	In	When this terminal is 'L', RINX and RINY are shorted.
OUT0~ OUT3	6,7,8,9	External component required	Connect to external capacitors for servo peak/hold.
WG	55	In	Write gate signal input. Set this PIN high during writing
NRZRD/WD1	53	In/Out	I/O pin of NRZ signal. This pin is effective only in the case of parallel transferring. NRZ Data select bit 7 of register($h8) controls parallel/serial. (When this bit is " H" , NRZ mode is parallel)
NRZRD/WD0	54	In/Out	I/O pin ooof NRZ signal. In the serial transfer mode, only this pin is effective. NRZ Data select bit 7 of register($h8) controls parallel/serial. (When this bit is " L" , NRZ mode is serial)
SDATA	23	In/Out	Data is transmitted in 16-bit packet MSB first. The first 2 bits determine the read or write mode, the next bit is "Don't Care", the next 4 bits are for the register address, followed by 1 "Don't Care" bit, then the last 8 bits are for the Write or Read Data.
RSENA	21	In	This active low input selects the device and enables the serial port.
POL	32	Out	Output pin of the polarity signal for read signal from disk drive.
$\overline{\text{DCERA}}$	18	In	Input pin for the DC erase. When this pin is "L", 1-7WDOUT(pin#48) is "L" and $\overline{\text{1-7WDOUT}}$(pin#47) is "H".
$\overline{\text{CHA}}$	30	In	Input pin of the control signal of Peak/hold circuit(TTL level) Position signal is sampled by $\overline{\text{CHA}}$="L"
$\overline{\text{DUMP}}$	29	In	Input pin of the discharge control signal of Peak/Hold circuit. TTL level, $\overline{\text{DUMP}}$="L" is for discharge.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
SCLK	22	In	This is the serial clock sent in by the hard disk controller or other ASIC device. When the serial port is not enabled, this clock line should be driven low. For either read or write transfer, a 16 clock burst is required for proper operation. Data is latch in during write or sent out during read with the rising edge of the SCLK.
$\overline{\text{DLYCLK}}$	41	Out	Monitor pin(TTL level) for Window adjustment. This pin allows the VCO clock signal output by the PLL circuit to be monitored. Contact Hitachi,Ltd. for special instrustions if use of this function is required.
$\overline{\text{DLYRD}}$	42	Out	Monitor pin(TTL level) for Window adjustment. This pin allows the read data signal output from the window adjustment circuit to be monitored. Contact Hitachi,Ltd. for special instructions if use of this function is required.
$\overline{\text{SYNCRD}}$	44	Out	Monitor pin(TTL level) for Window adjustment. This pin outputs the read data outputs the read data input to the PLL block latched by the VCO clock. Contact Hitachi,Ltd. for the special instructions if use of this function is required.
RRCLK	45	Out	Read refernce clock output(TTL level). At read time,this pin provides a clock which is synchronized with the converted NRZRD signal. This controller should read NRZRD by this clock. Other than read, reefernce clock is provided to disk controller.
DGND	1, 2, 24,25,26, 27, 38, 49, 50, 51, 52, 74, 75, 76, 77, 99,100	Ground	Digital ground.
DVcc	28, 43, 56	Power	Digital Vcc power supply.
AVcc(PH)	10	Power	Analog Vcc power supply for peak hold.
AGND(PH)	5	Ground	Analog ground for peak hold.
AVcc(W)	13	Power	Analog Vcc power supply for synthesizer.
AGND(W)	17	Ground	Analog ground for synthesizer.
AVcc(R)	62	Power	Analog Vcc power supply for synchronizer.
AGND(R)	58	Ground	Analog ground for synchronizer.
AVcc(AF)	3, 73	Power	Analog Vcc power supply for active filter.
AGND(AF)	4, 67	Ground	Analog ground for active filter.
AVcc(AGC)	89	Power	Analog Vcc power supply for AGC.
AGND(AGC)	84	Ground	Analog ground for AGC.
AVcc(RPD)	81	Power	Analog Vcc power supply for read pulse detector.
AGND(RPD)	78	Ground	Analog ground for read pulse detector.
AGND(DET)	98	Ground	Analog ground for AGC control circuit

5. Registers

The HD153035F has 16 address's 8 bits-register that control the center frequency of the decode clock generator's VFO and the frequency of the encode clock generator's frequency synthesizer, control the synthesizer's gain, control the read data pulse width and its polarity, control the synchronizer's gain and offset, adjust the decode window, apply the early/late write precompensation, control the prescaling value, adjust the active filter's cut-off frequency, and controls various functions.

Address register value (MSB LSB)	Name	Abbreviation
0 0 0 0	VCO center frequency control register	VFC register
0 0 0 1	RD-PLL Gain control register Synthesizer operating mode control bit	GAC register SPSYNT bit
0 0 1 0	RD-PLL Charge Pump offset control register Write precompensation delay control register (L)	CPO register WPL register
0 0 1 1	RD-PLL T/I offset control register Write precompensation delay control register (S)	TIO register WPS register
0 1 0 0	Window adjustment register (0.85ns typ. /step) Window fine adjustment register(0.25ns typ. /step)	WAJ register WFA register
0 1 0 1	AGC Mode control bit (FAST / SLOW) Read data (PDRD) polarity control register Read data (PDRD) pulse width control register WR-PLL Gain control register	AGS bit RDSEL register PW register SGC register
0 1 1 0	Prescaler of WR-PLLcontrol register	PSC register
0 1 1 1	AF cut-off frequency control register(for Read)	CFCA register
1 0 0 0	NRZ Data 1bit - serial / 2bits parallel select bit AF cut-off frequency control register(for Servo)	NRZM bit CFCB
1 0 0 1	Unlock detect gain control register (for WR-PLL) Boost level control register	ULD register BLC register
1 0 1 0	Boost enable bit at servo mode High pass filter cut-off frequency control register(for Read)	SRVBE bit HPCA register
1 0 1 1	High pass filter cut-off frequency control register(for Servo)	HPCB register
1 1 0 0	Gate generator's High-slice level control register(for Read) Gate generator's Low-slice level control register(for Read)	VSGHA register VSGLA register
1 1 0 1	1-7 WDOUT output type control bit (ECL / TTL) Write precompensation delay control register (E) Write precompensation delay control register (N)	WDT bit WPE register WPN register
1 1 1 0	AGCOUT enable control bit Power management control register Gate generator's Low-slice level control register(forServo)	AOE bit PCN register VSGLB register
1 1 1 1	Test Mode control register	MDC register

6. Register Descriptions

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Register Functions
0 0 0 0	VFC7	VFC6	VFC5	VFC4	VFC3	VFC2	VFC1	VFC0	VFC: controls the center frequency of the WR-PLL & RD-PLL.
0 0 0 1	SPSYNT	RFCA	GAC5	GAC4	GAC3	GAC2	GAC1	GAC0	GAC: controls the RD-PLL's T/I and Charge Pump gain. SPSYNT: controls the WR-PLL's operating mode
0 0 1 0	WPL2	WPL1	WPL0	CPO4	CPO3	CPO2	CPO1	CPO0	CPO: controls the Off-Set of the RD-PLL's Charge Pump circuit. WPLL: sets the write precompensation delays. (L)
0 0 1 1	WPS2	WPS1	WPS0	TIO4	TIO3	TIO2	TIO1	TIO0	TIO: controls the Off-Set of the RD-PLL's T/I converter. WPLS: sets the write precompensation delays. (S)
0 1 0 0	WFA2	WFA1	WFA0	WAJ4	WAJ3	WAJ2	WAJ1	WAJ0	WFA: fine adjusts data window. WAJ: adjusts data window.
0 1 0 1	AGCSEL	RDSEL1	RDSEL0	PW1	PW0	SGC2	SGC1	SGC0	AGCSEL: sets AGC mode Fast or Slow. RDSEL: controls PDRD pulse polarity PW: controls PDRD pulse width. SGC: sets the WR-PLL gain.
0 1 1 0	0	PSC6	PSC5	PSC4	PSC3	PSC2	PSC1	PSC0	PSC: sets the WR-PLL prescaler's counter value.
0 1 1 1	0	CFCA6	CFCA5	CFCA4	CFCA3	CFCA2	CFCA1	CFCA0	CFCA: controls Read Mode Active Filter's Cut-Off frequency.
1 0 0 0	NRZM	CFCB6	CFCB5	CFCB4	CFCB3	CFCB2	CFCB1	CFCB0	NRZM: selects 1bit or 2bits NRZ data CFCB: controls Servo Mode Active Filter's Cut-Off frequency.
1 0 0 1	TSTBF	ULD1	ULD0	BLC4	BLC3	BLC2	BLC1	BLC0	ULD: sets unlock detect period. BLC: controls AF's Boost level
1 0 1 0	SRVBE	0	0	HPCA4	HPCA3	HPCA2	HPCA1	HPCA0	SRVBE: controls filter boost on / off (at servo mode) HPCA: controls high-pass filter cut-off frequency(for Read)
1 0 1 1	0	0	0	HPCB4	HPCB3	HPCB2	HPCB1	HPCB0	HPCB: controls high-pass filter cut-off frequency(for Servo)
1 1 0 0	VGSHA3	VGSHA2	VGSHA1	VGSHA0	VGSLA3	VGSLA2	VGSLA1	VGSLA0	VGSHA: sets high-slice level of the gate generator(for Read) VGSLA: sets low-slice level of the gate generator(for read)
1 1 0 1	0	WDM	WPN2	WPN1	WPN0	WPE2	WPE1	WPE0	WDM: selects output type of 1-7 WDOUT (TTL / pseudo ECL) WPE / WPN: sets the write precompensation delays. (E/N)
1 1 1 0	AOE	0	PCN1	PCN0	VGSLB3	VGSLB2	VGSLB1	VGSLB0	AOE: AGCOUTX/Y outputs enable control PCN: power saving control register for the analog modules. VGSLB: sets low-slice level of the gate generator(for Servo)
1 1 1 1	TEST	0	MDC5	MDC4	MDC3	MDC2	MDC1	MDC0	MDC: TEST mode control register.

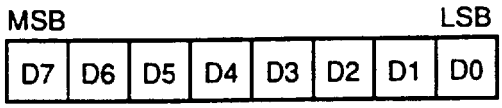
[redacted] are set to "1" during reset time.

Register Descriptions (cont)

VCO Center Frequency Control register (VFC)

Address (at write = "C0" hex), Address (at read = "80" hex),

VFC Register



VFC register is 8 bits long.
This register is used in multiple-zone recording to set the center frequency of the decode clock generator's VCO, the T/I converter's reference current, and the oscillation frequency of the encode clock generator's frequency synthesizer. Bit D7 is cleared when reset pin is asserted.

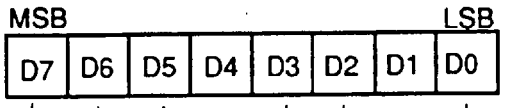
Resistors connected to the RFVCO and RSVCO lines set these values for the minimum data transfer rate. The VFC register raises these values in step of 1.56%, permitting 192 settings up to a maximum transfer rate 3.98 times of the minimum rate.

0 1 0 0 0 0 0 0 Minimum transfer rate (reference rate)

1 1 1 1 1 1 1 1 Maximum transfer rate (3.98 times speed)

Gain Control Register (GAC) = RFCA, GAC[5:0] for Read PLL synchronizer

Address (at write = "C2" hex), Address (at read = "82" hex)



GAC[2:0]

Bits 2 to 0: Select the output current of the T/I converter to vary the gain. Eight gain settings are possible.

0 0 0 Minimum gain (L=0)

1 1 1 Maximum gain (L=7)

GAC[5:3]

Bits 5 to 3: Select the output current of the Charge pump to vary the gain. Eight gain settings are possible.

0 0 0 Minimum gain (P=1)

1 1 1 Maximum gain (P=8)

RFCA

Bit 6 selects the resistors that determine the attenuation ξ of the loop filter for the decode clock generator's VFO.

Bit 6 = 0: resistors connected to the FC0 and FC1 are selected

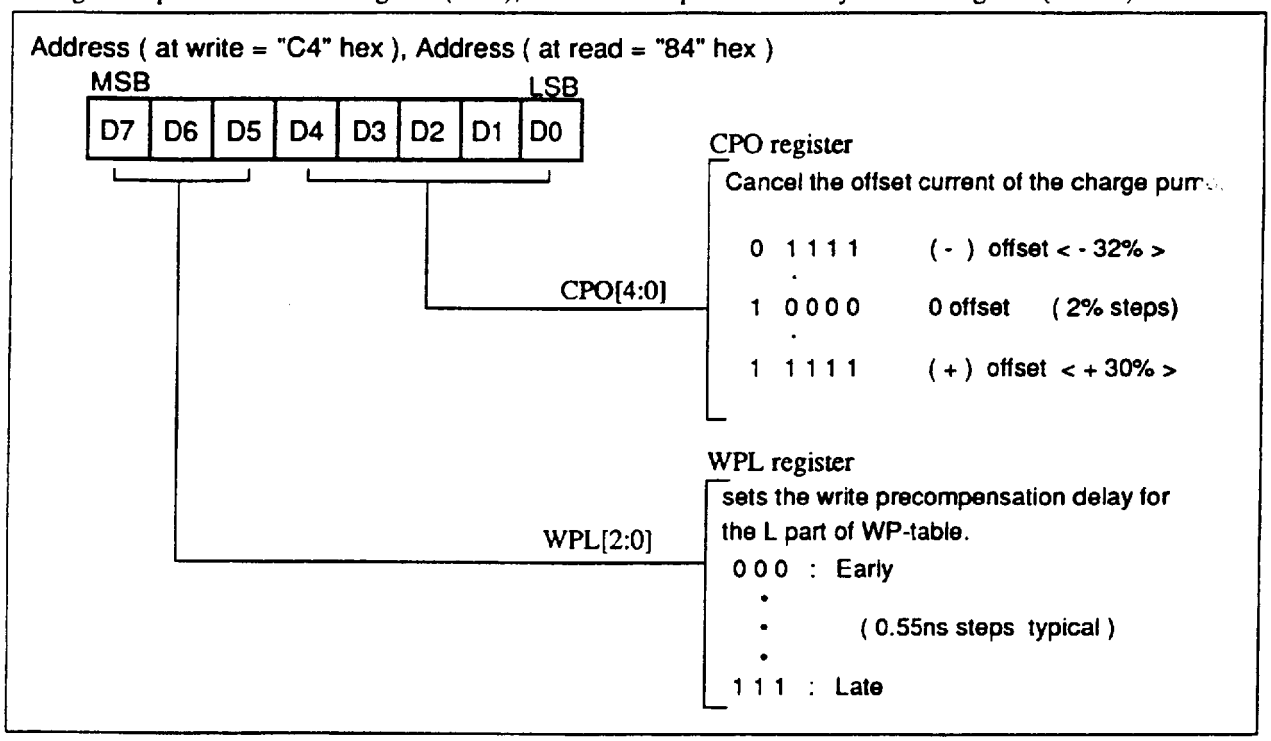
Bit 6 = 1: resistors connected to the FC2 and FC3 are selected

Synthesizer operating mode control bit

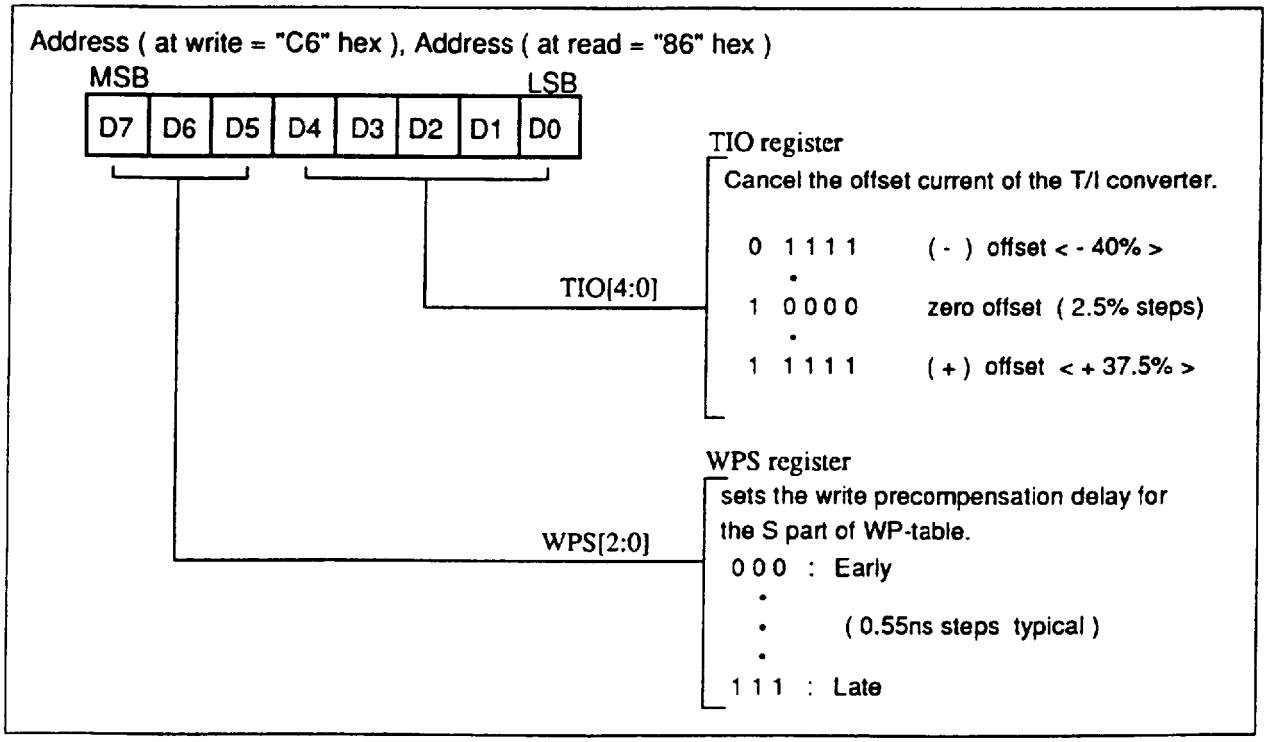
0 : 56Mbps mode
1 : 50Mbps mode

Register Descriptions (cont)

Charge Pump Offset Control Register (CPO), Write Precompensation delay control Register (WPLL)



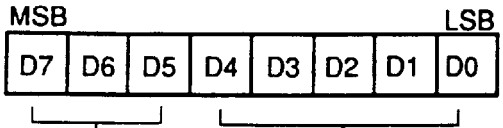
T/I Offset Control Register (TIO) , Write Precompensation delay control Register (WPLS)



Register Descriptions (cont)

Window Finc Adjust Register WFA[2:0] and Window Adjust Register WAJ[4:0]

Address (at write = "C8" hex), Address (at read = "88" hex)



WAJ register

WAJ[4:0]

This register adjusts the setting of the window. Window centering can be adjusted to 32 positions by an on-chip delay line. Bit D4 will always be cleared during reset. The microcontroller can center the window automatically with firmware by changing these values.

0 0000
·
·
(-) negative delay adjustment
0 1111
1 0000 Center (0.67ns steps typical)
1 0001
·
(+) positive delay adjustment
·
1 1111

WFA register

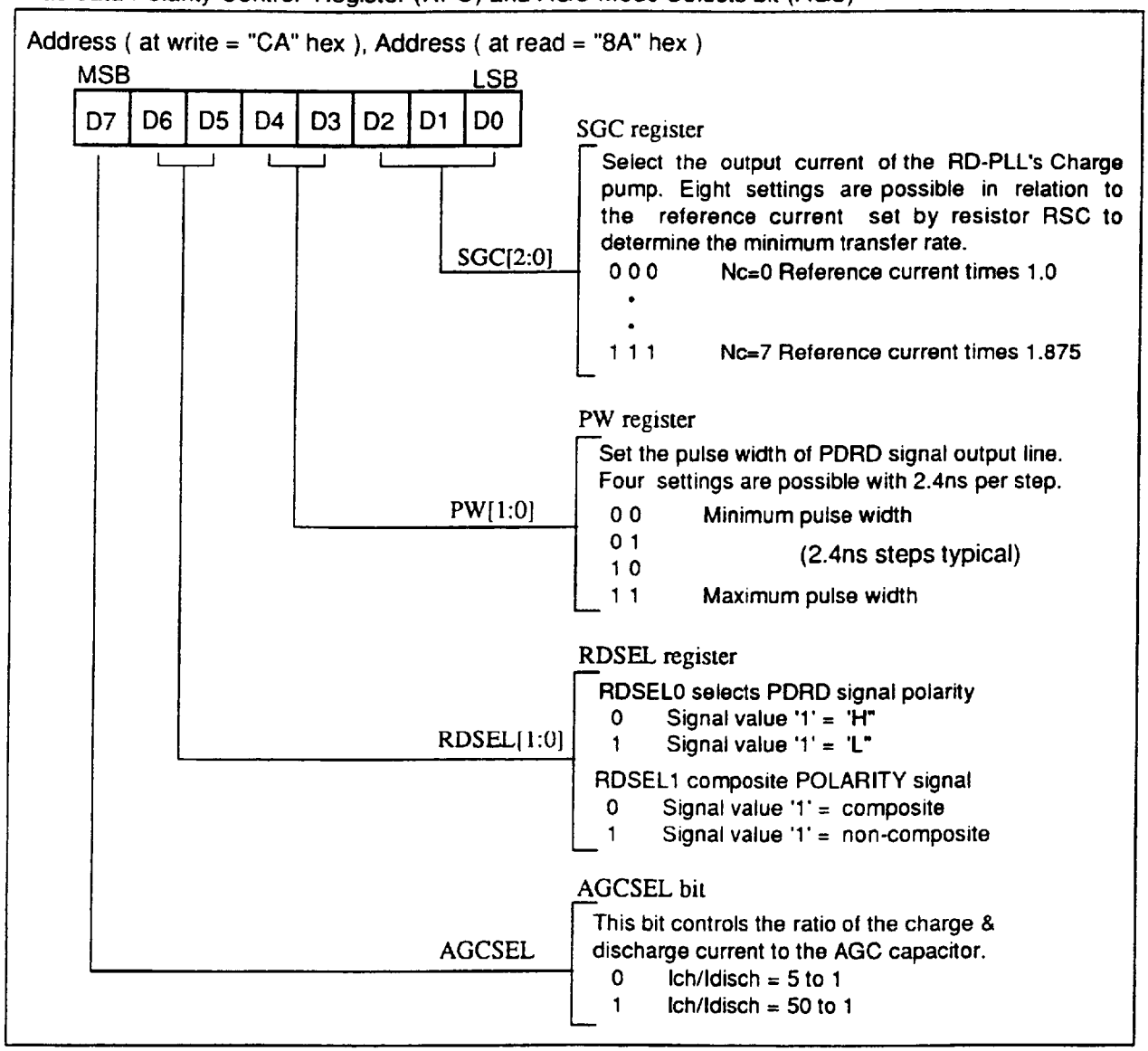
WFA[2:0]

This register adjusts eight setting of the window fine adjust circuit. The register setting adds fine delay to the Window adjustment circuit.

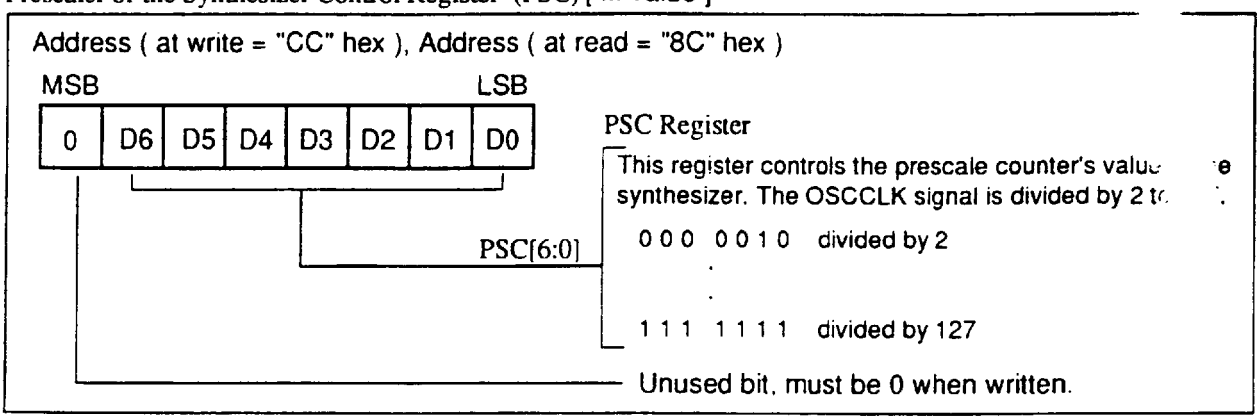
0 1 0 - 2 delay (- 0.50 ns typical)
0 0 1 - 1 delay (- 0.25 ns typical)
0 0 0 Center (0ns)
1 0 1 + 1 delay (+ 0.25 ns typical)
1 1 0 + 2 delay (+ 0.50 ns typical)

Register Descriptions (cont)

RD-PLL Gain Control Register (SGC), Read data Pulse Width Control Register (PW), Read data Polarity Control Register (RPC) and AGC Mode Selects bit (AGS)

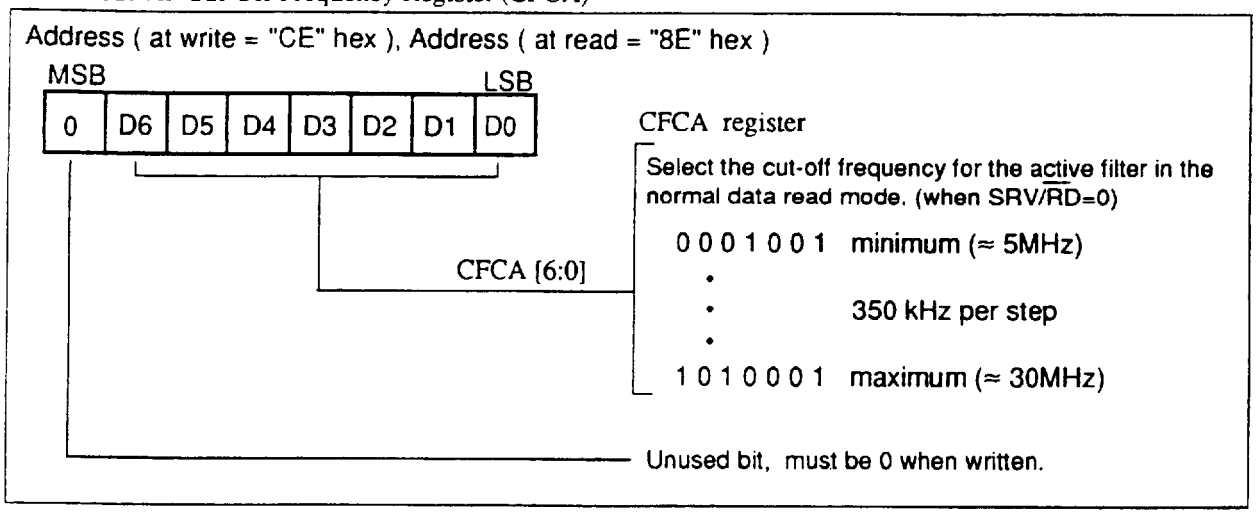


Prescaler of the Synthesizer Control Register (PSC) [M value]

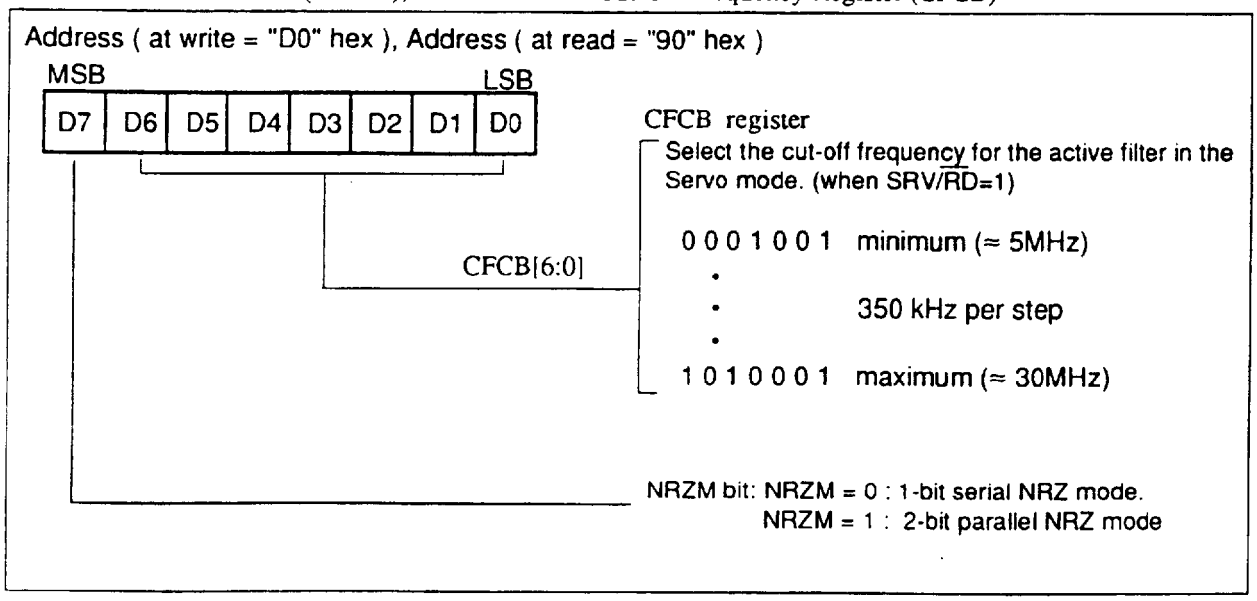


Register Descriptions (cont)

Read Mode AF Cut-Off Frequency Register (CFCA)



NRZ Data mode select bit (NRZM), Servo Mode AF Cut-Off Frequency Register (CFCB)



Register Descriptions (cont)

Unlock Detect Register (ULD) and Boost Level Control Register (BLC)

Address (at write = "D2" hex), Address (at read = "92" hex)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

BLC register

This register sets the boost amplifier's gain of the active filter for the equalization.

BLC[4:0]

0 0000 Minimum gain

.

.

1 1111 Maximum gain

ULD register

Select the unlocked detect gain for the RD-PLL synthesizer to activate the ULD~ output when unlock condition occurs.

ULD[1:0]

00 : 2 OSCCLK
01 : 4 OSCCLK
10 : 6 OSCCLK
11 : 8 OSCCLK

TESTBF — When this bit sets "1" , $\overline{\text{SYNCRD}}$(44Pin), $\overline{\text{DLYRD}}$(42Pin), $\overline{\text{DLYCLK}}$(41Pin) are output mode. Normaly this bit sets "0".

High-Pass Filter Cutoff Frequency Control Register (HPCA)

Address (at write = "D4" hex), Address (at read = "94" hex)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

HPCA Register

This register controls the cutoff frequency of the high-pass filter in the active filter circuit in the normal data read mode. (when SRV/$\overline{\text{RD}}$=0)The register changes it by 6.25% step.

HPCA[4:0]

0 1111 Maximum cutoff frequency (+ 93.75%)
•
• (+) 6.25% step
0 0001
0 0000 Center cutoff frequency (depend on CFC)
1 0111
• (-) 6.25% step
•
1 0000 Miniimum cutoff frequency (- 50%)

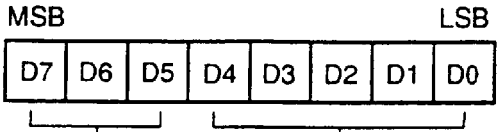
Unused bit, must be 0 when written.

This bit controls filter boost function on and off at servo mode.
" 1" : No boost at servo mode
" 0" : Boost at servo mode
(boost level : the same level at read mode)

Register Descriptions (cont)

High-Pass Filter Cutoff Frequency Control Register (HPCB)

Address (at write = "D6" hex), Address (at read = "96" hex)



HPCB Register

This register controls the cutoff frequency of the high-pass filter in the active filter circuit in the Servo mode.
(when SRV/$\overline{RD}$=1)The register changes it by 6.25% step.

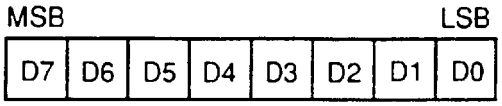
HPCB[4:0]

0 1 1 1 1	Maximum cutoff frequency (+ 93.75%)
•	
•	(+) 6.25% step
0 0 0 0 1	
0 0 0 0 0	Center cutoff frequency (depend on CFC)
1 0 1 1 1	
•	(-) 6.25% step
•	
1 0 0 0 0	Miniimum cutoff frequency (- 50%)

Unused bit, must be 0 when written.

High-Slice Level Register (VGSHA), low-Slice Level Register (VGSLA)

Address (at write = "D8" hex), Address (at read = "98" hex)



VGSLA Register

These are input to the internal DAC using VCOM as refenrece source to generate the programmable Low-Slice level for the Pulse detection circuit in the read mode. (when SRV/$\overline{RD}$="L")

VGSLA[3:0]

0 0 0 0	Minimum high-slice level (0% of VSH)
.	
.	
1 1 1 1	Maximum high-slice level (100% of VSH)

VGSHA Register

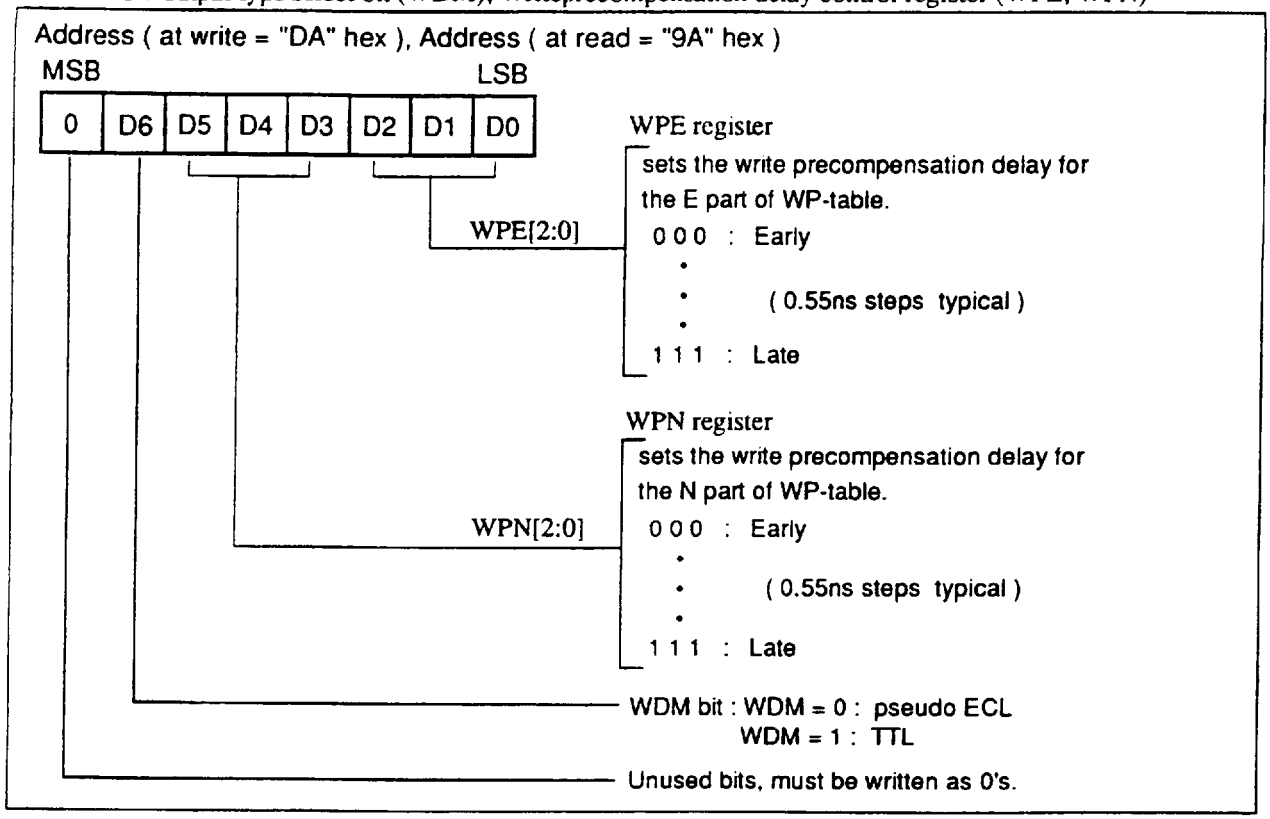
These are input to the internal DAC using VCOM as refenrece source to generate the programmable High-Slice level for the Pulse detection circuit both in the read and servo mode.

VGSHA[3:0]

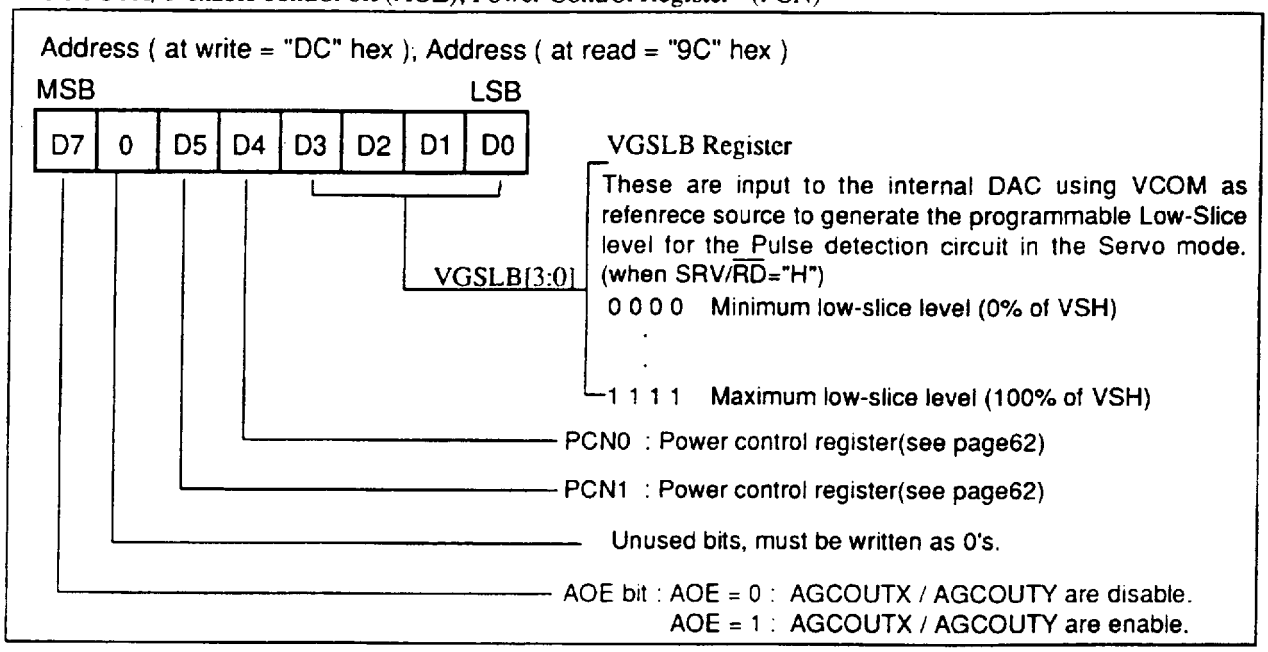
0 0 0 0	Minimum high-slice level (0% of VSH)
.	
.	
1 1 1 1	Maximum high-slice level (100% of VSH)

Register Descriptions (cont)

1-7WDOUT output type select bit (WDM), Writeprecompensation delay control register (WPE, WPN)



AGCOUTX/Y enable control bit (AOE), Power Control Register (PCN)



Register Descriptions (cont)

Test Mode Control Register (MDC)

Address = $hF

MSB							LSB
D7	0	D5	D4	D3	D2	D1	D0

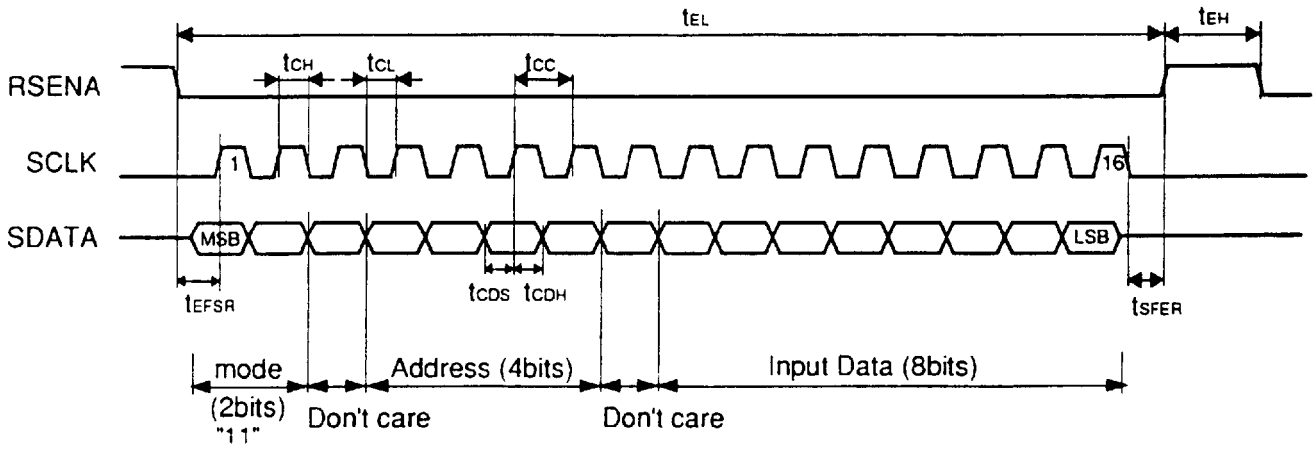
MDC[4:0] — *Reserved*

Unused bit, must be written as 0.

TEST: when set to "1", it enables the internal test mode.

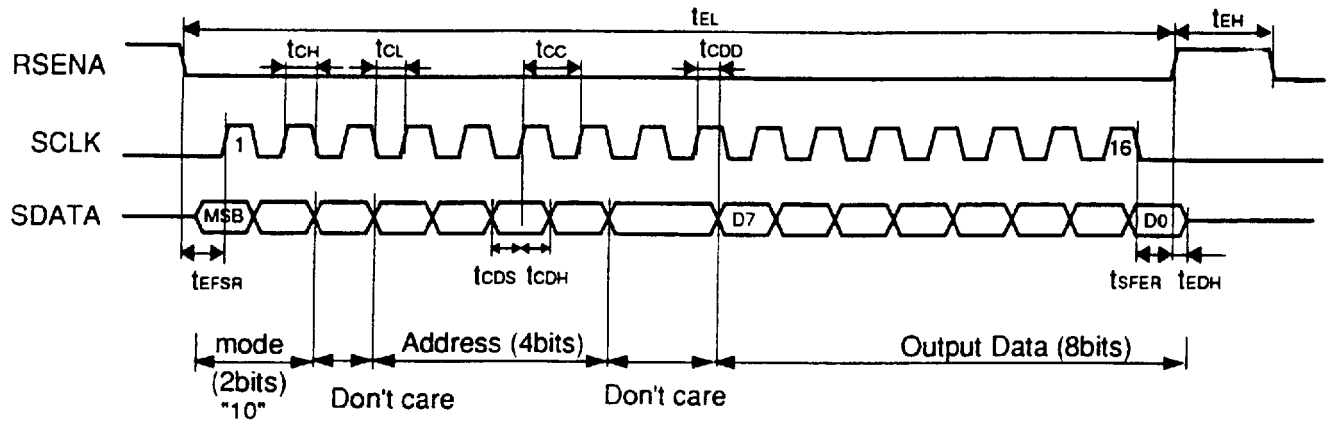
7. Read/Write timing of the control registers

< Write >



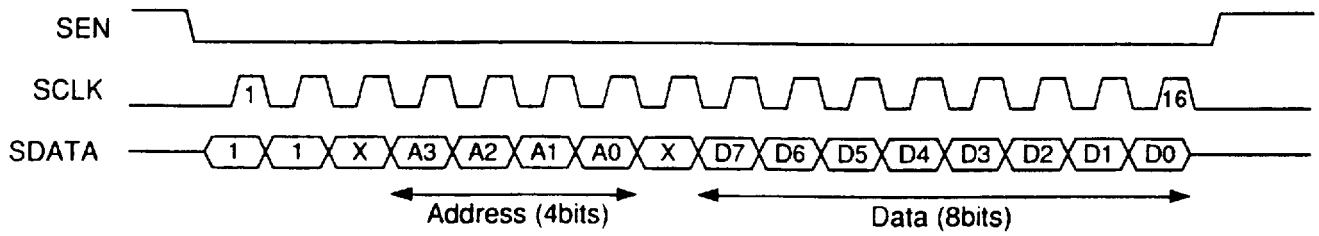
Read/Write timing of the control registers (cont)

< Read >

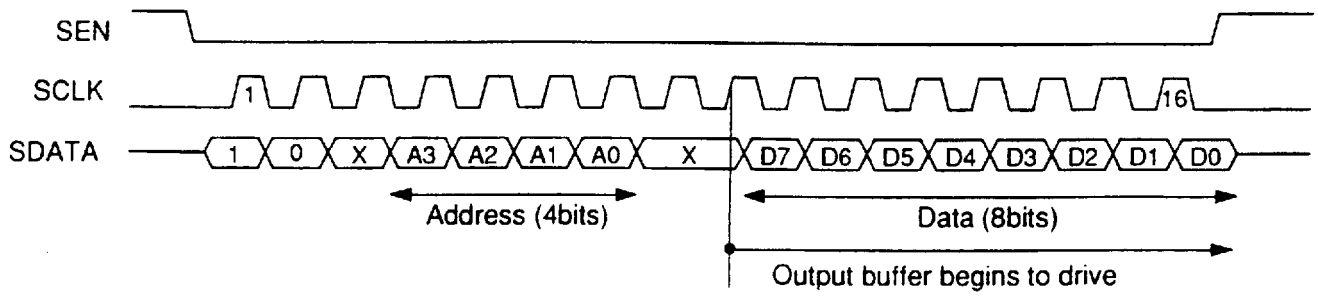


8. Write and read registers

Write to register

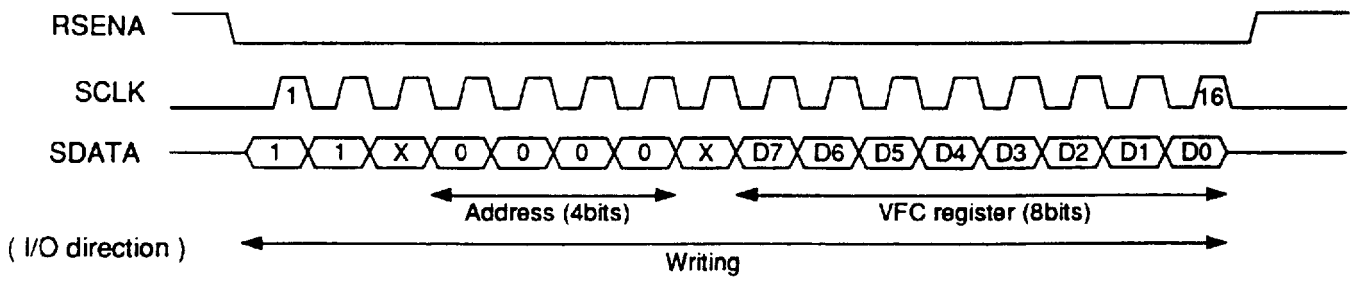


Read from register

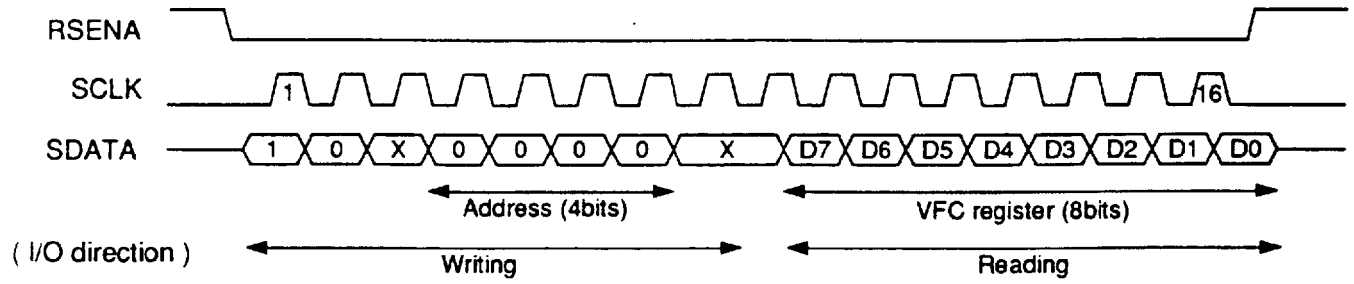


Write and read registers (cont)

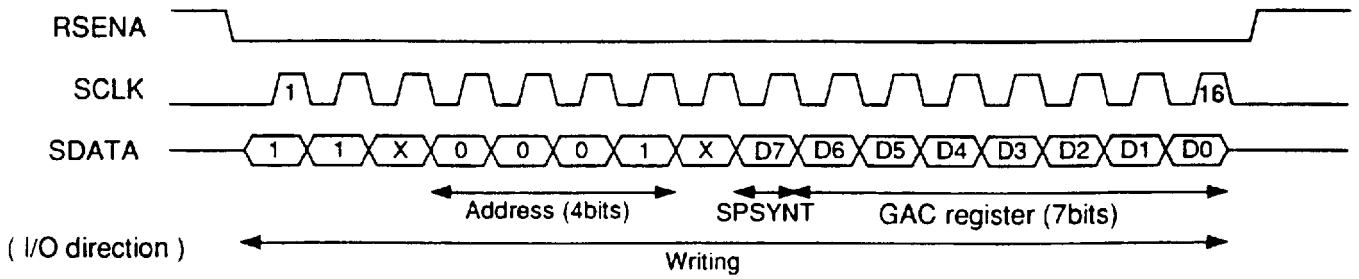
Write to VFC register



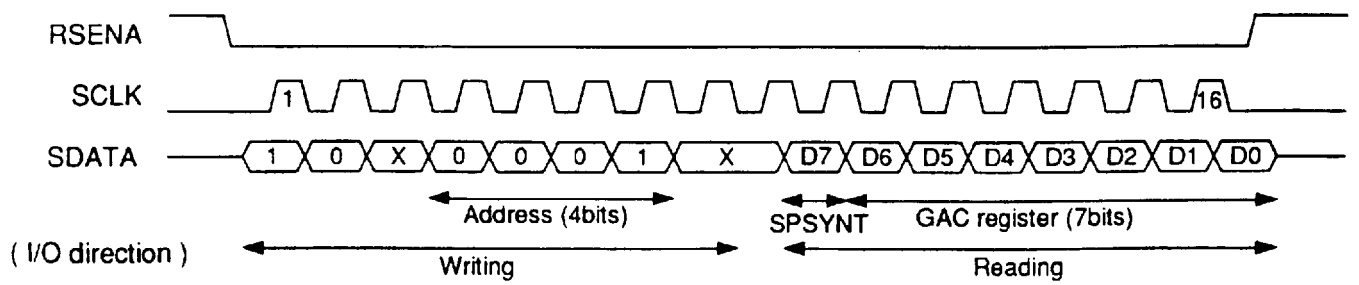
Read from VFC register



Write to GAC register

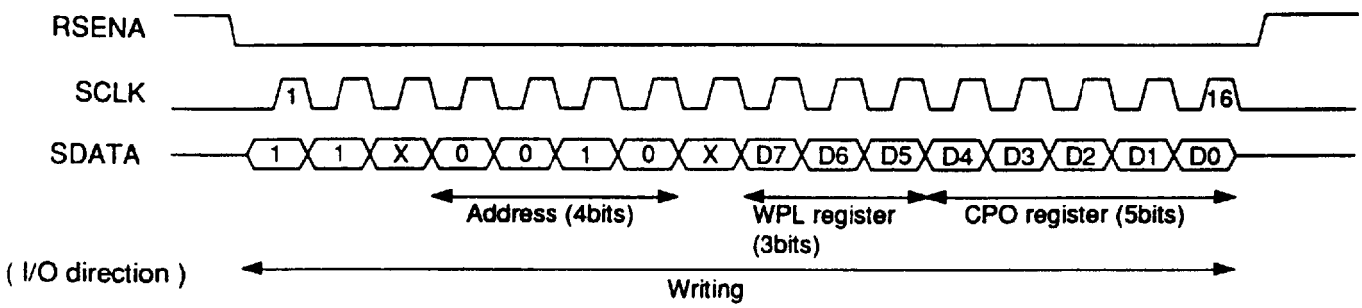


Read from GAC register

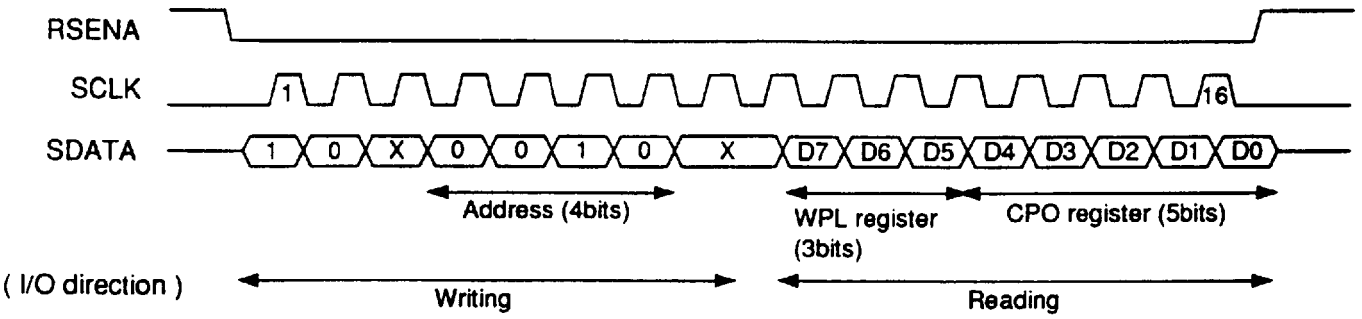


Write and read registers (cont)

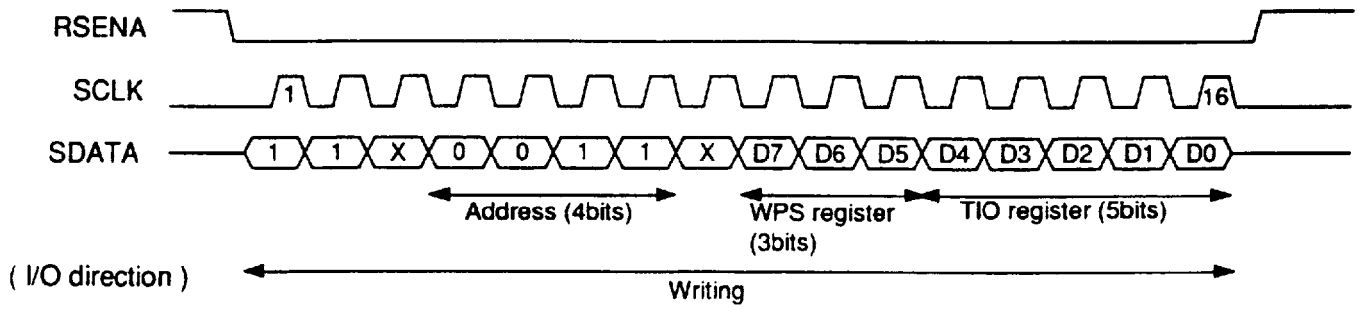
Write to WPLL & CPO register



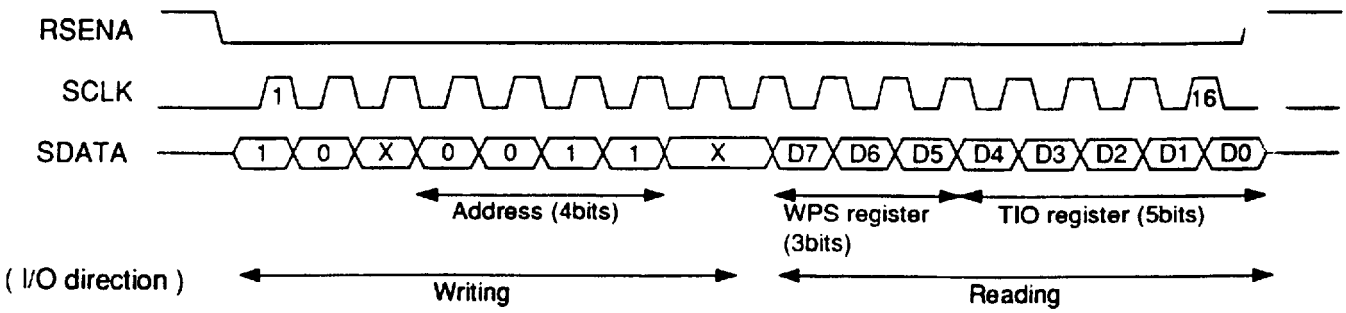
Read from WPLL &CPO register



Write to WPLS & TIO register

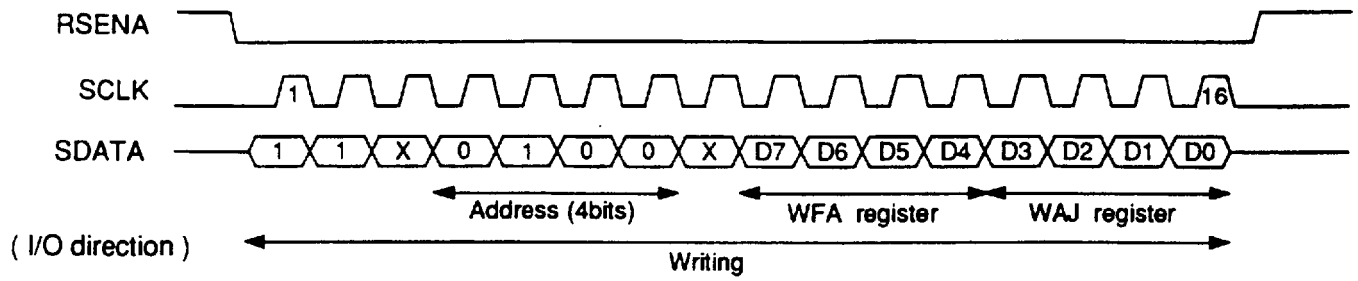


Read fromWPLS & TIO register

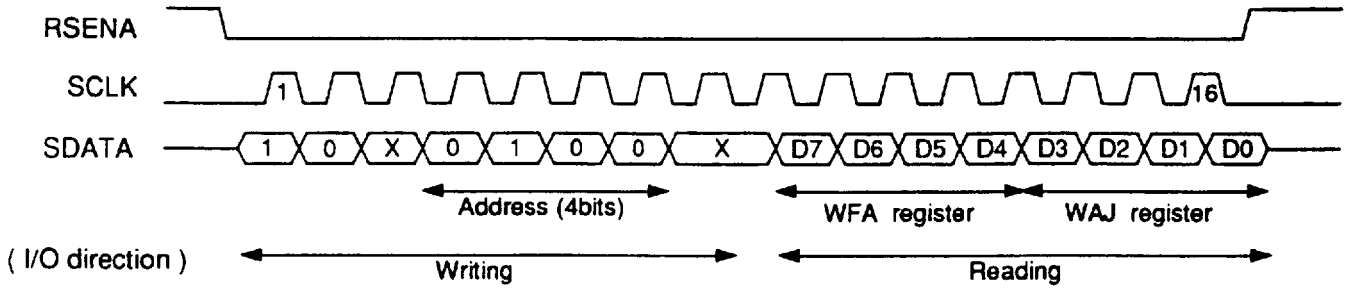


Write and read registers (cont)

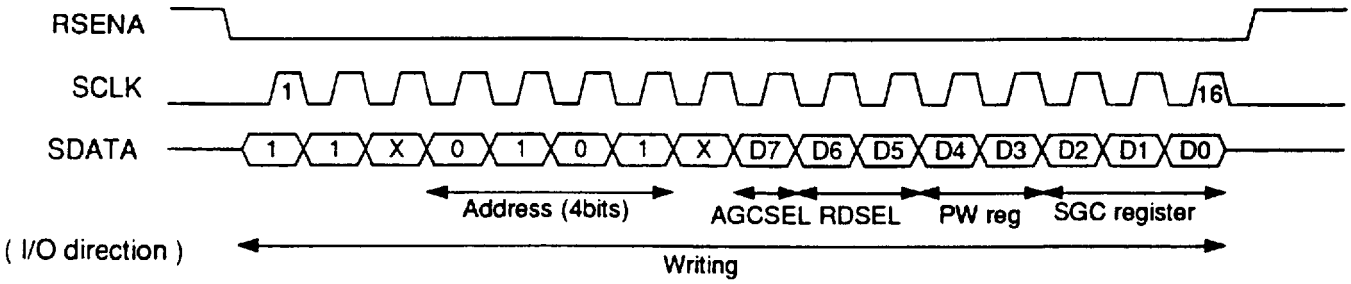
Write to WFA & WAJ register



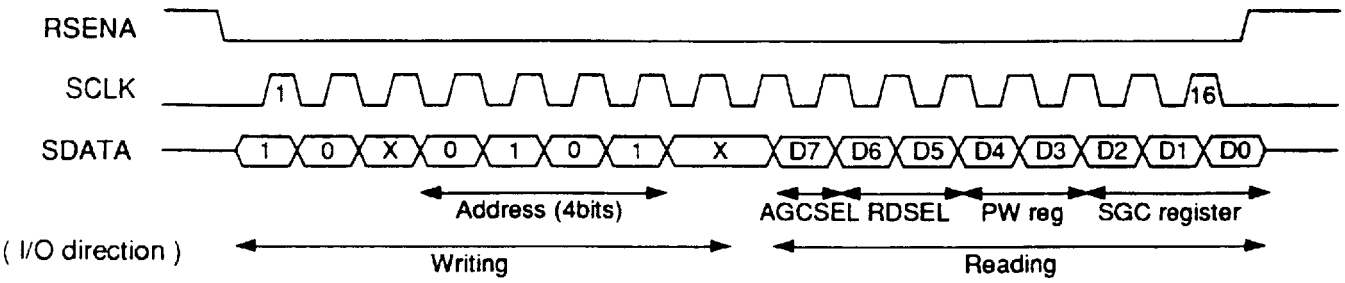
Read from WFA & WAJ register



Write to AGCSEL bit, RDSEL, PW & SGC register

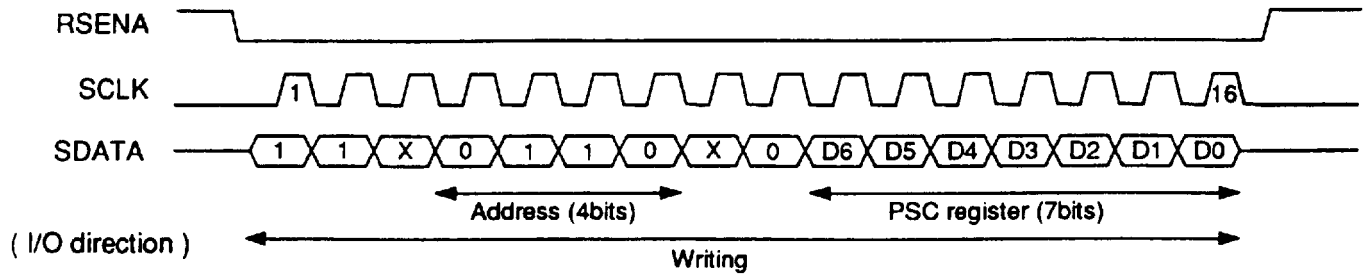


Read from AGS bit, RDS, PW & SGC register

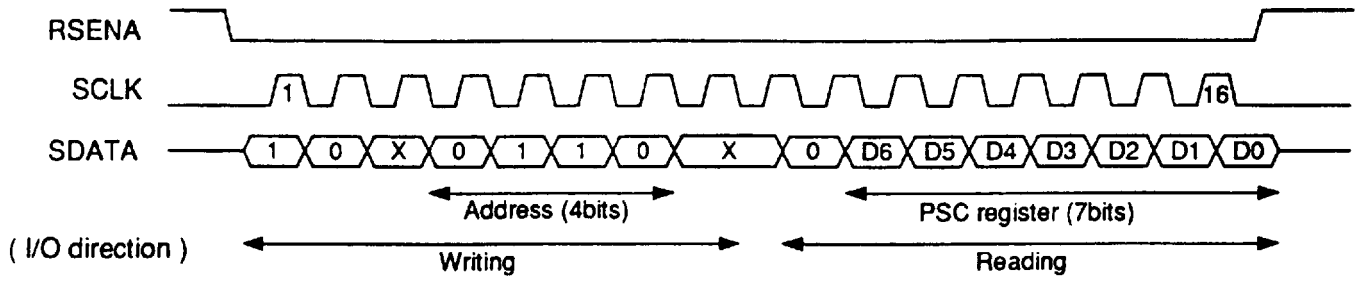


Write and read registers (cont)

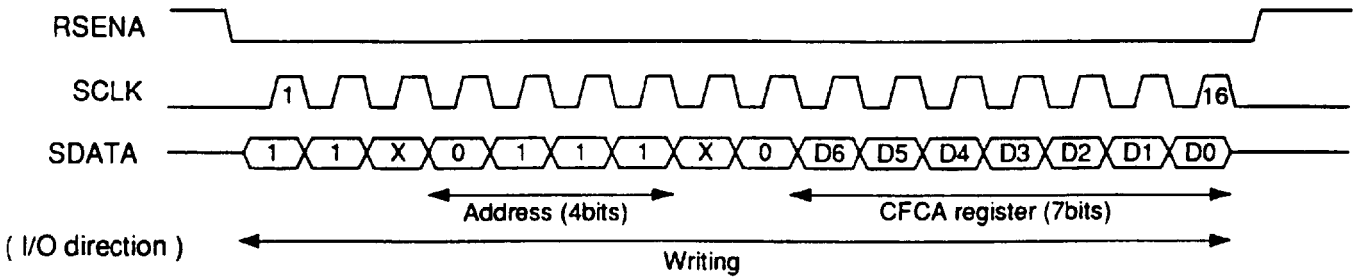
Write to PSC register



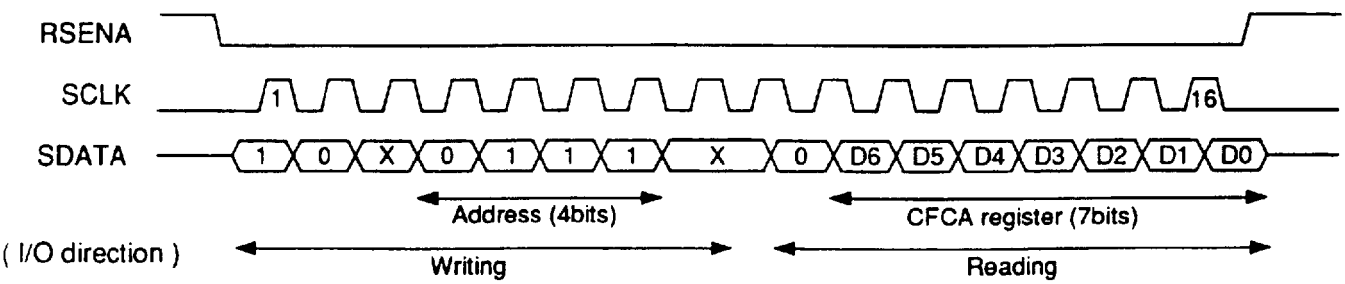
Read fromPSC register



Write to CFCA register

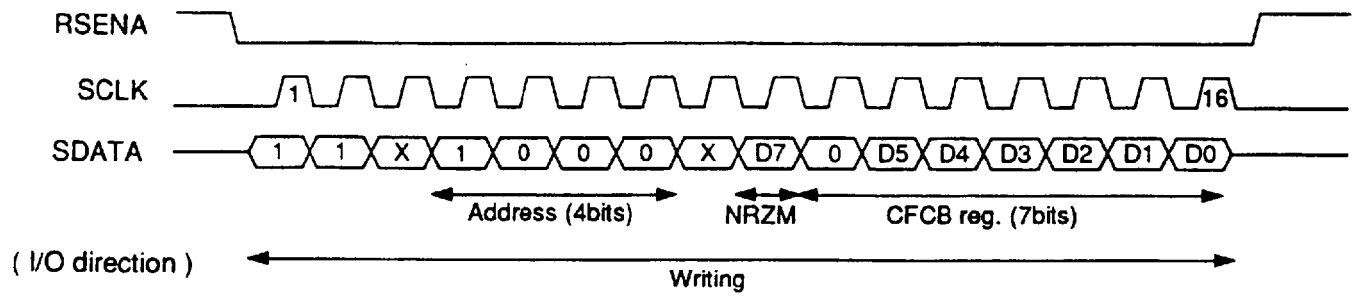


Read from CFC register

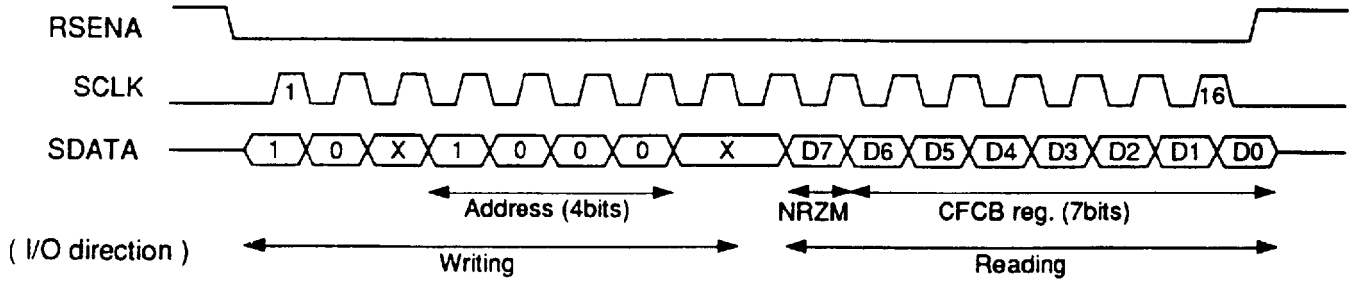


Write and read registers (cont)

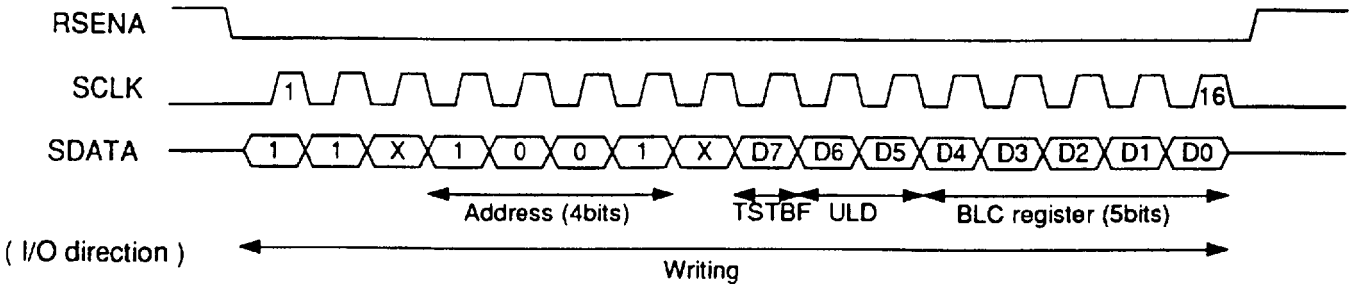
Write to NRZM bit & CFCB register



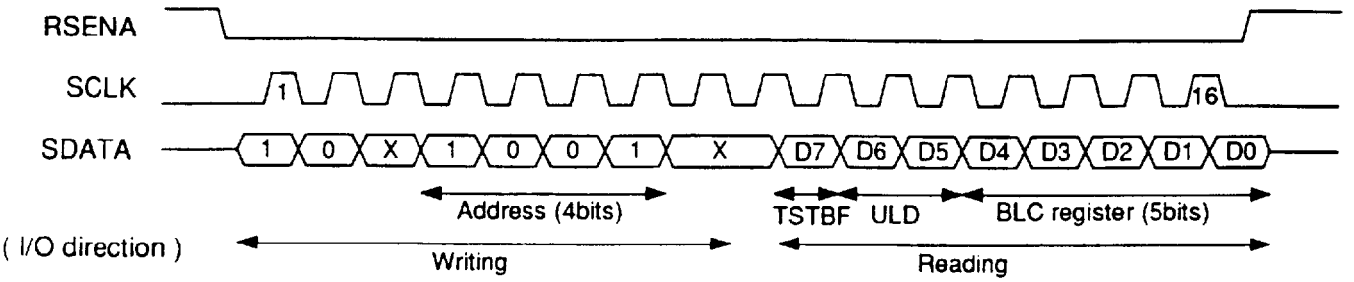
Read from NRZM bit & CFCB register



Write to ULD & BLC register

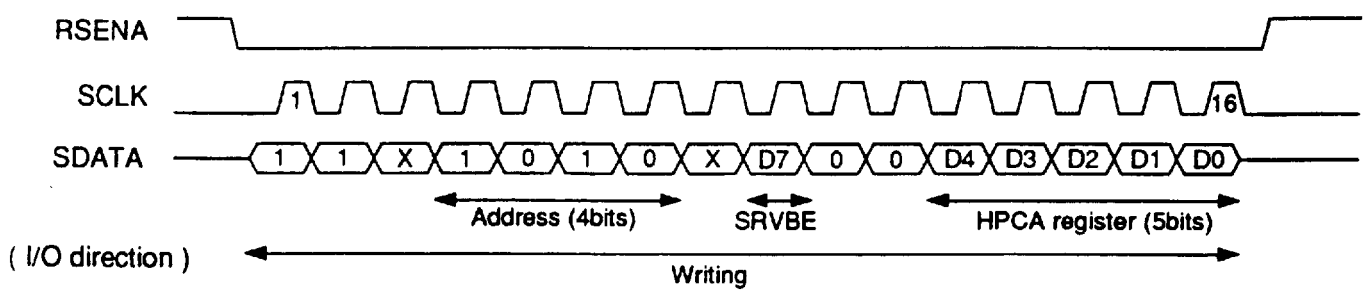


Read from ULD & BLC register

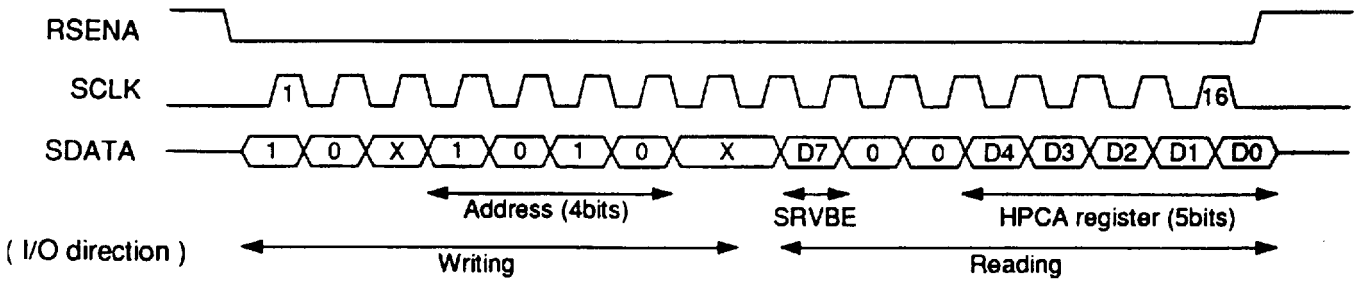


Write and read registers (cont)

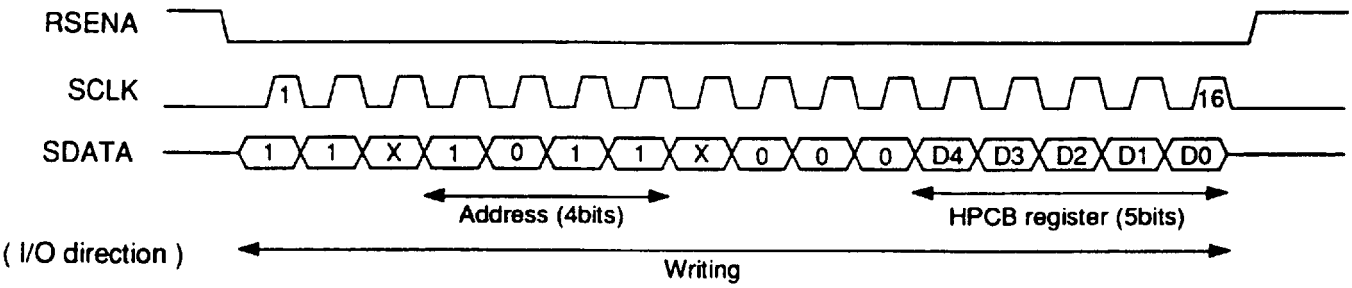
Write to HPCA register



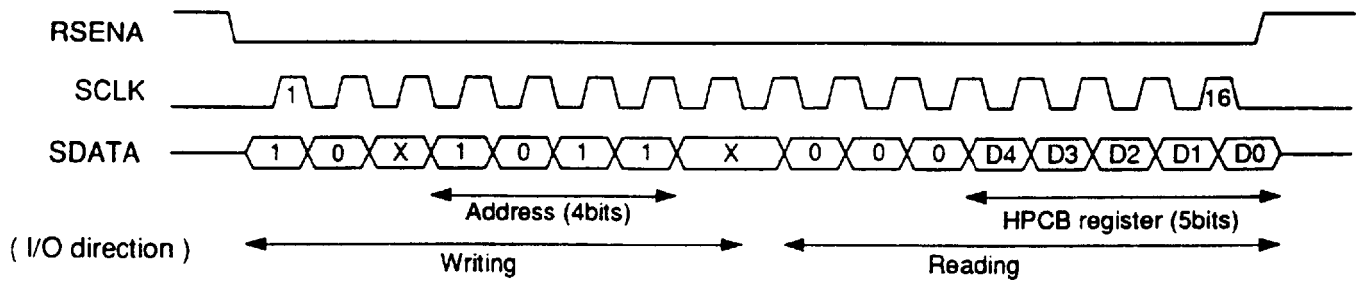
Read from HPCA register



Write to HPCB register

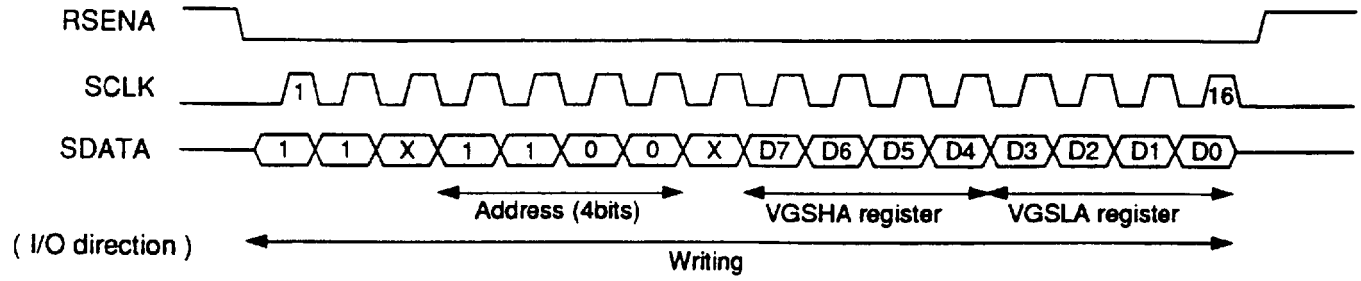


Read from HPCB register

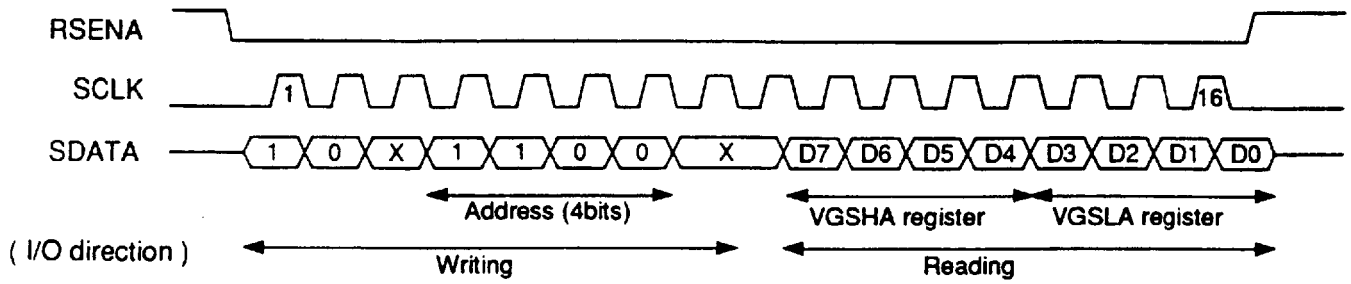


Write and read registers (cont)

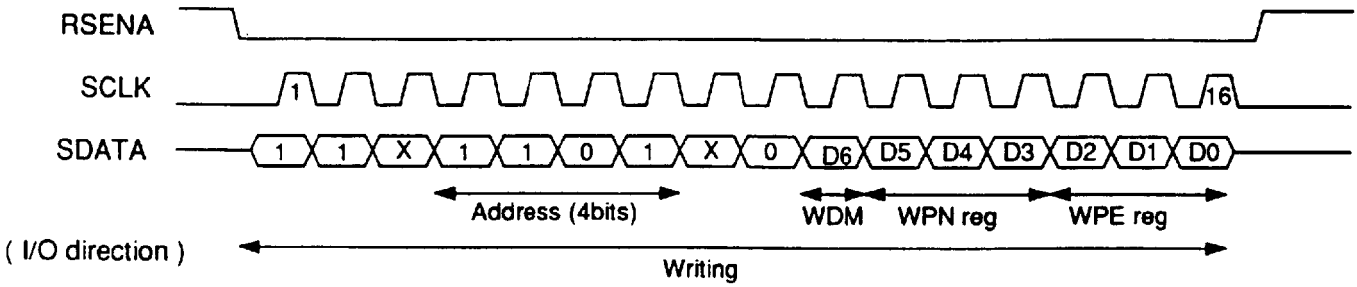
Write to VGSHA & VGSLA register



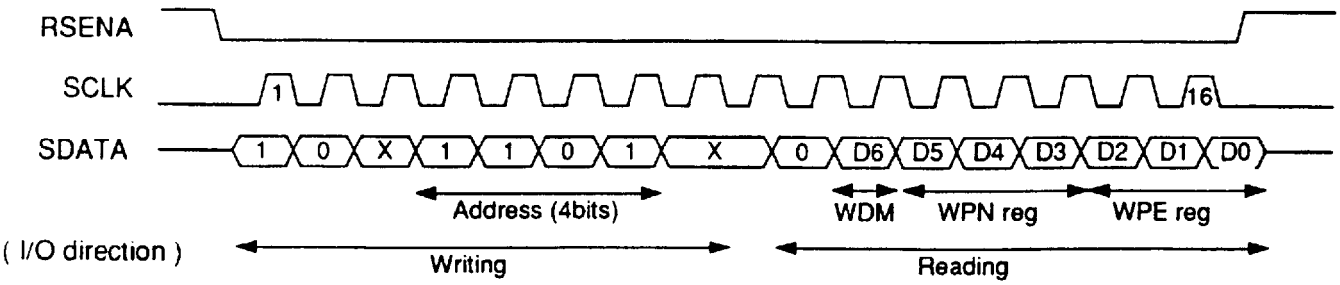
Read from VGSHA & VGSLA register



Write to WDM bit, WPN & WPE register

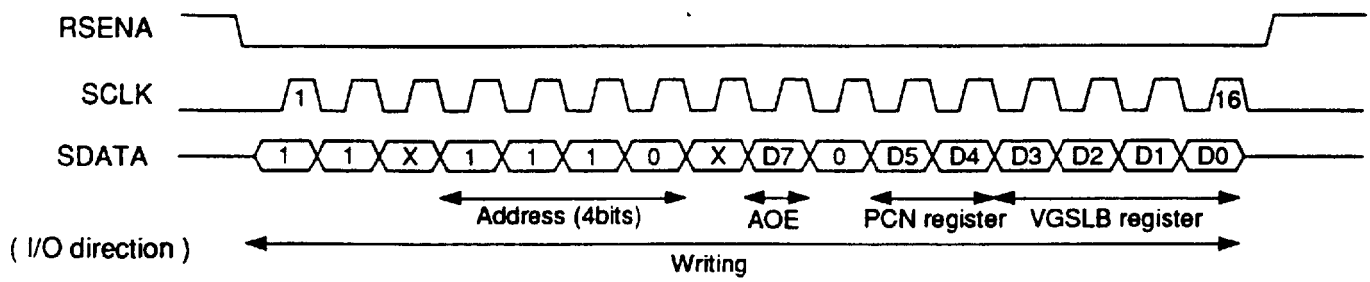


Read from WDM bit, WPN & WPE register

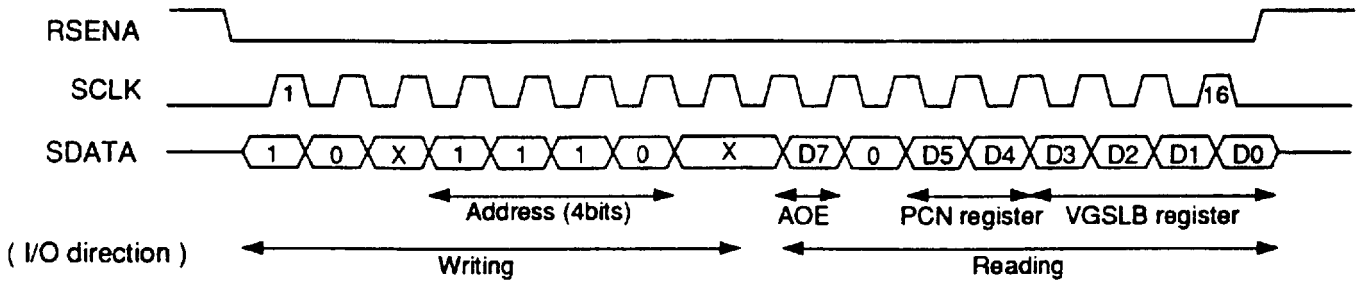


Write and read registers (cont)

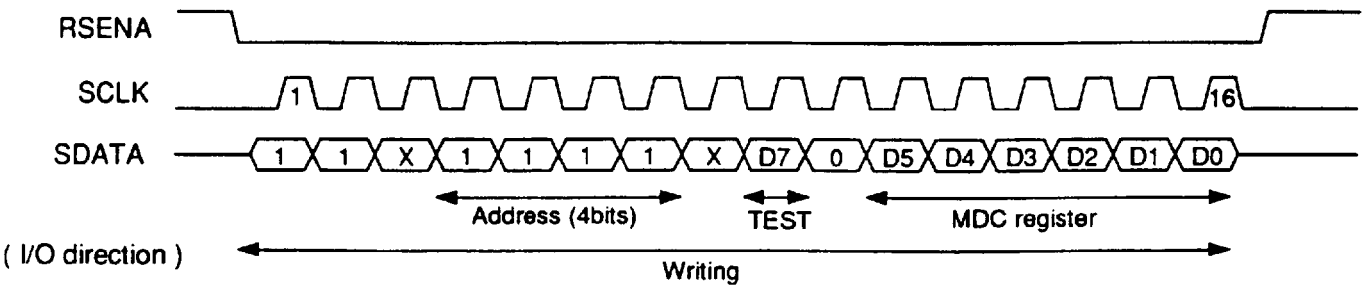
Write to AOE bit, VGSLB & PCN register



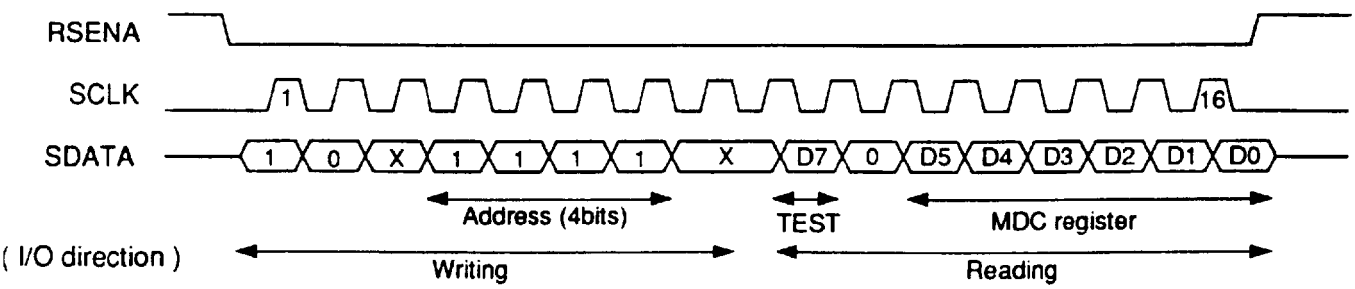
Read from AOE bit, VGSLB & PCN register



Write to MDC register



Read from MDC register



9. Absolute Maximum Ratings (Ta=25 °C)

Description	Symbol	Ratings	Unit	Applicable pins
Supply voltage	Vcc	7	V	DVcc, AVcc
Input voltage	Vi	- 0.3 to 5.5	V	Note1
Output voltage	Vo	5.5	V	Note2
Operating temperature	Topr	0 to 70	°C	
Storage temperature	Tstg	- 55 to + 125	°C	

Note1: OSCCLK,$\overline{\text{RESET}}$,IDLE/$\overline{\text{SERVO}}$,RSENA,SCLK,SDATA,$\overline{\text{DUMP}}$,$\overline{\text{CHA}}$,$\overline{\text{SHORT}}$,$\overline{\text{RX}}$,AGCHOLD,RG, SRV/$\overline{\text{RD}}$,NRZRD/WD0(Write mode),NRZRD/WD1(Write mode),WG,$\overline{\text{DCERA}}$

Note2: SDATA,POL,$\overline{\text{ULD}}$,PDRD,$\overline{\text{DLYCLK}}$,$\overline{\text{DLYRD}}$,$\overline{\text{SYNCRD}}$,RRCLK,CLKOUT1-7WDOUT,1-7WDOUT, NRZRD/WD0(Read mode),NRZRD/WD1(Read mode)

10. Electrical Characteristics (Ta=0 to + 70 °C, Vcc = 5.0V ± 10% unless otherwise noted)

General

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
Power supply voltage	Vcc	4.5	5	5.5	V		Note4
Operation temperature	Ta	0	25	70	°C		
Transfer rate		15		56	Mbps		
Power supply current	Icc		780	TBD	mW	at 50Mbps, R/W 20% Idle/Servo mode 80%.	Note4
TTL 'H' level intput voltage	V_{IH}	2.2			V	Vcc=4.5V	Note1
TTL 'L' level intput voltage	V_{IL}			0.8	V	Vcc=4.5V	Note1
TTL 'H' level output voltage	V_{OHT}	2.4			V	I_{OH}=-400μA, Vcc=4.5V	Note2
TTL 'L' level output voltage	V_{OLT}			0.5	V	I_{OL}=4mA, Vcc=4.5V	Note2
ECL 'H' level output voltage	V_{OHE}	Vcc -0.95	Vcc -0.8		V	Ta=25°C, RL=510Ω	Note3
ECL 'L' level output voltage	V_{OLE}		Vcc -1.8	Vcc -1.6	V	Ta=25°C, RL=510Ω	Note3
Input current	I_{IH}			20	μA	Vcc=5.5V,Vi=2.7V	Note1
	I_{IL}			-400	μA	Vcc=5.5V,Vi=0.4V	Note1
Output shorted current	Ios	-20		-120	mA	Vcc=5.5V	Note2
Input clamp voltage	V_{IK}			-1.5V	V	Vcc=4.5V,I_{OH}=-18mA	Note1

Note1: OSCCLK,$\overline{\text{RESET}}$,IDLE/$\overline{\text{SERVO}}$,RSENA,SCLK,SDATA,$\overline{\text{DUMP}}$,$\overline{\text{CHA}}$,$\overline{\text{SHORT}}$,$\overline{\text{RX}}$,AGCHOLD,RG, SRV/$\overline{\text{RD}}$,NRZRD/WD0(Write mode),NRZRD/WD1(Write mode),WG,$\overline{\text{DCERA}}$

Note2: SDATA,POL,$\overline{\text{ULD}}$,PDRD,$\overline{\text{DLYCLK}}$,$\overline{\text{DLYRD}}$,$\overline{\text{SYNCRD}}$,RRCLK,CLKOUT,$\overline{\text{1-7WDOUT}}$(TTL), 1-7WDOUT(TTL), NRZRD/WD0(Read mode),NRZRD/WD1(Read mode)

Note3: 1-7WDOUT(ECL),1-7WDOUT(ECL)

Note4: DVcc,AVcc(PH),AVcc(W),AVcc(R),AVcc(AF),AVcc(AGC),AVcc(RPD)

11. Encoder/Decoder(Ta=25°C, Vcc=5V,56Mbps)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
NRZRD set-up time(serial)	t_{SNRS}	9.0			ns		NRZRD/WD0
NRZRD set-up time(parallel)	t_{SNRP}	16.0			ns		NRZRD/WD0,1
NRZRD hold time(serial)	t_{HNRS}	8.0			ns		NRZRD/WD0
NRZRD hold time(parallel)	t_{HNRP}	21.0			ns		NRZRD/WD0,1
NRZWD set-up time(serial)	t_{SNWS}	8.0			ns		NRZRD/WD0
NRZWD set-up time(parallel)	t_{SNWP}	17.0			ns		NRZRD/WD0,1
NRZWD hold time(serial)	t_{HNWS}	0			ns		NRZRD/WD0
NRZWD hold time(parallel)	t_{HNWP}	0			ns		NRZRD/WD0,1
RRCLK high time	T/2(H)	14			ns		RRCLK
RRCLK low time	T/2(L)	14			ns		RRCLK
Decode time	t_{DD}		14	14	RRCLK		NRZRD/WD0
Encode time	t_{ED}		12.5	14.5	RRCLK		$\overline{1\text{-}7WDOUT}$, 1-7WDOUT
Write Precomp time step		0.28	0.55	0.82	ns	Not tested	
Write Precomp time width		± 2.0	± 3.85	± 5.7	ns	± 7steps	

12. Register (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
RSENA "L" time	t_{EL}	1650			ns		RSENA
RSENA "H" time	t_{EH}	50			ns		RSENA
RSENA falling edge to the first SCLK rising edge	t_{EFSR}	50			ns		SCLK
SDATA set up time	t_{CDS}	10			ns		SDATA
SDATA hold time	t_{CDH}	10			ns		SDATA
The last SCLK falling edge to RSENA rising edge	t_{SFER}	50			ns		RSENA
SCLK cycle time	t_{CC}	100			ns		SCLK
SCLK "H" time	t_{CH}	40			ns		SCLK
SCLK "L" time	t_{CL}	40			ns		SCLK
SDATA output delay	t_{CDD}			20	ns		SDATA
SDATA output hold time	t_{EDH}	5			ns		SDATA

13. Synchronizer (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Read VCO center frequency 1	fvco1	34.2	36	37.8	MHz	RFVCO=3k, Register VFC=80 Hex
Phase lock acquisition time 1		—	—	6	Byte	6 NRZ bytes period at 24Mbps
Capture range 1		±15	—	—	%	at 24Mbps
Lock range 1		±15	—	—	%	at 24Mbps
Read VCO gain 1		126	160	194	Mrad / sec •V	RFVCO=3k, Register VFC=80 Hex
Read VCO upper limit clamping frequency 1		—	48	—	MHz	RFVCO=3k, Register VFC=80 Hex
Read VCO lower limit clamping frequency 1		—	27	—	MHz	RFVCO=3k, Register VFC=80 Hex
Read VCO center frequency 2	fvco2	67.5	72	75.5	MHz	RFVCO=3k, Register VFC=FF Hex
Phase lock acquisition time 2		—	—	6	Byte	6 NRZ bytes period at 48Mbps
Capture range 2		±15	—	—	%	at 48Mbps
Lock range 2		±15	—	—	%	at 48Mbps
Read VCO gain 2		174	220	266	Mrad / sec •V	RFVCO=3k, Register VFC=FF Hex
Read VCO upper limit clamping frequency 2		—	95	—	MHz	RFVCO=3k, Register VFC=FF Hex
Read VCO lower limit clamping frequency 2		—	53	—	MHz	RFVCO=3k, Register VFC=FF Hex
Window margin loss		0		3	ns	at any data rate
Window adjust step		0.34	0.67	1.0	ns	31 steps, Not tested
Window adjust width		+5.5 -5.9	+10.0 -10.7	+14.5 -15.5	ns	+15 step, -16step
Window fine adjust width		0.12	0.25	0.5	ns	total 5 steps
Read VCO maximum oscillate frequency		90	108	—	MHz	RFVCO=1k, Register VFC=80 Hex

14. Synthesizer (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Write VCO center frequency	fwvco	67.5	71.5	75.5	MHz	RSVCO=6.2k, Register VFC=FF Hex
Write VCO upper limit clamping frequency		—	86	—	MHz	RSVCO=6.2k, Register VFC=FF Hex
Write VCO lower limit clamping frequency		—	56.8	—	MHz	RSVCO=6.2k, Register VFC=FF Hex
Phase lock acquisition time		—	—	1	ms	tested at 24Mbps,48Mbps
Capture range		±10	—	—	%	tested at 24Mbps,48Mbps
Lock range		±10	—	—	%	tested at 24Mbps,48Mbps
VCO frequency step		—	1.0	—	%	at f_{MAX} / f_{LOW} = 2.55
VCO gain		84	106	128	Mrad / sec • V	RSVCO=6.2k, Register VFC=FF Hex
Max frequency		80	—	—	MHz	RSVCO=2.3k, Register VFC=80 Hex

15. RPD & PH (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
Max peak-peak Input signal				2.0	Vpp	differential inputs	PHINX/Y
PDRD pulse width		4.5	9	13.5	ns	at 40Mbps, PW[1:0]=00	
PDRD pulse rise time	tr	0.5	2	4	ns	CL=15pF,20%-80%, Not tested	
PDRD pulse fall time	tf	0.5	2	4	ns	CL=15pF,80%-20%, Not tested	
P/H output voltage swing		2.0	2.3	2.6	V	fin=6.5MHz, Vin=2Vpp **	
P/H output leakage current		-0.2	0	+0.2	µA		OUT0 ~ OUT3
P/H Channel Offset		-50		+50	mV		OUT0 ~ OUT3
P/H Reference Voltage			VCOM x 25%		V	PHINX/Y=0Vpp	OUT0 ~ OUT3
P/H Discharge time	t_{DSCG}			2.0	µS	C_{OUT0} ~ C_{OUT3} =1000pF	OUT0 ~ OUT3 $\overline{DUMP}$
P/H Sampling time ($\overline{CHA}$ = "L" time)	t_{SPL}	2.0			µS		$\overline{CHA}$
$\overline{CHA}$ Switching time	t_{SWT}	200			ns		$\overline{CHA}$

** : differential input for PHINX and PHINY.

17. Active Filter (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Filter cutoff frequency	fc	5		25	MHz	
fc Accuracy	fca	(- 15)		(+15)	%	
Filter boost level	Fb	0		10	dB	
Filter boost Accuracy	Fba	- 1		1	dB	Fb = 10dB
Output dynamic range			1.8	2.0	Vpp	diff. outputs, THD < 2%
Output noise(normal)			3	5.5	mVRms	Not tested
Output noise(differential)			6	10	mVRms	Not tested
Group delay variation (0)			± 3		%	Fb=0, condition 1
Group delay variation (1)			± 3		%	Fb=10, condition 1
Power noise rejection	PSRR		- 45		dB	Not tested

Condition 1: fc =18MHz, range = 0.2fc to fc, measured from AGCOUTX/Y to FILOUTX/Y.

18. AGC (Ta=25°C, Vcc=5V)

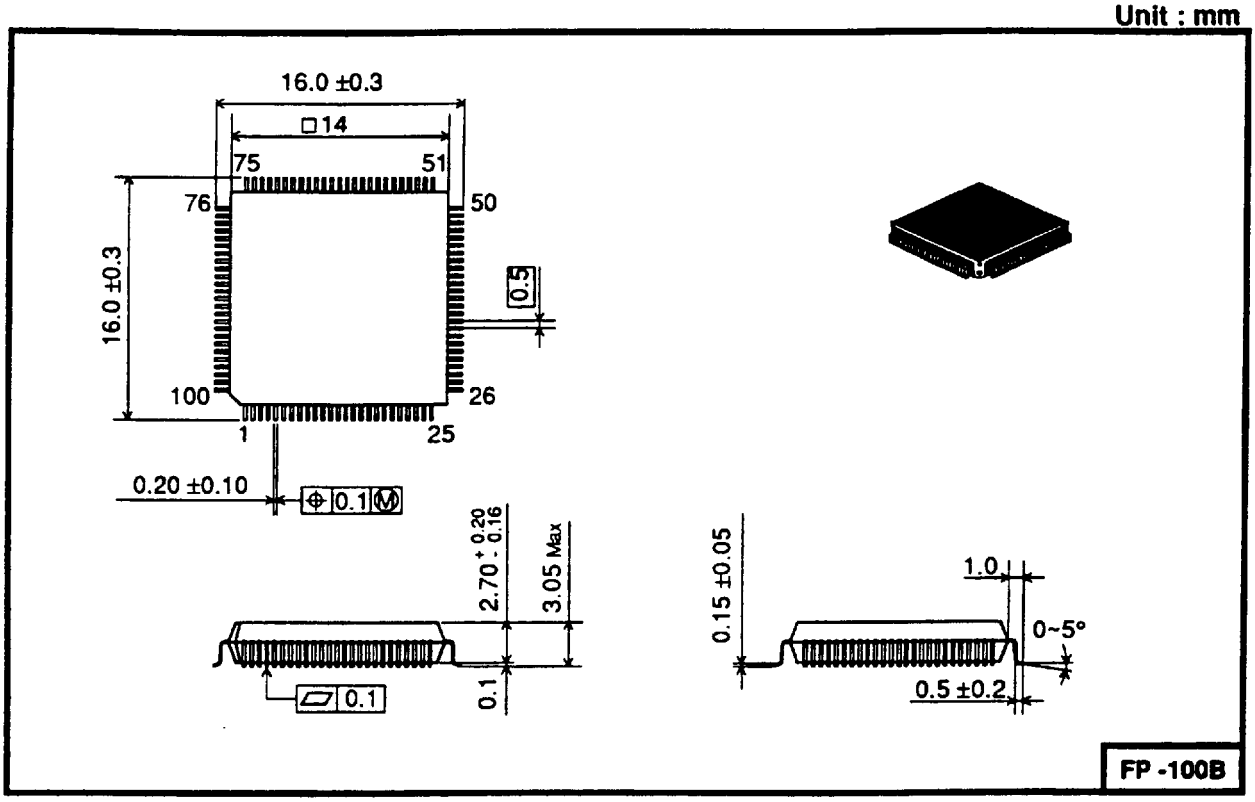
Item	Symbol	min	typ	max	unit	conditions
AGC max gain		(39)	41		dB	RINX/Y to FILOUTX/Y
AGC min gain				0	V/V	
Input dynamic range		20		200	mV	Distortion <2%
Band width(-3dB)	Bw	50			MHz	
Output DC offset	Voff		100	200	mV	AGCOUTX/Y
Input noise(max gain)			5	15	nV/$\sqrt{Hz}$	Not tested
Write to read recovery time	twrr		1	2	µs	write($\overline{RX}$=L) to read cycle
Read recovery time	trr			5	µs	recovery from max gain

19. P/H of servo mode (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
AGC initialize time	t_{XS}	150			ns	
AGC gain attack time	t_{AGCA}			2	µs	CRD=3300pF
P/H discharge time	t_{DSCG}			2	µs	C_{OUT0}~C_{OUT3}=1000pF
$\overline{CHA}$ sample waiting time	t_{SWT}	200			ns	
P/H sample time	t_{SPL}	2			µs	

20. PACKAGE DIMENSIONS

Unit : mm



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