HITACHI MONOCHROMATIC IMAGING DEVICE

HE 98222

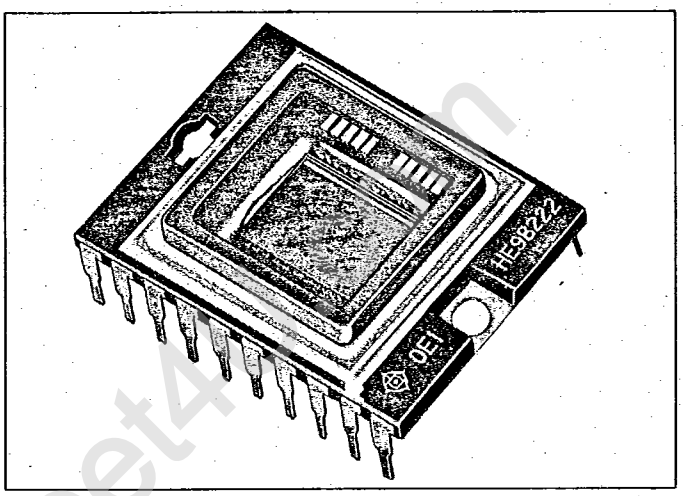
MOS IMAGING DEVICE
384 (H) x 485 (V)
Picture element

HITACHI

The Hitachi Monochrome Imaging Device HE98222 is a two-dimensional MOS imaging device developed for use in high-resolution monochrome TV cameras and three-chip color cameras.

The device has 384 horizontal and 485 vertical picture elements arranged in a densely staggered form to offer a 500 TV line horizontal resolution. The n-p-n vertical three layer structur of the device makes it sensitive to visible light to help suppress blooming.

The device is assembled in a 20-pin dual-in-line package with an optical glass cap.



FEATURES

- Maximum resolution derived from the densely staggered arrangement of 384 (horizontal) by 485 (vertical) picture elements.
- Resolution: 500 TV lines (horizontal)
  350 TV lines (vertical)
- Low operating voltage and low power dissipation-as low as 60 mW.
- Blooming eliminated by the n-p-n vertical three layer structure.
- Effective picture size: 8.8 mm x 6.6 mm.

DEVICE CONFIGURATION AND OPERATION

Fig. 2 shows the schematic diagram of HE98222. Picture elements are centered, with vertical and horizontal shift registers in the periphery.

The method of arranging picture elements in the device has been changed from the previous aligned arrangement to a densely staggered arrangement, in which the picture elements are each shifted a half pitch horizontally to allow picture element interpolation. This interpolation effect is increased by a concurrent two-line scanning system, allowing a horizontal resolution nearly two times the number of horizontal picture elements (500 TV lines).

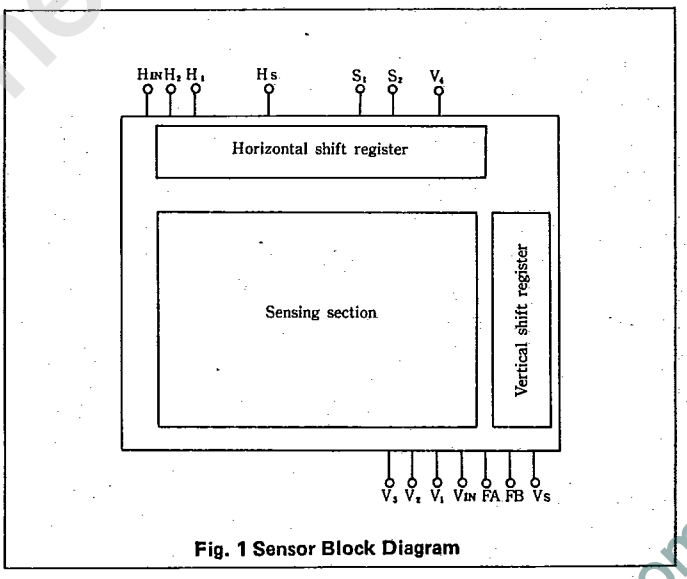


Fig. 1 Sensor Block Diagram

Note: The information contained herein is tentative and way be changed without prior notice. It is therefore advisable to contact Hitachi before processing with the design of equipment in corporating this product.

www.DataSheet4U.com

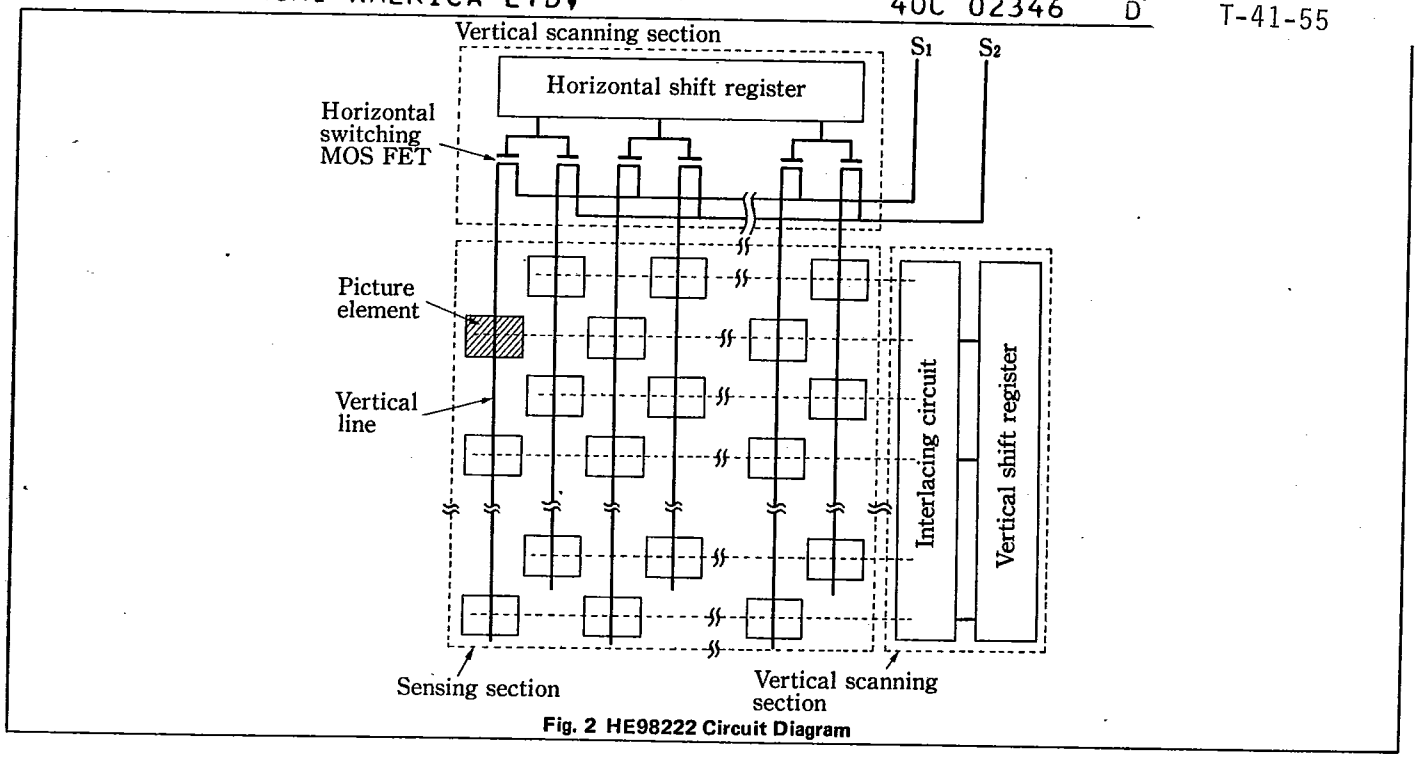


Fig. 2 HE98222 Circuit Diagram

1. SENSING SECTION

The sensing section consists of 384 horizontal and 485 vertical picture elements-a total of 186, 240 picture elements.

Figure 3 shows a typical cross section of a picture element.

The picture element is formed in a p-type island, called the WELL layer of the N-type substrate the FET source.

Incident light, passing through the SiO_2 film with little light absorption, reaches the photodiode at exceptionally high transmittance.

To increase the saturation signal current, a high-concentration layer (P^+) is formed in a portion of the photodiode for added storage capacitance, resulting in a wider dynamic range. Blooming is suppressed by a vertical three-layer structure consisting of the substrate, the WELL layer, and the photodiode. As incident light strikes the photodiode, it causes a proportionate signal charge to be stored in it. (Actually, the charge of the photodiode produced by video voltage V_V is discharged in proportion to the quantity of the incident light.) Next, when the vertical shift register selects a given line, the stored signal charge moves from the photodiode to a vertical signal line. Then, the horizontal shift register turns ON the horizontal switching MOS FET in each step to output the signal charges on the vertical signal line to the V_V terminal successively via the horizontal signal line.

After the signal is read out from a photodiode, the photodiode is reset in the initial condition by V_V to store a new signal charge in preparation for the next scan period (16.7 ms).

This device permits the signals from two lines to be read out concurrently. After one two-line set is scanned, the next two-line set is selected by the vertical shift register and the same operation is repeated.

Pseudo-interlaced scanning is effected by altering the two-line combination to be scanned concurrently with the A and B fields.

The buffer circuit is used to apply voltage to the vertical gate line selected by the vertical shift register. In this device the

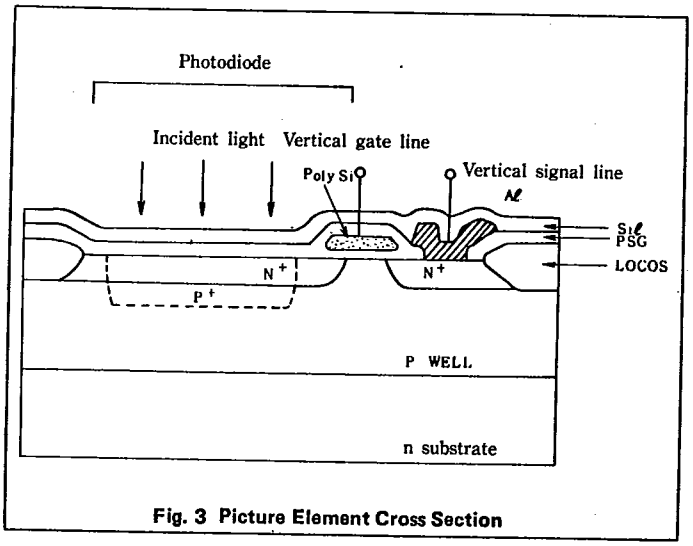


Fig. 3 Picture Element Cross Section

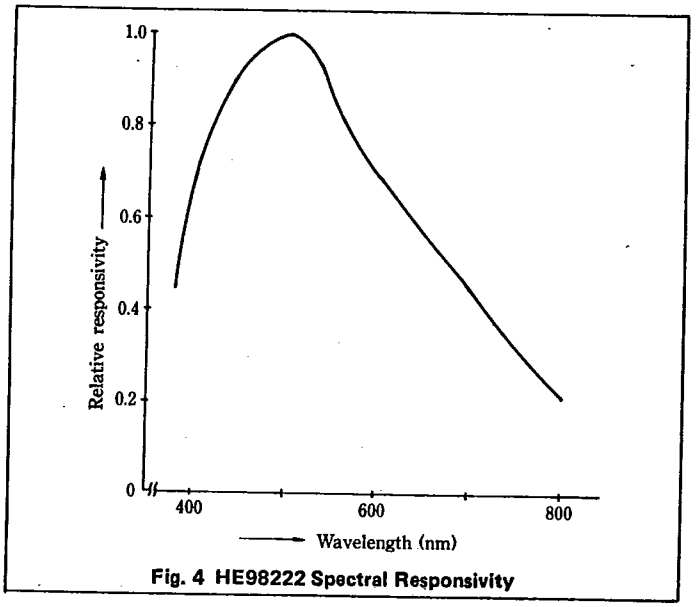


Fig. 4 HE98222 Spectral Responsivity

input voltage to the buffer circuit is divided into two (V_3 and V_4) to suppress flicker noise.
No buffer circuit is provided in the horizontal scanning section, however.
The WELL layer of the device cuts off long wavelength regions to provide a near-equivalent to the spectral characteristics of human sight, making the device best suited for use in VTR cameras.
The picture elements are equally spaced at 23 μm horizontal pitches and 13.5 μm vertical pitches to dispel geometric distortion in the images. The device thus provides a useful tool for measuring dimensions and areas throughout the images with precision and is suitable for instrumentation applications.

2. VERTICAL AND HORIZONTAL SHIFT REGISTERS

Both registers are dynamic, ratioless registers operating on the bootstrapping principle. Both registers consist of eight MOS FETs per step and use identical circuit setups. Each is driven by one synchronizing and two clock pulses. Timing charts of these pulses are given later in this catalog. In the horizontal shift register, V_{HIN} is a synchronizing pulse which is input to the first step of the shift register. V_{H1} and V_{H2} carry the synchronizing pulse sequentially to the subsequent steps.
The pulse height is $7V_{p\text{-}p}$. Provision is made to uniform the output waveform from each step. The horizontal drive (clock) frequency is 7.16 MHz, and the vertical drive (clock) frequency is 15.73 kHz.

HE98222 PERIPHERAL APPLICATION CIRCUIT

Figure 5 shows a typical peripheral application circuit for HE98222.
The device is driven by a drive circuit generating pulses like those outlined in Tables 1 and 2 and in the footnotes. Each of the two-output signals (S_1 and S_2) from the circuit are amplified by an independent preamplifier and an integrating circuit. The integrating circuit serves to cancel fixed-pattern noises generated in the device. The circuit setup is illustrated in Fig ure 6. A 70-ms delay circuit is provided for the S_2 output signal after integration. Its purpose is to reproduce the picture element interpolation effect at image pickup time to assure high resolution. The resultant S_1 and S_2 output signals are added and passed through a low-pass filter (LPF), then amplified to yield TV signals.

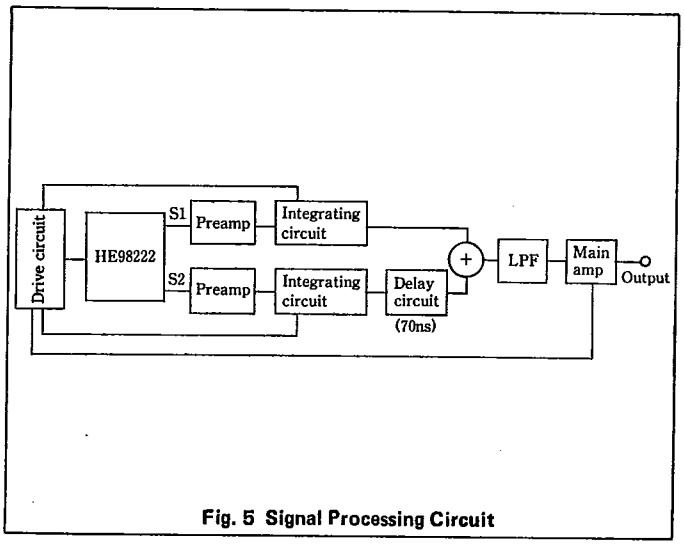


Fig. 5 Signal Processing Circuit

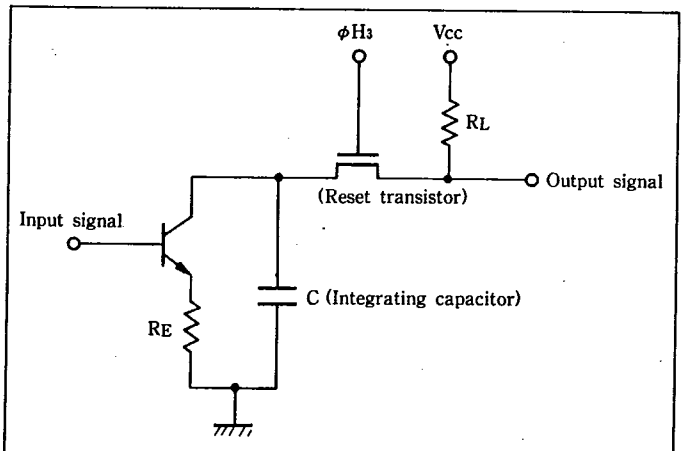


Fig. 6 Fixed-Pattern Noise Cancellation Circuit (Integrating Circuit)

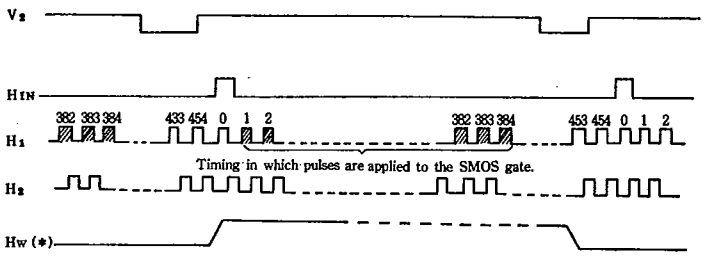
Table 1 Driving Conditions

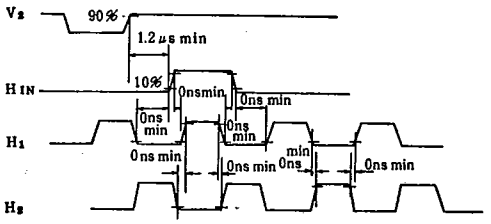
No.	Item	Symbol	Condition	Ratings			Unit
				Min-imum	Typi-cal	Max-imum	
1	Printed circuit board voltage	V_{SUB}		6.65	7.0	7.35	V
2	WELL voltage	V_{WPD}		0.7	0.8	0.9	V
3	Video voltage	V_{V1}, V_{V2}	Without light ir-radiation	2.85	3.0	3.15	V
4	High level of check pulse	V_{V1NH}, V_{V1H}, V_{V2H}, V_{FAH} V_{FBH}, V_{HINH}, V_{H1H}, V_{H2H}		6.65	7.0	7.35	V
5	Low level of check pulse	V_{V1NL}, V_{V1L}, V_{V2L}, V_{FAL}, V_{FBL}, V_{H1NL}		0.0	0.25	0.35	V
6	Kick high level of intialized pulse	V_{WVH} V_{WHH}		0.60	0.65	0.70	V
7	Low level of initialized pulse	V_{WVL} V_{WHL}		0	0.0	0.05	V
8	Test point	V_{HO}		–	0	–	V
9	Shift register source voltage	V_{VS}		–	0	–	V
10	Clock pulse frequency (H_1, L_1)	fH		–	7.16	–	MHz
11	Clock pulse frequency (H, V_1, V_2, V_3, V_4)	fV		–	15.73	–	KHz
12	Clock pulse frequency (V_{IN})	fI		–	60.0	–	Hz
13	Clock pulse frequency (F_A, F_B)	fF		–	30.0	–	Hz
14	Low level of a pulse clock	V_{H1L}, V_{H2L}		0.9	1.1	1.3	V
15	Horizontal shift register source voltage	V_{HS}		1.0	1.1	1.2	V
16	High level of pulse buffer	V_{V3H} V_{V4H}		6.65	7.0	7.35	V
17	Low level of pulse buffer	V_{V3L}, V_{V4L}		0.0	0.10	0.15	V

Note: Low level of clock pulse values for H_1 and H_2 include undershoots.

FOOTNOTES TO OPERATING CONDITIONS

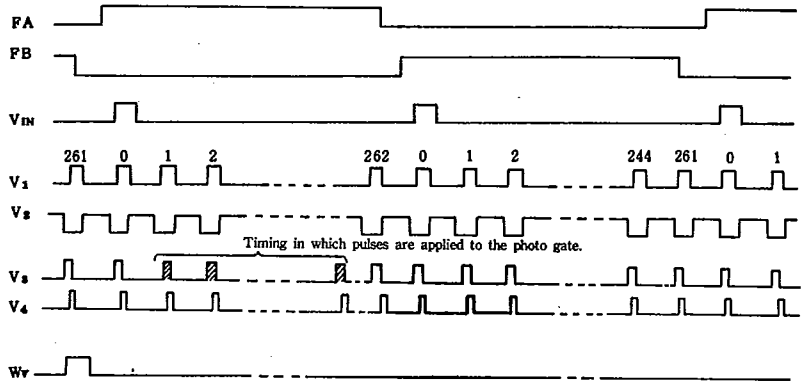
■ Horizontal Shift Register Clock Pulse Timing





*The H_W pulse must operate only once at power application, and the H_{IN}, H_1, and H_2 pulses must overlap for at least 0.5ms while the H_W pulse is at the high level.

■ **Vertical Shift Register Clock Pulse Timing**



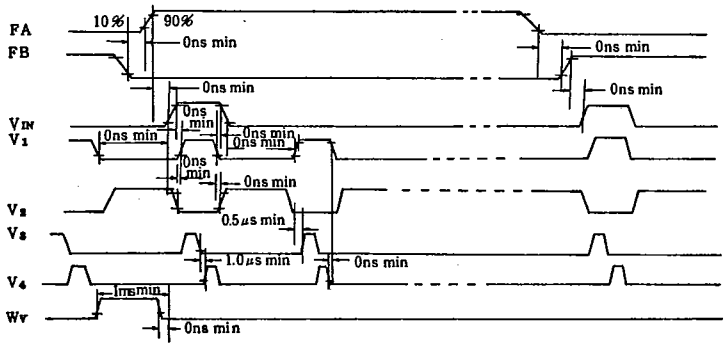
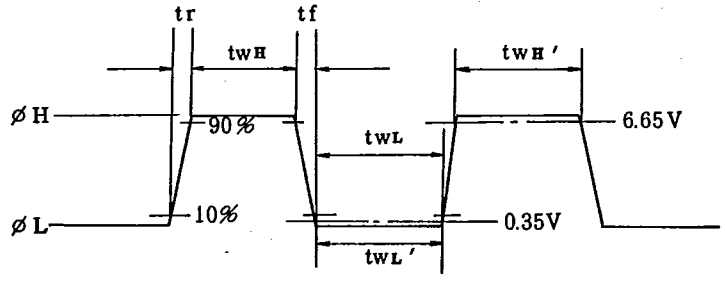
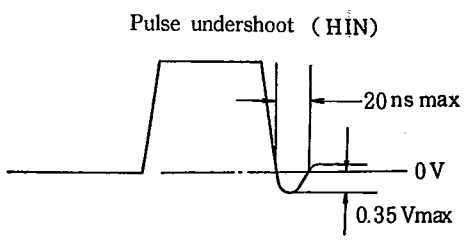


Table 2 Pulse Wave Form

Pin name	t_{WH}			t_{WH}			t_{WL}			t_{WL}			tr			tf			Unit
	Min-imum	Typi-cal	Max-imum	Min-imum	Typi-cal	Max-imum	Min-imum	Typi-cal	Max-imum	Min-imum	Typi-cal	Max-imum	Min-imum	Typi-cal	Max-imum	Min-imum	Typi-cal	Max-imum	
H1	35	40	45	30	37		55	70		50	67		10	15	20	10	15	20	ns
H2	35	40	45	30	37		55	70		50	67		10	15	20	10	15	20	ns
HIN	65	100											10	15	20	10	15	20	ns
V1	4.5	7.3											50ns	0.2	0.5	50ns	0.2	0.5	μs
V2	54	56						7.7					50ns	0.2	0.5	50ns	0.2	0.5	μs
V3	1.0	2.0											50ns	0.2	0.5	50ns	0.2	0.5	μs
V4	1.0	20											50ns	0.2	0.5	50ns	0.2	0.5	μs
VIN	4.6	64											50ns	0.1	0.5	50ns	0.1	0.5	μs
FA	15.0	15.5												0.2μs	0.5μs		0.2μs	0.5μs	ms
FB	15.0	15.5												0.2μs	0.5μs		0.2μs	0.5μs	ms
WV	1	—	10																ms
WH	1	—	10																ms





ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test condition	Minimum	Typical	Maximum	Unit
Saturation signal current	I_{SAT}	V_V=3V L=1.2 L_{SAT}	0.8	1.4	—	μA
Sensitivity	S	V_V=3V	10	13	—	nA/I_X
Signal uniformity	S_U		—	—	15	%
Horizontal resolution	R_H		—	500	—	TV lines
Vertical resolution	R_V		—	350	—	TV lines
Gama	r		—	1	—	—
Dark current	Id		—	—	10	nA
Power dissipation	P		—	60	100	mW
Input leak current	I_L	V_{SUB}= 7V maximum rating	—	—	10	μA

MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Value	Unit	Note
Operating temperature	Topr	−10~60	°C	1
Storage temperature	Tstg	−30~80	°C	
Terminal voltages Pin No. 1		0.0~9.0	V	2
Terminal voltages Pin No. 2		0.0~V_V	V	2,3
Terminal voltages Pin Nos. (*)		0.0~9.0	V	2,3,4
Terminal voltages Pin Nos. 10 and 15		0.0~0.7	V	2,4
Terminal voltages Pin No. 12		GND	V	
Exposure value		500,000	lx-hour	
Surface illumination		10,000	lx	

Pin Nos. (*): 3,4,5,6,7,8,11,13,14,16,17,18,19,20.

Notes: 1. Operating temperature refers to any temperature at which picture signals are obtained with both the horizontal and vertical shift registers operating.
2. Terminal voltages are those voltages appearing when Pin No. 9 is used as GND.
3. Do not apply voltage unless the conditions $V_{S1}=V_{V'}$ $V_{S2}=V_{V'}$ and $V_{SUB}\geqq V_V$ are satisfied.
4. Do not apply voltage unless the condition $V_{SUB}\geqq$=6.5V is satisfied.
5. When the undershoot of the pulse becomes 0.0V or lower at Pin No. 20 (HIN), limit it to the range specified in the footnote to the typical pulse waveform table given in this catalog.

TYPICAL OPERATING CONDITIONS

Pin No.	Pin name	Conditions (typical)
1	SUB	7.0V
2	WPD	0.8V
3	V3	High level of clock pulse (φH) 7.0V Low level of clock pulse (φL) 0.10V (φL>0V)
4	V2	
5	V1	High level of clock pulse (φH) 7.0V
6	VIN	Low level of clock pulse (φL) 0.25V
7	FA	(φL>0V)
8	FB	
9	VS	0.0V
10	WV	High level of intializing pulse 0.65V Low level of intializing pulse 0.0V
11	V4	High level of clock pulse (φH) 7.0V Low level of clock pulse (φL) 0.10V (φL> 0V)
12	GND	Non-connection GND
13	S2	3V
14	S1	3V
15	WH	High level of sychronized pulse 0.65V Low level of sychronized pulse 0.0V
16	HO	0.0V
17	HS	0.0V
18	H1	High level of clock pulse (φH) 7.0V
19	H2	Low level of clock pulse (φL) 0.25V
20	HIN	(φL>0V)

PIN ARRANGEMENT

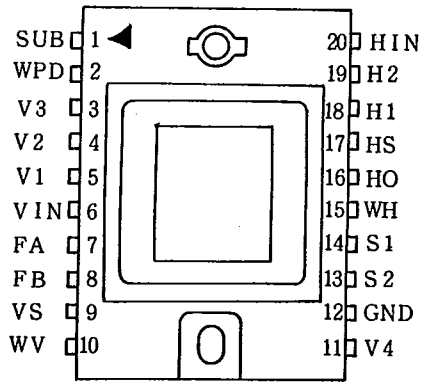
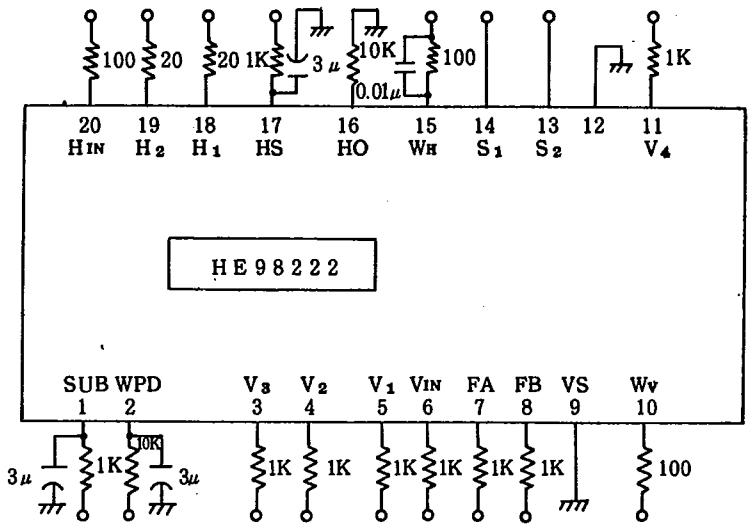


Fig. 7 Pin Arrangement

PROTECTIVE RESISTOR CONNECTION METHOD

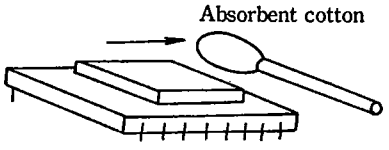


Units
Resistance : Ω
Capacitor : F

Fig. 8 Protective Resistor Connection Method

PRECAUTIONS

1) The Hitachi Monochrome Image Device HE98222, an MOSLSI, must be protected against electrostatic breakdown. When handling, ground the human body and associated apparatus as well. For the sake of added safety, insert a 1 MΩ resistor in series between the human body and GND. Also, connect protective resistors to protect the device as shown above.
2) Set V_{SUB} above 6.5V before applying any voltage or clock pulse to terminals.
3) When satisfied, these driving conditions assure:
   a Proper operation of the horizontal and the vertical shift register
   b Availability of picture signals.
4) Exercise utmost care in handling the device;
   7 VDC standard is applied to the copal metal on the back during operation.
5) Keep hands off the surface of the optical glass cap when handling the device. If a fingerprint or other foreign matter adheres to the glass surface because of contact, wipe it off in the following way:



Breathe upon the glass surface lightly enough to make it cloudy and wipe it slowly with a cotton swab moving it left to right about once a second.

Fig. 9 Image Device Handling

6) Take care not to drop the device, because the glass cap is fragile.
7) When storing or moving the device, store it in the case in which it was delivered. When installing the device in a camera, ensure that it will not be exposed to light except during operation.
8) Provide circuits to cancel dark currents, clock noise, and fixed-pattern noise.

Unit : mm

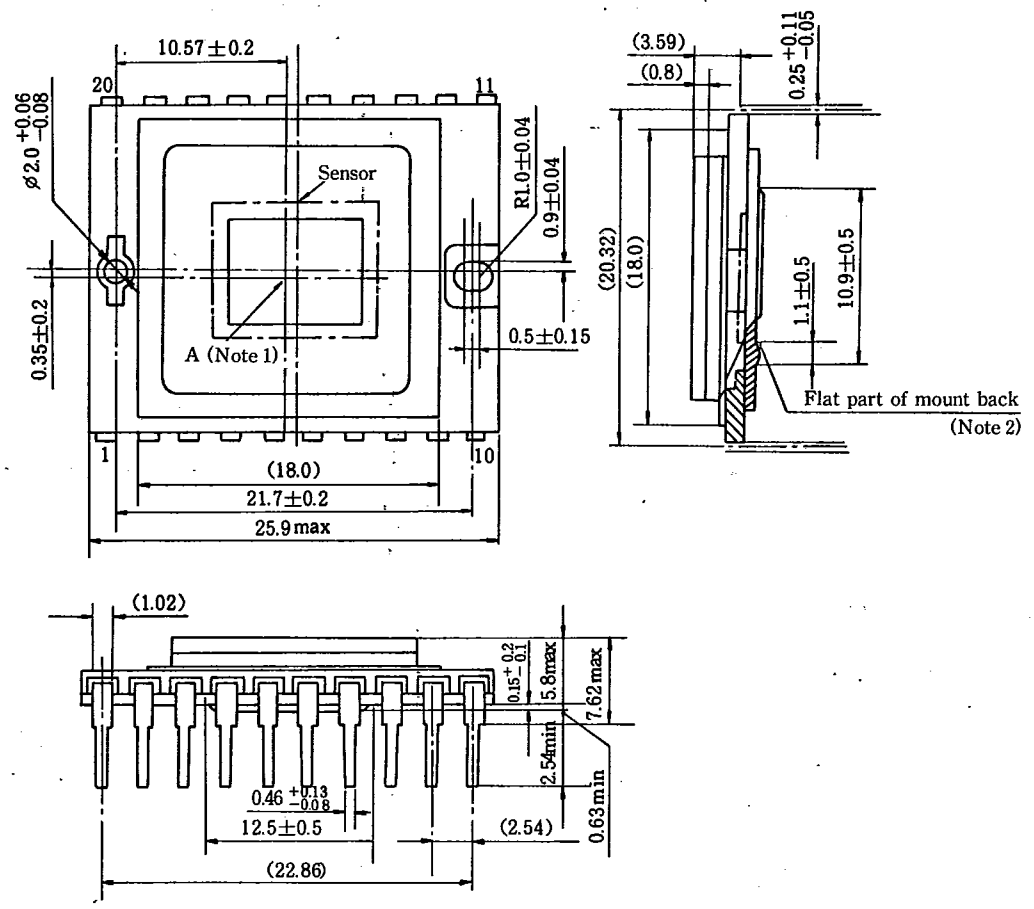


Fig. 10 Dimensional outline of HE98222

Notes : 1. Point A is the center of the photodiode array.
2. Install the package at the holes on both ends and the flat part of the mount back.

Hitachi, Ltd. 6-2, Otemachi 2-chome, Chiyoda-ku, Tokyo 100
Telephone: Tokyo (270) 2111 Cable: "HITACHY" TOKYO
Telex: J22395, 22432, 24491, 26375 (HITACHY)

For inquiry write to:

CHICAGO
Hitachi America, Ltd.
Chicago Office
500 Park Boulevard
Suite 805
Itasca, Illinois
60143
Telephone: (312) 773-0700
TWX: 910-651-3105

MÜNCHEN
Hitachi Electronic Components
Europe GmbH
Hans-Pinsel-Str 3,
8013 Haar, München
Telephone: 089-46140
Telex: 05-22593 (HITEC D)

LONDON
Hitachi Electronic Components
(U.K.) Ltd.
HITEC House, 221-225
Station Road, Harrow,
Middlesex, HA1 2XL
Telephone: 01-861 1414
Telex: 936293 (HITEC G)

HONG KONG
Hitachi Semiconductor (Hong Kong)
Ltd.
Room 706~707, 7/F., Wing On Plaza,
Salisbury Road, Tsimshatsu,
Knowloon, Hong Kong,
Telephone: 3-7219218~9
Telex: 40815 HISAL HX
FAX: 666164

Dec./1982 Catalog No. CE-E578 Printed in Japan TF-TF(H)

6